

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4516B

MSI

Binary up/down counter

Product specification
File under Integrated Circuits, IC04

January 1995

Binary up/down counter

HEF4516B MSI

DESCRIPTION

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input (CE), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P₀ to P₃), four parallel outputs (O₀ to O₃), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on P₀ to P₃ is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and CE are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when O₀ and O₃ are HIGH and CE is LOW. When counting down, TC is LOW when O₀ to O₃ and CE are LOW. A HIGH on MR resets the counter (O₀ to O₃ = LOW) independent of all other input conditions.

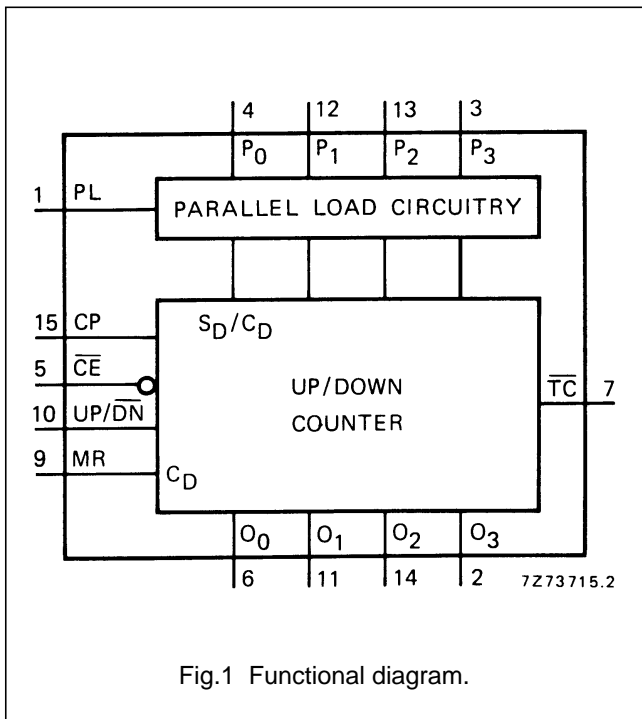


Fig.1 Functional diagram.

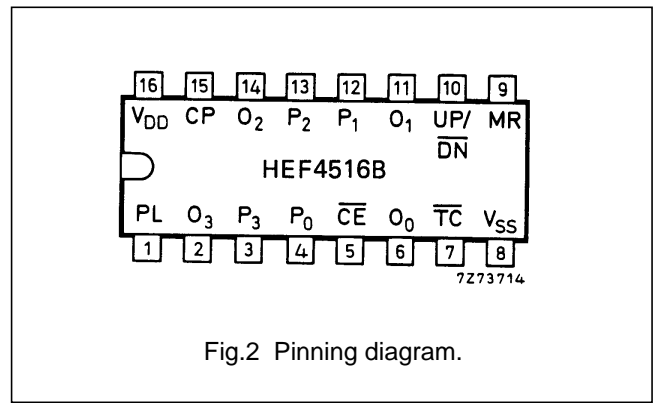


Fig.2 Pinning diagram.

PINNING

- PL parallel load input (active HIGH)
- P₀ to P₃ parallel inputs
- CE count enable input (active LOW)
- CP clock pulse input (LOW to HIGH, edge triggered)
- UP/DN up/down count control input
- MR master reset input
- TC terminal count output (active LOW)
- O₀ to O₃ parallel outputs

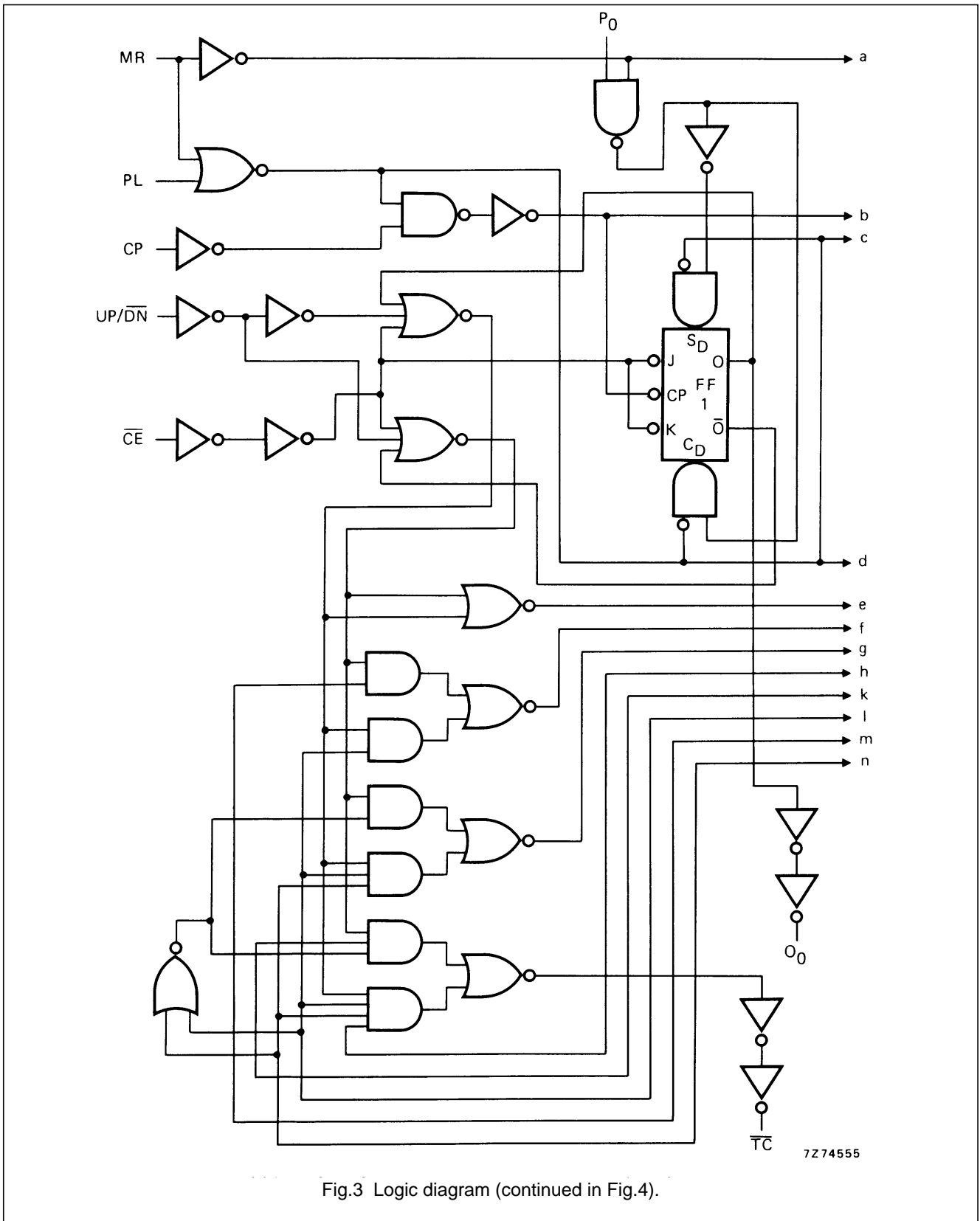
FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4516BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4516BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4516BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

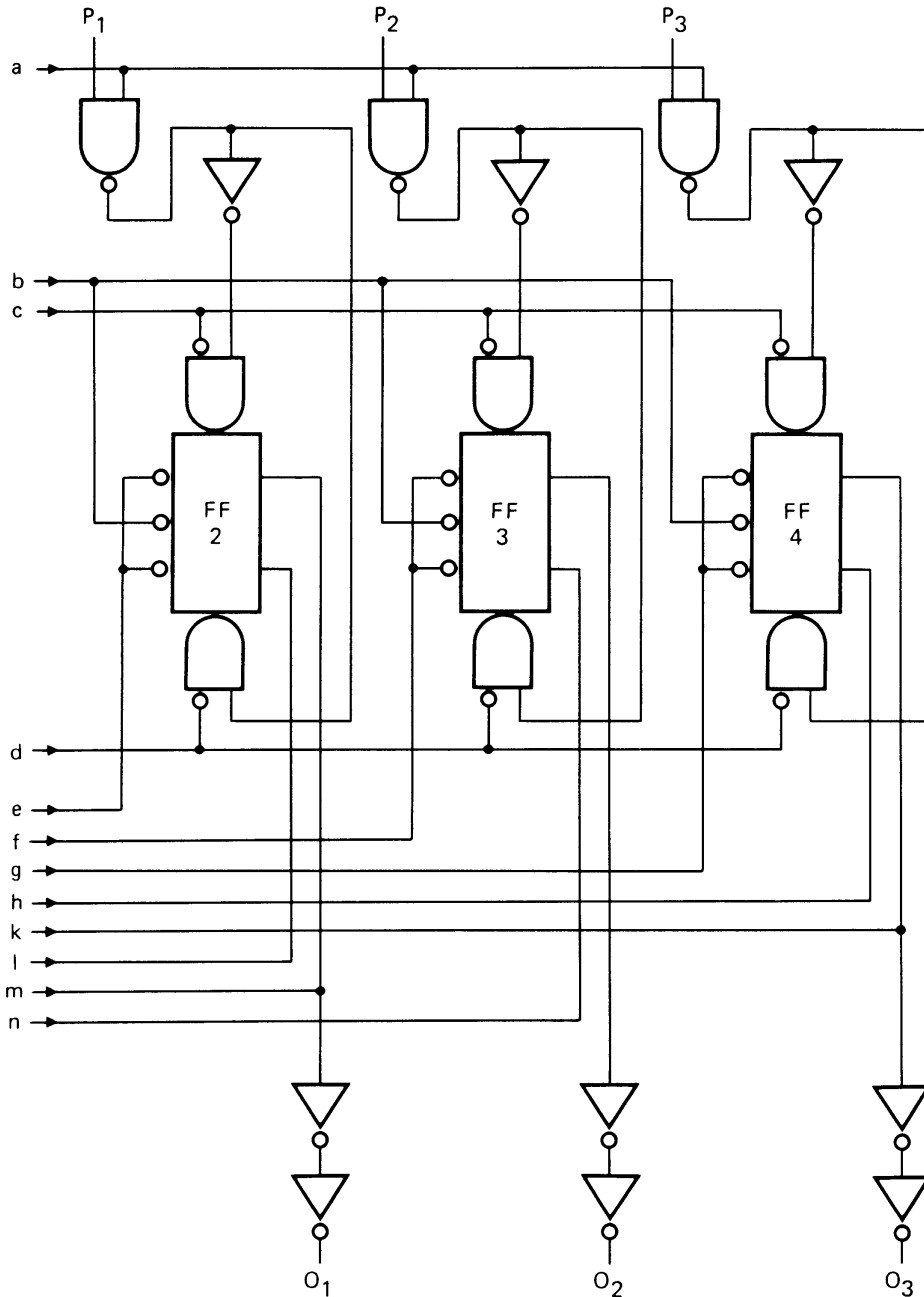
Binary up/down counter

HEF4516B
MSI



Binary up/down counter

HEF4516B
MSI



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Fig.4 Logic diagram (continued from Fig.3).

Binary up/down counter

HEF4516B
MSI

FUNCTION TABLE

MR	PL	UP/DN	\overline{CE}	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	\nearrow	count down
L	L	H	L	\searrow	count up
H	X	X	X	X	reset

Notes

- 1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- \nearrow = positive-going transition

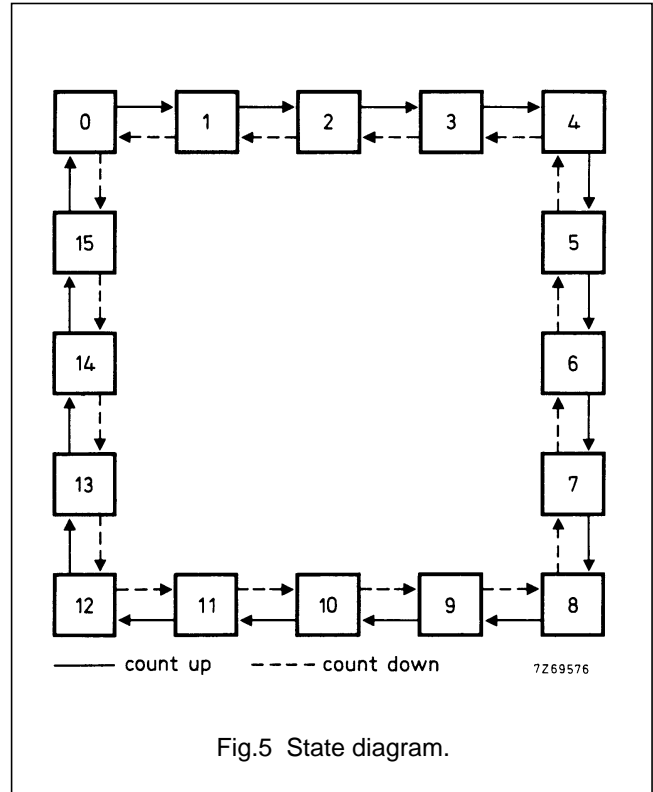


Fig.5 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + (\overline{UP/DN}) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \}$$

AC CHARACTERISTICS

$V_{SS} = 0 V$; $T_{amb} = 25 ^\circ C$; input transition times $\leq 20 ns$

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	$1000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $4500 f_i + \sum (f_o C_L) \times V_{DD}^2$ $11\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

Binary up/down counter

HEF4516B
MSI

AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP \rightarrow O_n	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		155	310 ns	128 ns + (0,55 ns/pF) C_L
	10			65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
CP \rightarrow \overline{TC}	5			260	525 ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210 ns	94 ns + (0,23 ns/pF) C_L
	15			75	150 ns	67 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		180	360 ns	153 ns + (0,55 ns/pF) C_L
	10			75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			55	115 ns	47 ns + (0,16 ns/pF) C_L
PL \rightarrow O_n	5			125	255 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	85 ns	32 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		170	340 ns	143 ns + (0,55 ns/pF) C_L
	10			70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
PL \rightarrow \overline{TC}	5			250	500 ns	223 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		110	220 ns	99 ns + (0,23 ns/pF) C_L
	15			80	160 ns	72 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		250	500 ns	223 ns + (0,55 ns/pF) C_L
	10			110	220 ns	99 ns + (0,23 ns/pF) C_L
	15			80	160 ns	72 ns + (0,16 ns/pF) C_L
$\overline{CE} \rightarrow \overline{TC}$	5			165	330 ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		145	290 ns	118 ns + (0,55 ns/pF) C_L
	10			60	125 ns	49 ns + (0,23 ns/pF) C_L
	15			45	95 ns	37 ns + (0,16 ns/pF) C_L
MR \rightarrow O_n, \overline{TC}	5			205	405 ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
MR \rightarrow \overline{TC}	5			225	450 ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L

Binary up/down counter

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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

Binary up/down counter

HEF4516B
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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Minimum clock pulse width; LOW	5	t _{WCPL}	95	45	ns	see also waveforms Figs 6 and 7	
	10		35	20	ns		
	15		25	15	ns		
Minimum PL pulse width; HIGH	5	t _{WPLH}	105	55	ns		
	10		45	25	ns		
	15		35	15	ns		
Minimum MR pulse width; HIGH	5	t _{WMRH}	120	60	ns		
	10		50	25	ns		
	15		40	20	ns		
Recovery time for MR	5	t _{RMR}	130	65	ns		
	10		45	20	ns		
	15		30	15	ns		
Recovery time for PL	5	t _{RPL}	150	75	ns		
	10		50	25	ns		
	15		30	15	ns		
Set-up times P _n → PL	5	t _{su}	100	50	ns		
	10		50	25	ns		
	15		40	20	ns		
	UP/ $\overline{\text{DN}}$ → CP	5	t _{su}	250	125		ns
		10		100	50		ns
		15		75	35		ns
	$\overline{\text{CE}}$ → CP	5	t _{su}	120	60	ns	
		10		40	20	ns	
		15		25	10	ns	
Hold times P _n → PL	5	t _{hold}	10	-40	ns		
	10		5	-20	ns		
	15		0	-20	ns		
	UP/ $\overline{\text{DN}}$ → CP	5	t _{hold}	35	-90	ns	
		10		15	-35	ns	
		15		15	-25	ns	
	$\overline{\text{CE}}$ → CP	5	t _{hold}	20	-40	ns	
		10		5	-15	ns	
		15		5	-10	ns	
Maximum clock pulse frequency	5	f _{max}	3	6	MHz		
	10		7	14	MHz		
	15		9	18	MHz		

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MSI

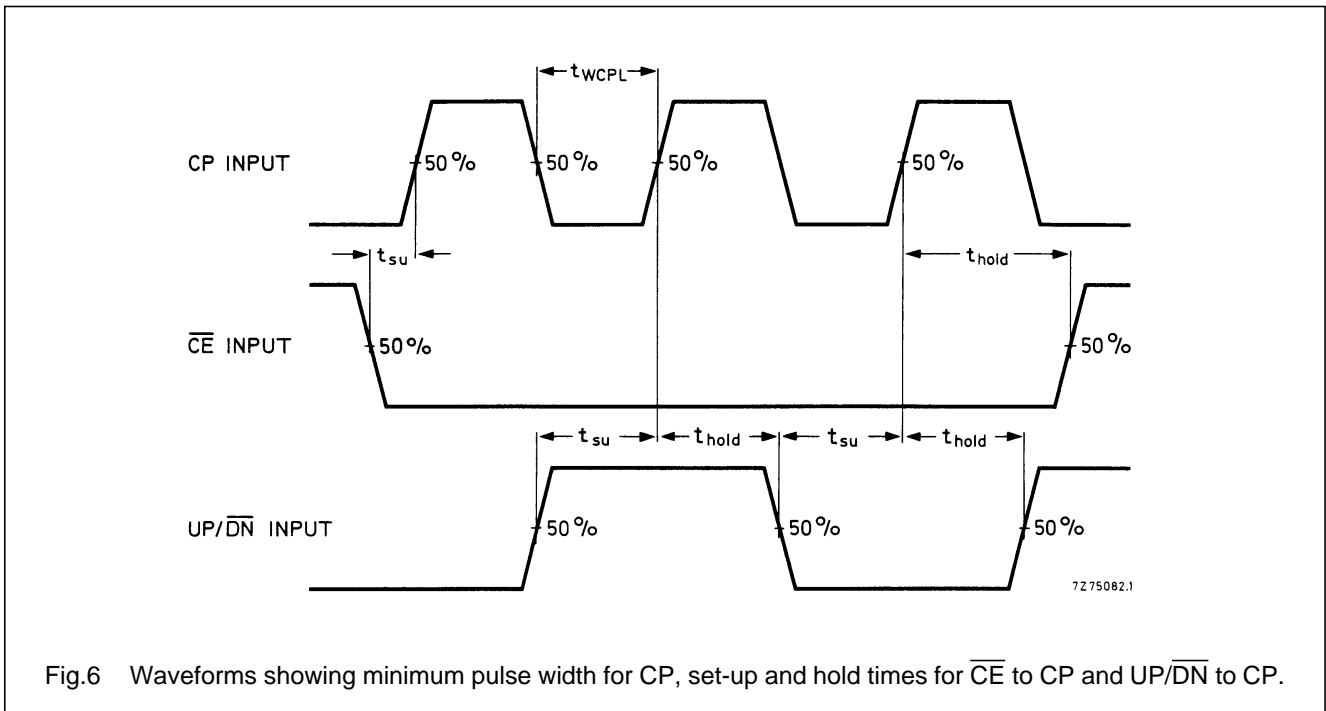


Fig.6 Waveforms showing minimum pulse width for CP, set-up and hold times for \overline{CE} to CP and UP/ \overline{DN} to CP.

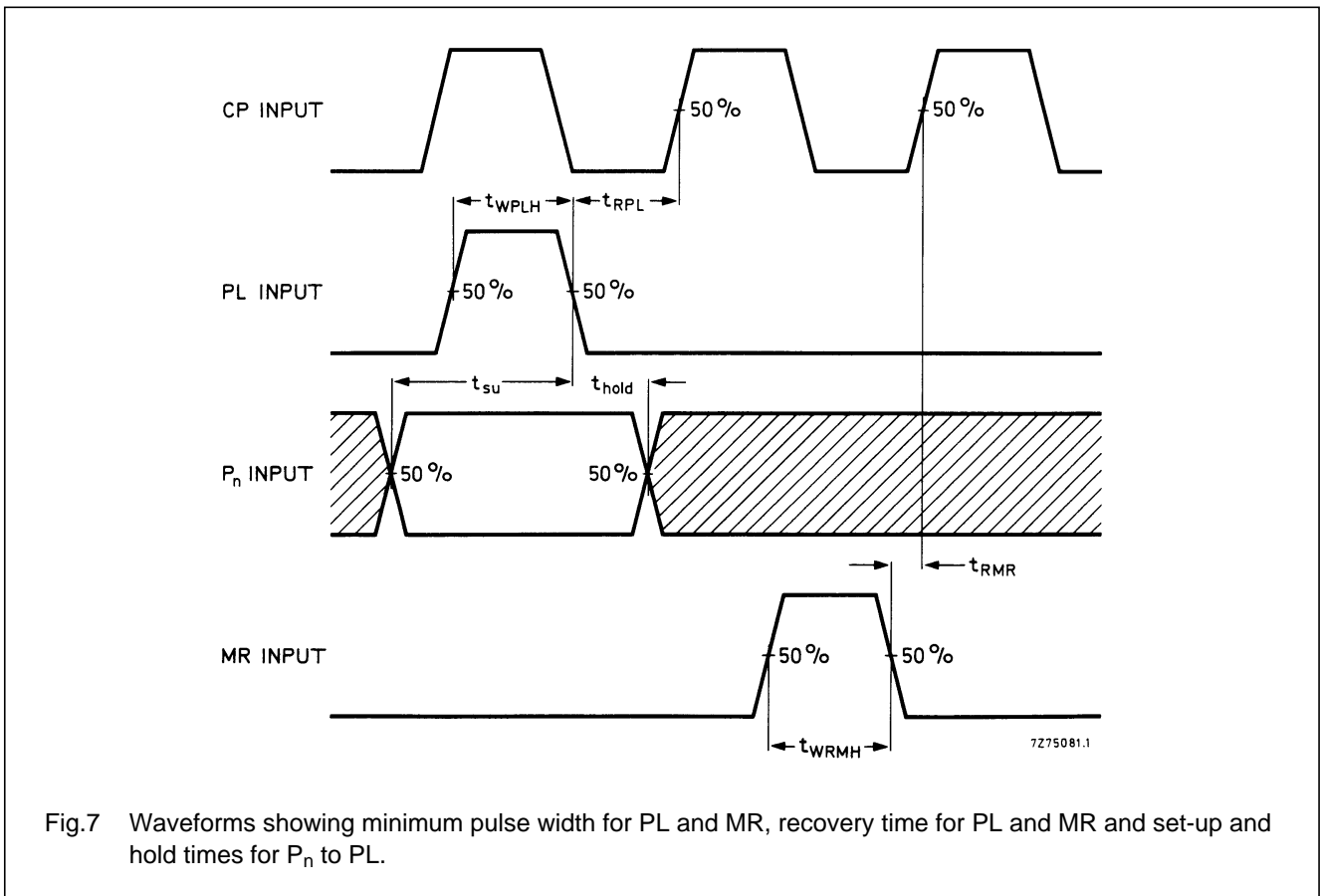


Fig.7 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

Binary up/down counter

HEF4516B
MSI

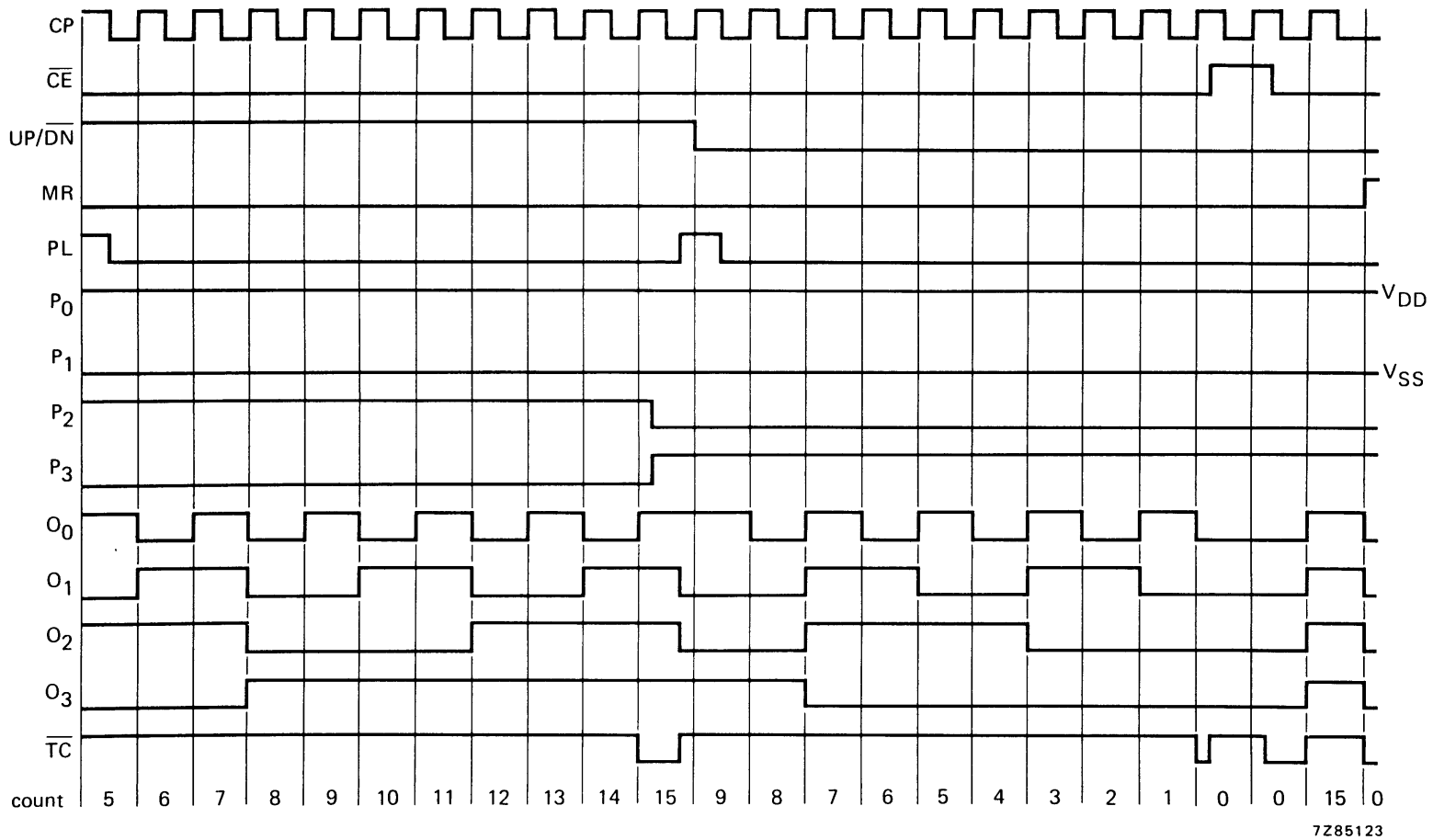
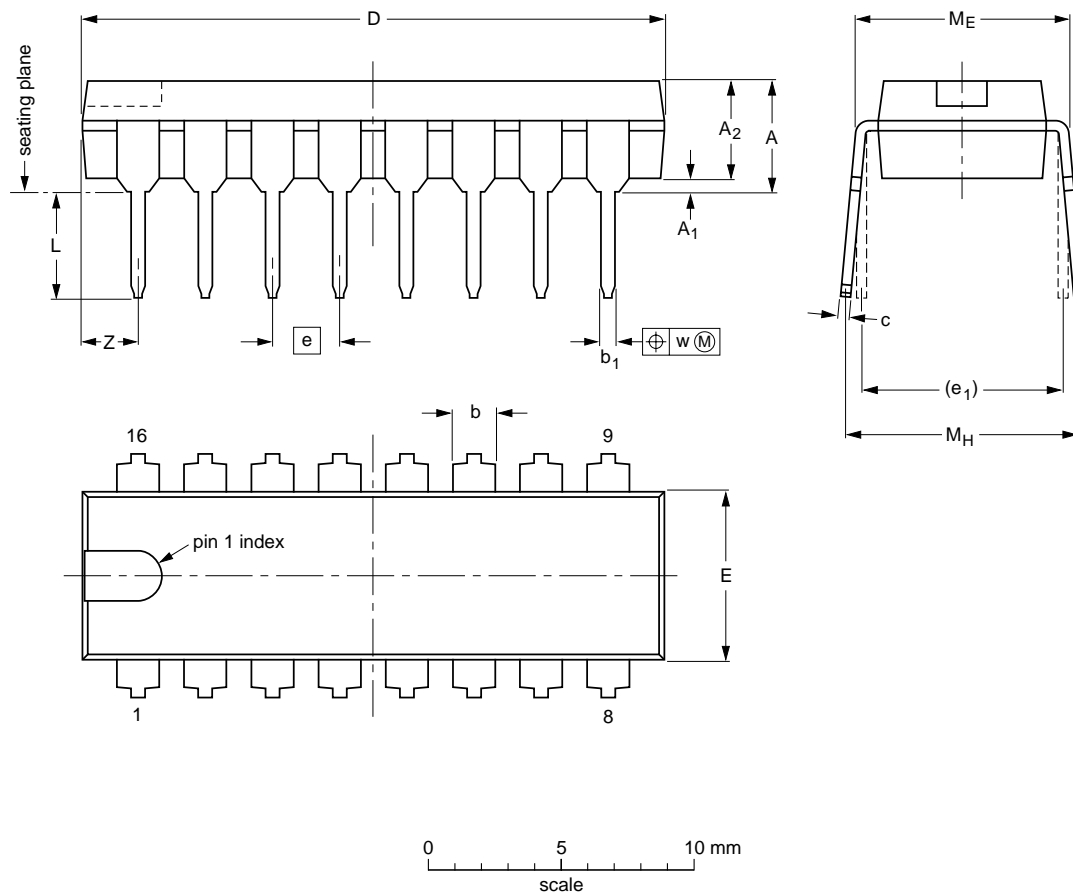


Fig.8 Timing diagram.

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

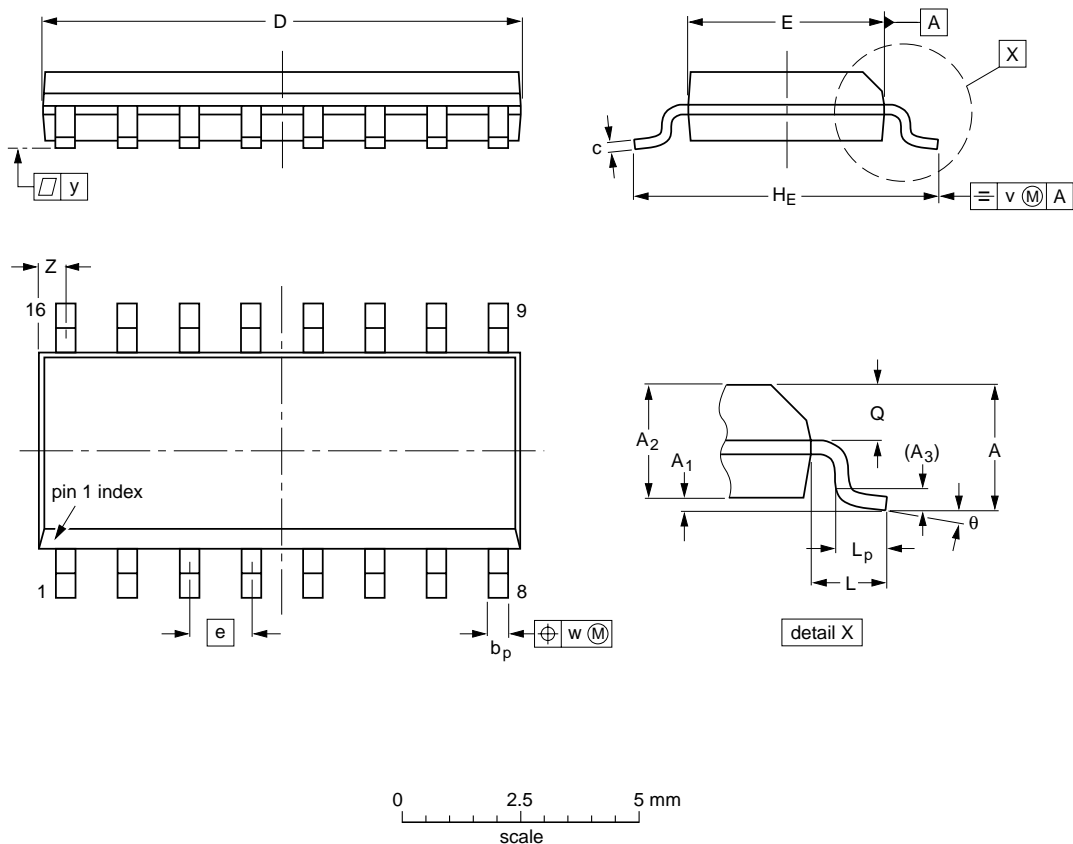
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22