

## Evaluation Board for a Quad-Channel, 16-Bit, Serial Input, 4 mA to 20 mA, Voltage Output DAC with Dynamic Power Control and HART Connectivity

### FEATURES

**Full-featured evaluation board for the AD5755, AD5755-1, AD5757, and**

**Link options**

**PC control in conjunction with Analog Devices, Inc., system demonstration platform (SDP)**

**PC software for control**

### GENERAL DESCRIPTION

The EVAL-AD575xSDZ is a full-featured evaluation board that is designed to allow the user to easily evaluate all features of the [AD5755](#), [AD5755-1](#), or [AD5757](#), quad channel, 16-bit current source and voltage output DAC with dynamic power control and HART connectivity. The board can be controlled by two means: via the on-board connector (J11) or via the SDP connector (J9). The SDP board allows the evaluation board to be controlled through the USB port of a Windows® XP® (SP2 or later) or Windows Vista® (32-bit or 64-bit) or Windows 7 (32-bit or 64-bit) based PC using the EVAL-AD575xSDZ evaluation software.

### DEVICE DESCRIPTION

The [AD5755](#) is a quad, voltage and current output DAC that operates with a power supply range from  $-26.4\text{ V}$  to  $+33\text{ V}$ . On-chip dynamic power control minimizes package power dissipation in current mode. This is achieved by regulating the voltage on the output driver from  $7.4\text{ V}$  to  $29.5\text{ V}$ .

The part uses a versatile 3-wire serial interface that operates at clock rates up to  $30\text{ MHz}$  and is compatible with standard SPI, QSPI™, MICROWIRE™, DSP, and microcontroller interface standards. The interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

The [AD5757](#) is a current output-only version of the [AD5755](#) and is HART compatible. The [AD5755-1](#) is identical to the [AD5755](#) except the  $-V_{\text{SENSE}_x}$  functionality has been removed and, instead, the device is HART compatible. For both the [AD5757](#) and [AD5755-1](#), each channel has a corresponding CHART pin so that HART signals can be coupled onto the current output.

### EVALUATION BOARD CONNECTION DIAGRAM

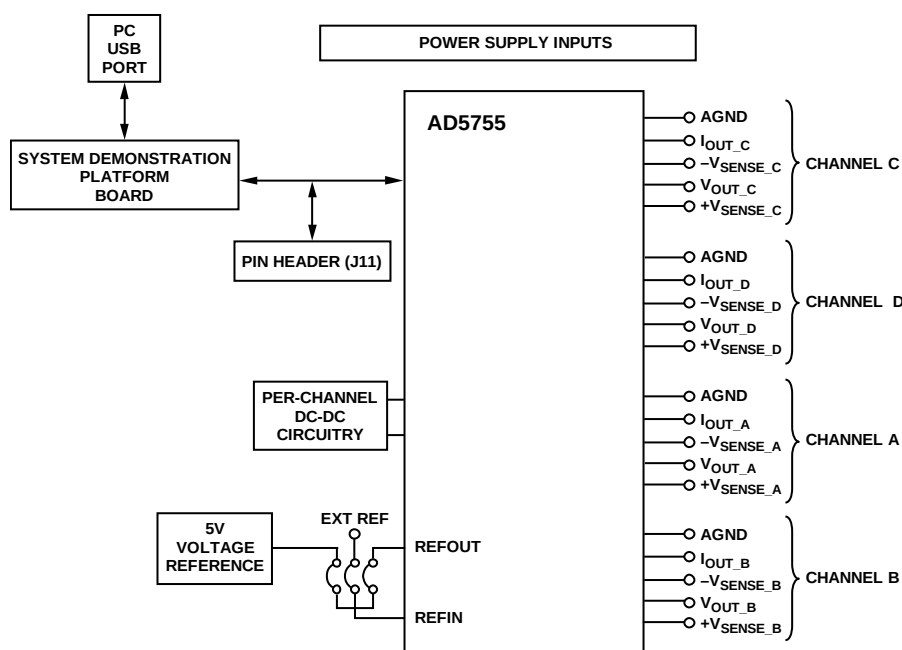


Figure 1.

## TABLE OF CONTENTS

|                                           |   |                                                 |    |
|-------------------------------------------|---|-------------------------------------------------|----|
| Features .....                            | 1 | Changing and Reprogramming the Range .....      | 6  |
| General Description .....                 | 1 | Clear Command .....                             | 6  |
| Device Description .....                  | 1 | Control of Digital Pins .....                   | 7  |
| Evaluation Board Connection Diagram ..... | 1 | Writing to Data Registers .....                 | 7  |
| Revision History .....                    | 2 | Reading from Registers .....                    | 7  |
| Evaluation Board Hardware .....           | 3 | Writing to the DAC Control Registers .....      | 7  |
| Power Supplies .....                      | 3 | Writing to the DC-to-DC Control Register .....  | 8  |
| Link Options .....                        | 3 | Writing to the Main Control Register .....      | 8  |
| Output Connectors .....                   | 4 | Writing to the Slew Rate Control Register ..... | 8  |
| DC-to-DC Boost .....                      | 4 | Software Register .....                         | 9  |
| Patchwork .....                           | 4 | PEC .....                                       | 9  |
| System Demonstration Platform (SDP) ..... | 4 | Status Readback .....                           | 9  |
| Evaluation Board Software .....           | 5 | Evaluation Board Schematics and Artwork .....   | 10 |
| Software Installation .....               | 5 | Ordering Information .....                      | 15 |
| Software Operation .....                  | 5 | Bill of Materials .....                         | 15 |
| Selecting the Device .....                | 6 | Related Links .....                             | 15 |
| Enabling the Output Correctly .....       | 6 |                                                 |    |

## REVISION HISTORY

### 4/13—Rev. A to Rev. B

|                          |   |
|--------------------------|---|
| Changes to Table 1 ..... | 3 |
|--------------------------|---|

### 6/11—Rev. 0 to Rev. A

|                                                            |           |
|------------------------------------------------------------|-----------|
| Added AD5755 and AD5757 .....                              | Universal |
| Changes to Table 2 .....                                   | 3         |
| Added Table 5 and Table 6; Renumbered Sequentially;        |           |
| Changes to Table 6, and Changes to Patchwork Section ..... | 4         |
| Changes to Bill of Materials Section and Related Links     |           |
| Section .....                                              | 15        |

### 5/11—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

The following power supplies are required.

**Table 1. Power Supply Connections**

| Connector        | Nominal        | Comment                                                                                                                                                                                                                                                       |
|------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AV <sub>DD</sub> | 15 V           | Positive analog supply voltage. 10.8 V to 33 V range. (Green LED D2 lights up when power is supplied to AV <sub>DD</sub> .)                                                                                                                                   |
| AV <sub>SS</sub> | –15 V/<br>+0 V | Negative analog supply voltage. +10.8 V to –26.4 V range, or 0 V for the <a href="#">AD5757</a> or <a href="#">AD5755-1</a> in unipolar supply mode.                                                                                                          |
| AV <sub>CC</sub> | 5 V            | DC-to-dc supply voltage. 4.5 V to 5.5 V range. The AV <sub>CC</sub> input supplies all four on-board dc-to-dc blocks and may draw as much as 0.8 A peak current per channel, depending on the configuration (see the device data sheet for more information). |
| DV <sub>DD</sub> | 3.3 V          | Supplied from the SDP connector. 2.7 V to 5.5 V range.                                                                                                                                                                                                        |
| REFIN            | 5 V            | See Table 3 for selecting the reference source: the AD575x internal reference, the on-board <a href="#">ADR02</a> reference, or externally provided via the REFIN input.                                                                                      |

Both analog AGND and PGND inputs are provided on the board. The PGND input is for the ground of the dc-to-dc converter circuitry, and a ground connection for the AV<sub>CC</sub> supply should be made at this point. The AGND and PGND planes are connected at one location on the evaluation board.

The AGND and DGND planes are connected at one location close to the [AD5755](#), [AD5755-1](#), or [AD5757](#) device. Each supply is decoupled to the relevant ground plane with 10  $\mu$ F and 0.1  $\mu$ F capacitors. Each device supply pin is also decoupled with a 10  $\mu$ F and 0.1  $\mu$ F capacitor pair to the relevant ground plane.

### LINK OPTIONS

The link options on the evaluation board should be set for the required operating setup before using the board. The functions of the link options are described in Table 3.

#### Default Link Option Setup

The default link options are listed in Table 2.

**Table 2. Default Link Options**

| Link No. | <a href="#">AD5755</a> Link Setup | <a href="#">AD5755-1</a> Link Setup | <a href="#">AD5757</a> Link Setup |
|----------|-----------------------------------|-------------------------------------|-----------------------------------|
| LK0      | Removed                           | Removed                             | Removed                           |
| LK1      | Removed                           | Removed                             | Removed                           |
| LK2      | Inserted                          | Inserted                            | Inserted                          |
| LK3      | Inserted                          | Inserted                            | Inserted                          |
| LK4      | Inserted                          | Inserted                            | Removed                           |
| LK5      | Inserted                          | Removed                             | Removed                           |
| LK6      | Inserted                          | Inserted                            | Removed                           |
| LK7      | Inserted                          | Removed                             | Removed                           |
| LK8      | Inserted                          | Inserted                            | Removed                           |
| LK9      | Inserted                          | Removed                             | Removed                           |
| LK10     | Inserted                          | Inserted                            | Removed                           |
| LK11     | Inserted                          | Removed                             | Removed                           |
| LK12     | Removed                           | Removed                             | Removed                           |
| LK13     | Removed                           | Removed                             | Removed                           |
| LK14     | Removed                           | Removed                             | Removed                           |
| LK15     | Removed                           | Removed                             | Removed                           |

**Table 3. Link Options**

| Link No.                  | Device              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LK0, LK1, LK2             | All Models          | These links select the voltage reference source (only one of these should be inserted at any one time). LK0 selects the internal voltage reference of the AD575x as the voltage reference source. LK1 selects an external voltage reference source that can be applied at Connector J7. LK2 selects the on-board <a href="#">ADR02</a> as the voltage reference source. The ADR02 is supplied by the AV <sub>DD</sub> supply and operates under the same input voltage range as the AV <sub>DD</sub> input of the AD575x, that is 9 V to 33 V. |
| LK3                       | All Models          | Powers the on-board <a href="#">ADR02</a> 5 V reference by connecting the AV <sub>DD</sub> supply to the ADR02 supply pin.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| LK4, LK6<br>LK10, LK8,    | AD5755,<br>AD5755-1 | These links connect the +V <sub>SENSE</sub> input to V <sub>OUT</sub> for Channel A, Channel B, Channel C, and Channel D, respectively. When this link is inserted, the +V <sub>SENSE</sub> input is connected directly to the V <sub>OUTX</sub> pin. When this link is removed, the +V <sub>SENSE</sub> input is left floating and should be connected to the high-side of the load resistance external to the evaluation board.                                                                                                              |
| LK5, LK7 LK9,<br>LK11,    | AD5755              | These links connect the +V <sub>SENSE</sub> input to V <sub>OUT</sub> for Channel A, Channel B, Channel C, and Channel D, respectively. When this link is inserted, the +V <sub>SENSE</sub> input is connected directly to the V <sub>OUT</sub> pin. When this link is removed, the +V <sub>SENSE</sub> input is left floating and should be connected to the high-side of the load resistance external to the evaluation board.                                                                                                               |
| LK12, LK13,<br>LK14, LK15 | All Models          | These links allow connection of an external V <sub>BOOST</sub> supply. (Remove Resistors R43, R44, R17, and R20 to use this feature.) When inserted, these connect the V <sub>BOOST</sub> pin of Channel A, Channel B, Channel C, and Channel D, respectively, to the AV <sub>DD</sub> supply. When removed, the V <sub>BOOST</sub> supplies are controlled by the dc-to-dc converter circuitry.                                                                                                                                               |

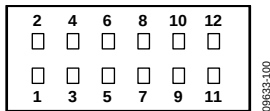
**Connector J11 Pin Descriptions**

Figure 2. Connector J11 Pin Configuration

**Table 4. Connector J11 Pin Descriptions<sup>1</sup>**

| Pin No. | Description               |
|---------|---------------------------|
| 1       | DV <sub>DD</sub>          |
| 2       | DGND                      |
| 3       | SYNC                      |
| 4       | SCLK                      |
| 5       | SDIN                      |
| 6       | SDO (output)              |
| 7       | LDAC                      |
| 8       | CLEAR                     |
| 9       | POC (AD5755 and AD5755-1) |
| 10      | RESET                     |
| 11      | FAULT (output)            |
| 12      | ALERT (output)            |

<sup>1</sup> The SDP board must be disconnected when using the J11 connector.

**OUTPUT CONNECTORS**

There are five connectors per channel on the EVAL-AD575xSDZ PCB. The output connectors are used as outlined in Table 5, Table 6, and Table 7.

**Table 5. On-Board Connectors for AD5755**

| Connector      | Function                                                                                    |
|----------------|---------------------------------------------------------------------------------------------|
| GND            | There is a per-channel connection to AGND.                                                  |
| A1, B1, C1, D1 | I <sub>OUT</sub> output for Channel A, Channel B, Channel C, and Channel D, respectively.   |
| A2, B2, C2, D2 | –V <sub>SENSE</sub> input for Channel A, Channel B, Channel C, and Channel D, respectively. |
| A3, B3, C3, D3 | V <sub>OUT</sub> output for Channel A, Channel B, Channel C, and Channel D, respectively.   |
| A4, B4, C4, D4 | +V <sub>SENSE</sub> input for Channel A, Channel B, Channel C, and Channel D, respectively. |

**Table 6. On-Board Connectors for AD5757**

| Connector      | Function                                                                                                                                                                         |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND            | There is a per-channel connection to AGND.                                                                                                                                       |
| A1, B1, C1, D1 | I <sub>OUT</sub> output for Channel A, Channel B, Channel C, and Channel D, respectively.                                                                                        |
| A2, B2, C2, D2 | CHART input for Channel A, Channel B, Channel C, and Channel D, respectively. HART signals should be capacitively coupled onto these pins as described in the AD5757 data sheet. |
| A4, B3, C3, D4 | Connection to the IGATE <sub>x</sub> pin                                                                                                                                         |
| A3, B4, C4, D3 | Not used.                                                                                                                                                                        |

**Table 7. On-Board Connectors for AD5755-1**

| Connector      | Function                                                                                                                                                                           |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND            | There is a per-channel connection to AGND.                                                                                                                                         |
| A1, B1, C1, D1 | I <sub>OUT</sub> output for Channel A, Channel B, Channel C, and Channel D, respectively.                                                                                          |
| A2, B2, C2, D2 | CHART input for Channel A, Channel B, Channel C, and Channel D, respectively. HART signals should be capacitively coupled onto these pins as described in the AD5755-1 data sheet. |
| A3, B3, C3, D3 | V <sub>OUT</sub> output for Channel A, Channel B, Channel C, and Channel D, respectively.                                                                                          |
| A4, B4, C4, D4 | +V <sub>SENSE</sub> input for Channel A, Channel B, Channel C, and Channel D, respectively.                                                                                        |

**DC-TO-DC BOOST**

Each channel has a dc-to-dc boost converter. This consists of a Schottky diode, inductor, and a low ESR, high voltage capacitor. A low-pass RC filter is also included on a per-channel basis.

**Table 8. DC-to-DC Circuitry**

| Symbol              | Component          | Value               | Manufacturer |
|---------------------|--------------------|---------------------|--------------|
| L <sub>DCDC</sub>   | XAL4040-103        | 10 μH               | Coilcraft    |
| C <sub>DCDC</sub>   | GRM32ER71H475KA88L | 4.7 μF              | Murata       |
| D <sub>DCDC</sub>   | PMEG3010BEA        | 0.38 V <sub>F</sub> | NXP          |
| R <sub>FILTER</sub> | N/A                | 10 Ω                | N/A          |
| C <sub>FILTER</sub> | N/A                | 0.1 μF              | N/A          |

The L<sub>DCDC</sub> 10 μH inductor provides the best performance at the 410 kHz switching frequency. Consult the AD5755, AD5755-1, AD5757, or data sheet for more information on the dc-to-dc converter circuitry.

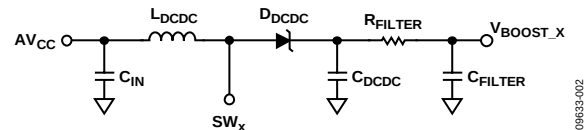


Figure 3. DC-to-DC Converter Circuitry

**PATCHWORK**

Patchwork is included on the EVAL-AD575xSDZ near the output connectors. This is connected in rows with one row connected to AGND per channel and one row connected to I<sub>OUT</sub> per channel. All other rows are left floating.

When evaluating the EVAL-AD5757SDZ, the patchwork gives access to the drain, gate and source of a discreet PMOS transistor which can be used to evaluate the Igate functionality.

**SYSTEM DEMONSTRATION PLATFORM (SDP)**

The EVAL-AD575xSDZ board can connect to the SDP board via the J9 connector. The SDP is a hardware and software platform that provides a means to communicate from the PC to supported Analog Devices products and systems that require digital control and/or readback. The SDP has a Blackfin® (BF527) at its core. This has on-chip USB 2.0 capabilities as well as many external interface ports, such as SPI, SPORT, I<sup>2</sup>C, and a 16-bit parallel interface. See Figure 20 for connections made to the SDP board.

## EVALUATION BOARD SOFTWARE

### SOFTWARE INSTALLATION

The EVAL-AD575xSDZ evaluation kit includes self-installing software on a CD. The software is compatible with Windows XP (SP2) and Windows Vista (32-bit or 64-bit), and Windows 7 (32-bit or 64-bit). If the setup file does not run automatically, you can run **setup.exe** from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. After installation from the CD is complete, power up the EVAL-AD575xSDZ as described in the Power Supplies section.
2. Next, connect the SDP board to the EVAL-AD575xSDZ and then to the USB port of your PC using the supplied cable.
3. When the evaluation system is detected, proceed through any dialog boxes that appear. This finishes the installation.

### SOFTWARE OPERATION

To launch the software, complete the following steps:

1. From the **Start** menu, select **Analog Devices –AD5755 AD5757 AD5755-1**, and then select **AD5755 AD5757**

**AD5755-1 Evaluation Software.** The main window of the software opens (see Figure 5).

2. If the evaluation system is not connected to the USB port when the software is launched, a connectivity error is displayed (see Figure 4). Simply connect the evaluation board to the USB port of the PC, wait a number of seconds, and click **Rescan**. Follow the instructions.

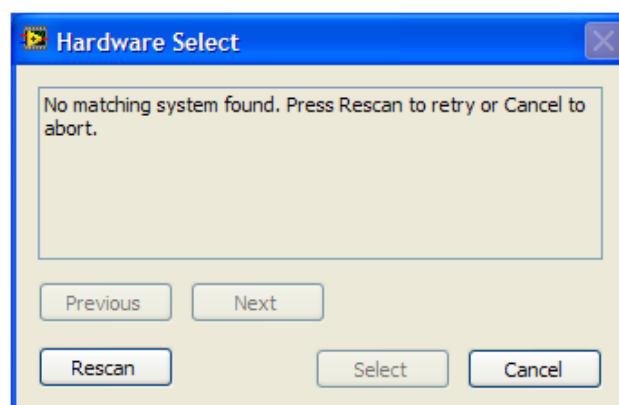


Figure 4. Connectivity Error Alert



Figure 5. Main Window

## SELECTING THE DEVICE



Figure 6. Device Selection

In the top left corner of the main window, select the main device on the board, either AD5755, AD5755-1, or AD5757, from the drop-down list (see Figure 6) to adjust the available controls accordingly.

## ENABLING THE OUTPUT CORRECTLY

To correctly write to and set up the part from a power-on condition, use the following sequence.

1. Perform a hardware or software reset after initial power-on.
2. The dc-to-dc converter supply block must be configured. Set the dc-to-dc switching frequency, maximum output voltage allowed, and the phase that the four dc-to-dc channels clock at.
3. Configure the DAC control register on a per channel basis. The output range is selected, and the dc-to-dc converter block is enabled (DC\_DC bit). Other control bits can be configured at this point. Set the INT\_ENABLE bit; however, the output enable bit (OUTEN) should not be set.
4. Write the required code to the DAC data register. This implements a full DAC calibration internally. Allow at least 200  $\mu$ s before Step 5 for reduced output glitch.
5. Write to the DAC control register again to enable the output (set the OUTEN bit).

A flowchart of this sequence is shown in Figure 7.

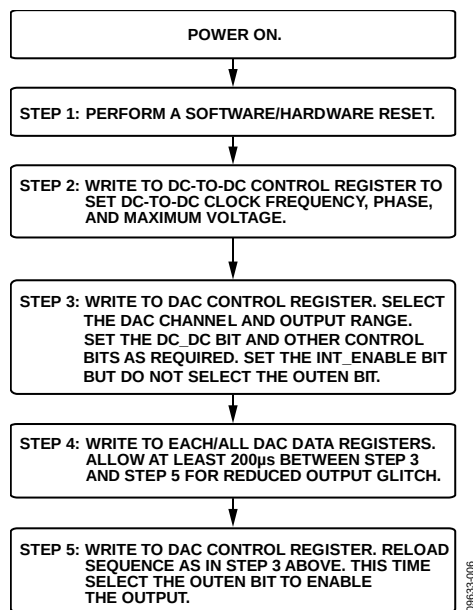


Figure 7. Programming Sequence for Enabling the Output Correctly

## CHANGING AND REPROGRAMMING THE RANGE

When changing between ranges, the same sequence as described in the Enabling the Output Correctly section should be used. It is recommended to set the range to its zero point (can be midscale or zero scale) prior to disabling the output. Because the dc-to-dc converter switching frequency, maximum voltage, and phase have already been selected, there is no need to reprogram these. A flowchart of this sequence is shown in Figure 8.

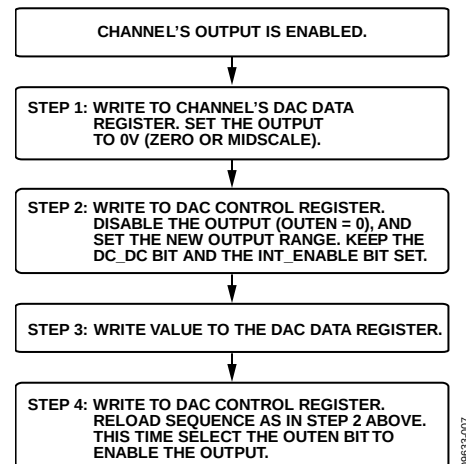


Figure 8. Steps for Changing the Output Range

## CLEAR COMMAND

To clear an output, each relevant channel must have its clear code set in the relevant data register (default of 0x0000) and be enabled for clear operation via the DAC control registers. After these are set, assert the CLEAR pin to clear the selected channels.



## CONTROL OF DIGITAL PINS

The **RESET**, **LDAC**, **POC**, and **ALERT** pins can all be controlled by clicking the relevant boxes shown in Figure 9. The **FAULT** and **ALERT** boxes display the status of the **ALERT** and **FAULT** pins. The **FAULT** and **ALERT** pins of the device are polled by the evaluation software every ~100 ms. The **FAULT** pin is also connected to the reference LED, D1, on the evaluations board, and **ALERT** is connected to the orange LED, D14.

## WRITING TO DATA REGISTERS

This function allows you to write to all the data registers. Select the register to write to from the pull-down menu, enter the 16-bit data-word to be written (in hexadecimal) and click **WRITE** to load data to the register. Note that the gain and offset registers do not update until the DAC has been written to.

## READING FROM REGISTERS

This function allows you to read from all the data registers, control registers, and the status register. Select the register to read from the pull-down menu and click **READ**. The 16 bits of LSB data appear in the number box in hexadecimal format.

## WRITING TO THE DAC CONTROL REGISTERS

This function allows you to write to and configure the DAC control register for a selected channel. Select the required DAC channel to be configured from the pull-down menu. After configuring the settings you require, click **WRITE** to write to the device. The LSB data written to the selected channel's DAC control register is shown in the register display at the top right of Figure 12.

Table 9. DAC Control Register Functions

| Option       | Description                                                                                                                                                                 |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EN Internal  | Powers up internal amplifiers. This should be done when enabling the output.                                                                                                |
| EN Clear     | Selects if the channel clears when the CLEAR pin is activated.                                                                                                              |
| EN Output    | Enables/disables the selected output channel.                                                                                                                               |
| Rset         | Selects whether internal or external sense resistor is used when using a current range.                                                                                     |
| EN DC-DC     | Powers up/down the dc-to-dc converter on a selected channel. To correctly power down the dc-to-dc converter, <b>EN Output</b> and <b>EN Internal</b> must also be disabled. |
| Over-Range   | Enables/disables 20% overrange. This is available on $V_{OUT}$ ranges only.                                                                                                 |
| Output Range | Selects the output range for the specified channel.                                                                                                                         |

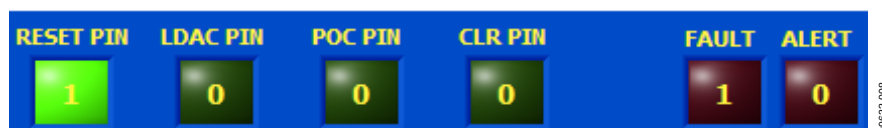


Figure 9. Digital Pin Controls and Indicators in the Evaluation Software



Figure 10. Write to Data Register in the Evaluation Software



Figure 11. Read from Register in the Evaluation Software



Figure 12. Write to the DAC Control Registers in the Evaluation Software

### WRITING TO THE DC-TO-DC CONTROL REGISTER

This function allows you to write to and configure the dc-to-dc control register. Select the required clamp voltage, switching frequency, and phase from the pull-down menu and click **WRITE** to write the selected data to the device. On the evaluation board, the dc-to-dc converter perform best at a 410 kHz switching frequency (see the DC-to-DC Boost section). See the appropriate data sheet for information on the DC-DC Comp bit. If selecting an external compensation resistor, this can be placed at R12, R13, R14, and R15.

### WRITING TO THE MAIN CONTROL REGISTER

This function allows you to write to and configure the main control register. After configuring the settings you require, click **WRITE** to write to the device.

### WRITING TO THE SLEW RATE CONTROL REGISTER

The slew rate control register can be accessed from the tab at the bottom of the evaluation software window (see Figure 15). The slew rate control functions (**Slew Rate Clock** and **Slew Rate Step**) allow you to configure the slew rate on a per-channel basis. After configuring the setting you require, click **WRITE** to write to the device.

Table 10. Slew Rate Register Functions

| Option          | Description                                   |
|-----------------|-----------------------------------------------|
| SE              | Enable/disable the slew rate control feature. |
| Slew Rate Clock | Set the slew clock rate.                      |
| Slew Rate Step  | Set the step size when slewing.               |



Figure 13. Write to the DC-to-DC Control Register in the Evaluation Software

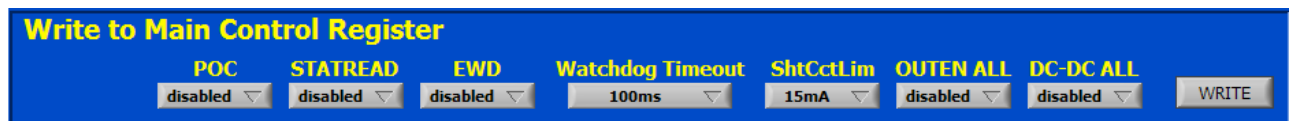


Figure 14. Write to the Main Control Register in the Evaluation Software

Table 11. Main Control Register Functions

| Option           | Description                                                                                                                                                                                                                                                                                |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POC              | Determines the state of the $V_{OUT}$ channel when the voltage output channel is disabled during normal operation.<br>Disabled: disabled $V_{OUT}$ channels goes to the function set by the POC pin.<br>Enabled: disabled $V_{OUT}$ channels goes to the opposite function of the POC pin. |
| STATREAD         | Enable/disable status readback during a write (see the Status Readback section for details about using this feature).                                                                                                                                                                      |
| EWD              | Enable/disable the watchdog timer (see the Writing to the Main Control Register section for details about using this feature).                                                                                                                                                             |
| Watchdog Timeout | Select timeout period for watchdog timer (using 100 ms or 200 ms with the evaluation software recommended).                                                                                                                                                                                |
| ShtCctLim        | Selects short-circuit current limit on the $V_{OUT}$ channels.                                                                                                                                                                                                                             |
| OUTEN ALL        | Enables the output on all four DACs simultaneously.<br>Do not use <b>OUTEN ALL</b> when enabling channels via the DAC control registers.                                                                                                                                                   |
| DC-DC ALL        | When set, powers up the dc-to-dc converter on all four channels simultaneously.<br>To power down the dc-to-dc converters, all channels outputs must first be disabled.<br>Do not use the <b>DC-DC ALL</b> option when enabling the dc-to-dc converters via the DAC control registers.      |

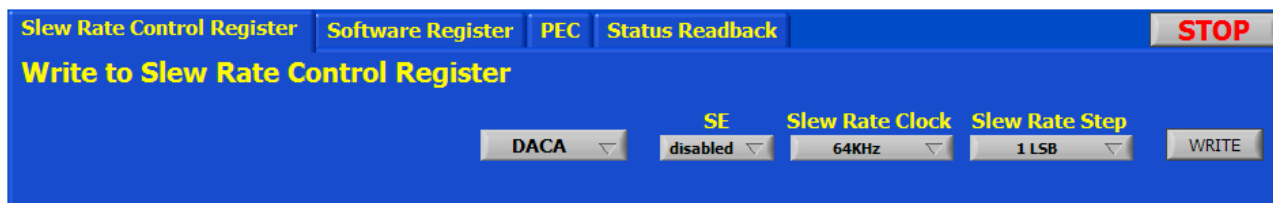


Figure 15. Write to the Slew Rate Control Register and Other Functions in the Evaluation Software



## SOFTWARE REGISTER

Click the **Software Register** tab shown in Figure 15 to access this feature. From this tab, you can set the user toggle bit that is contained in the status register and perform a software reset.

This tab contains a feature for using the watchdog timer. By entering a value for **Delay (ms)**, the evaluation software attempts to send the SPI code required to the software register (0x195) in approximately the time specified. Note that, because the latency of the USB connection is not strictly defined, this time delay is only a rough estimate but can be far exceeded. It is recommended to use the 100 ms or 200 ms watchdog timeouts when using this feature.

This tab also contains the option to latch the ALERT pin display in the evaluation software. See the Control of Digital Pins section for more information on the ALERT pin.

## PEC

Click the **PEC** tab shown in Figure 15 to access this feature. Click the **Use PEC** button to enable the automatic PEC feature of the device: an 8-bit PEC code is appended to the end of every write sequence and is read at the end of every read sequence. The data and PEC written are displayed in this tab; if a PEC error occurs, the  $\overline{\text{FAULT}}$  pin lights up. During a read operation, the data received from the device and the PEC code received are displayed in this tab.

## STATUS READBACK

When **STATREAD** is enabled (see Figure 14), the status register is displayed in the **Status Readback** tab shown in Figure 15. Note that the status register readback on a write operation reports any errors present immediately before the current write command.

## EVALUATION BOARD SCHEMATICS AND ARTWORK

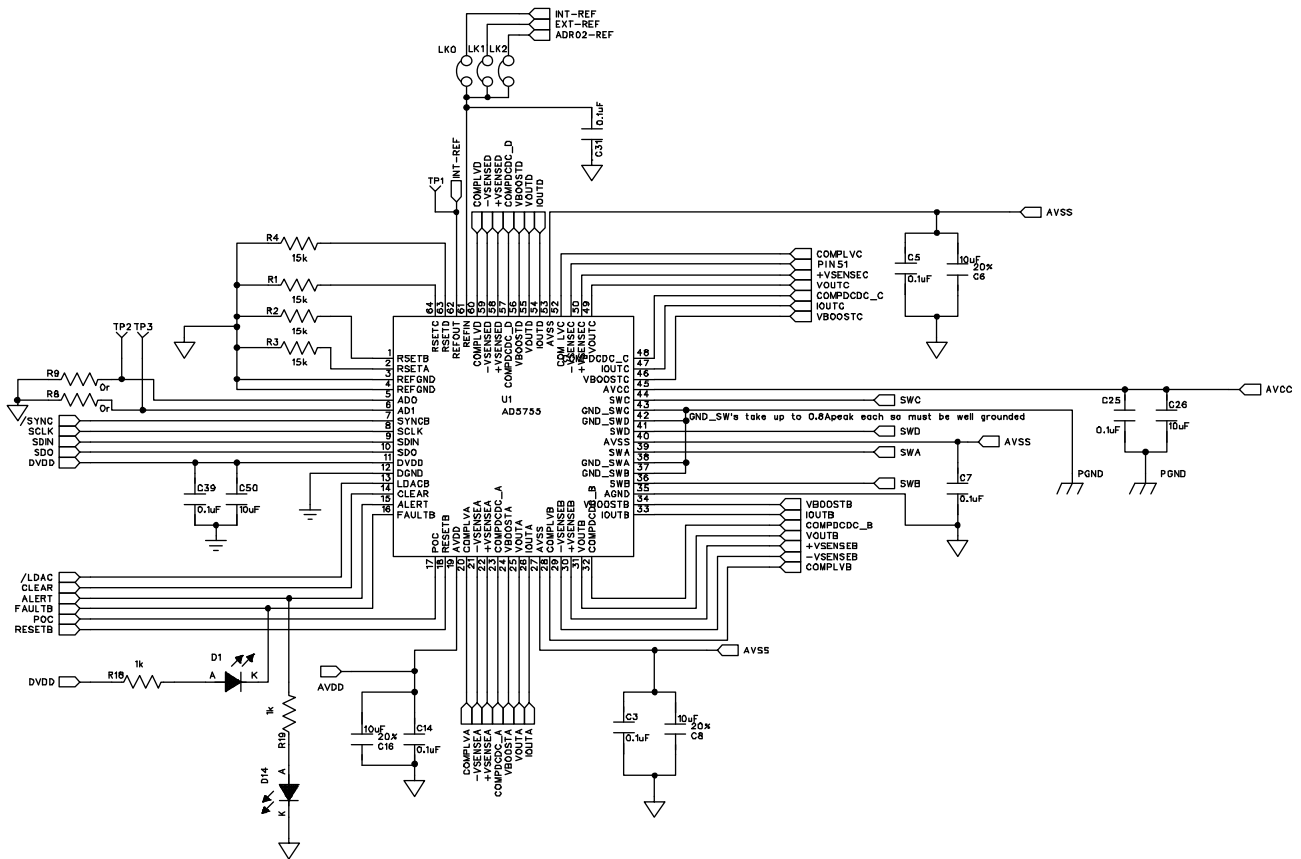


Figure 16. Main Device Circuitry

09633-015

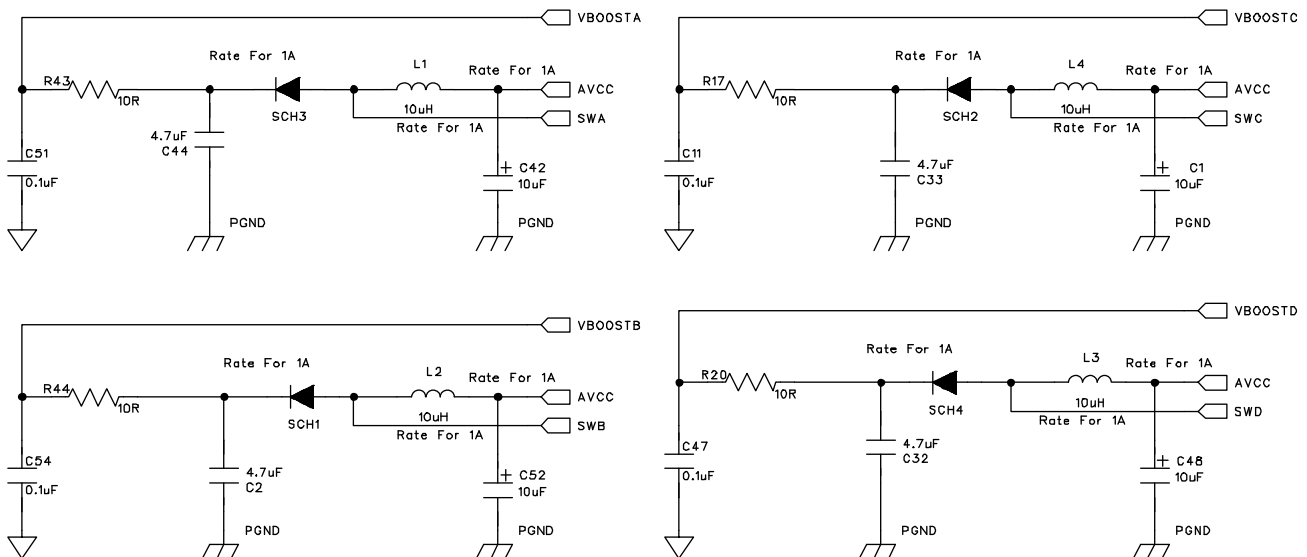


Figure 17. DC-to-DC Circuitry

09633-016

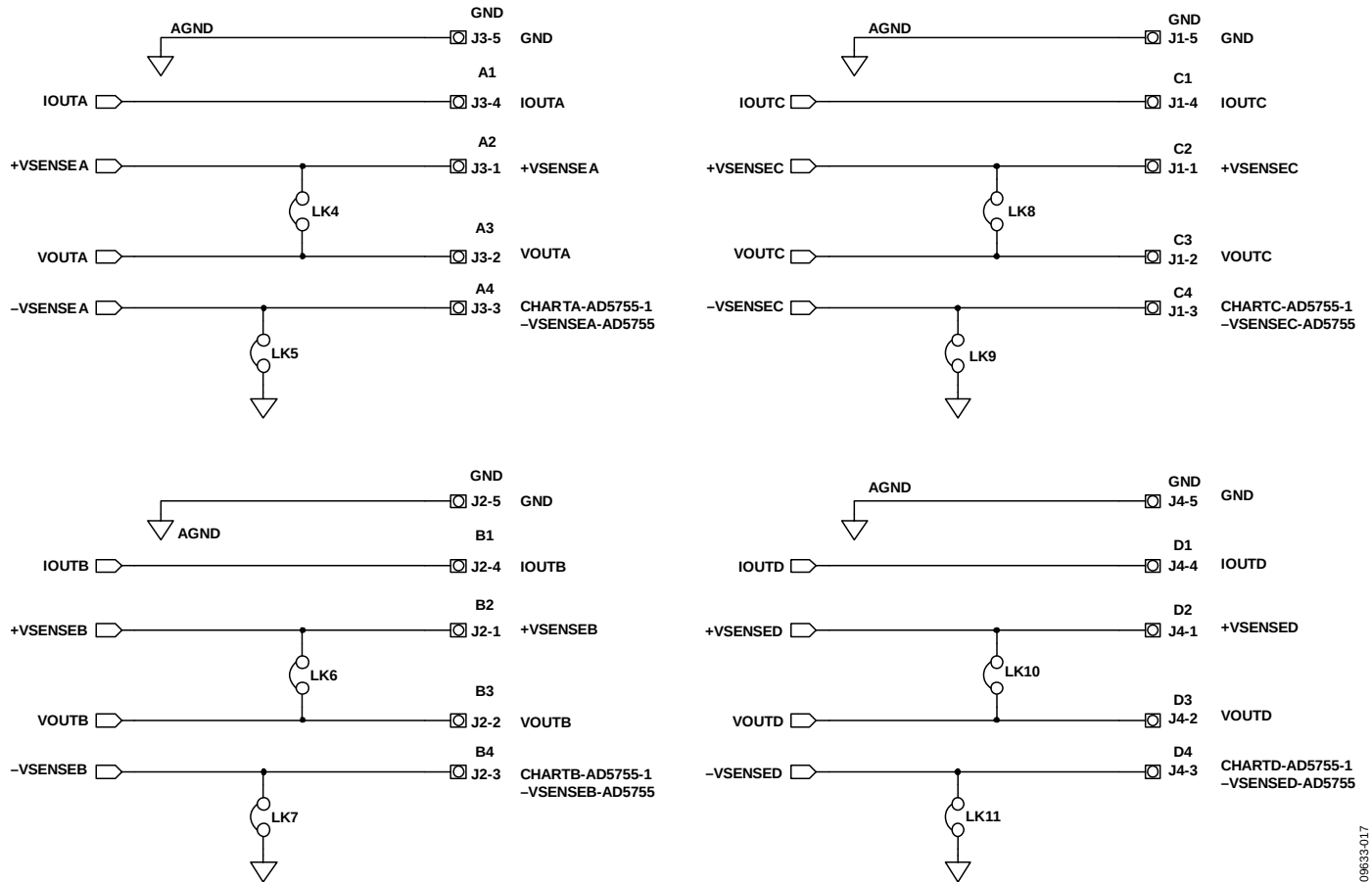


Figure 18. Output (Terminal Blocks) Circuitry

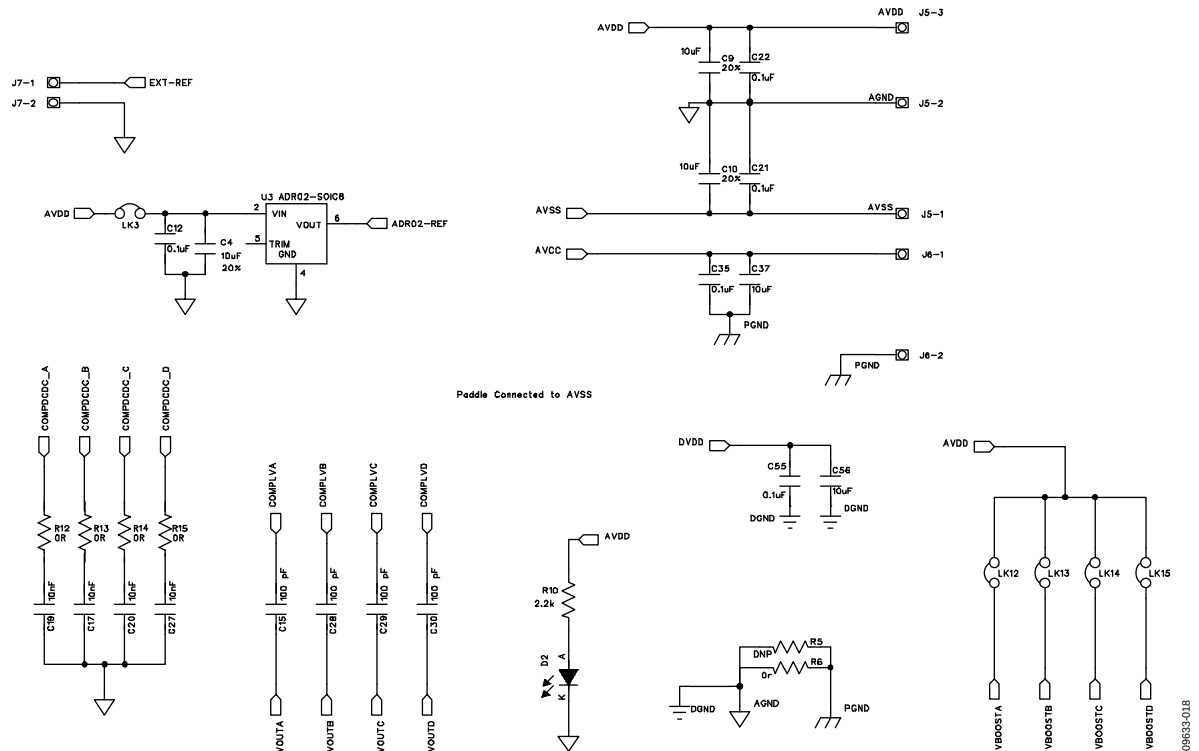


Figure 19. Supply Connections and Circuitry

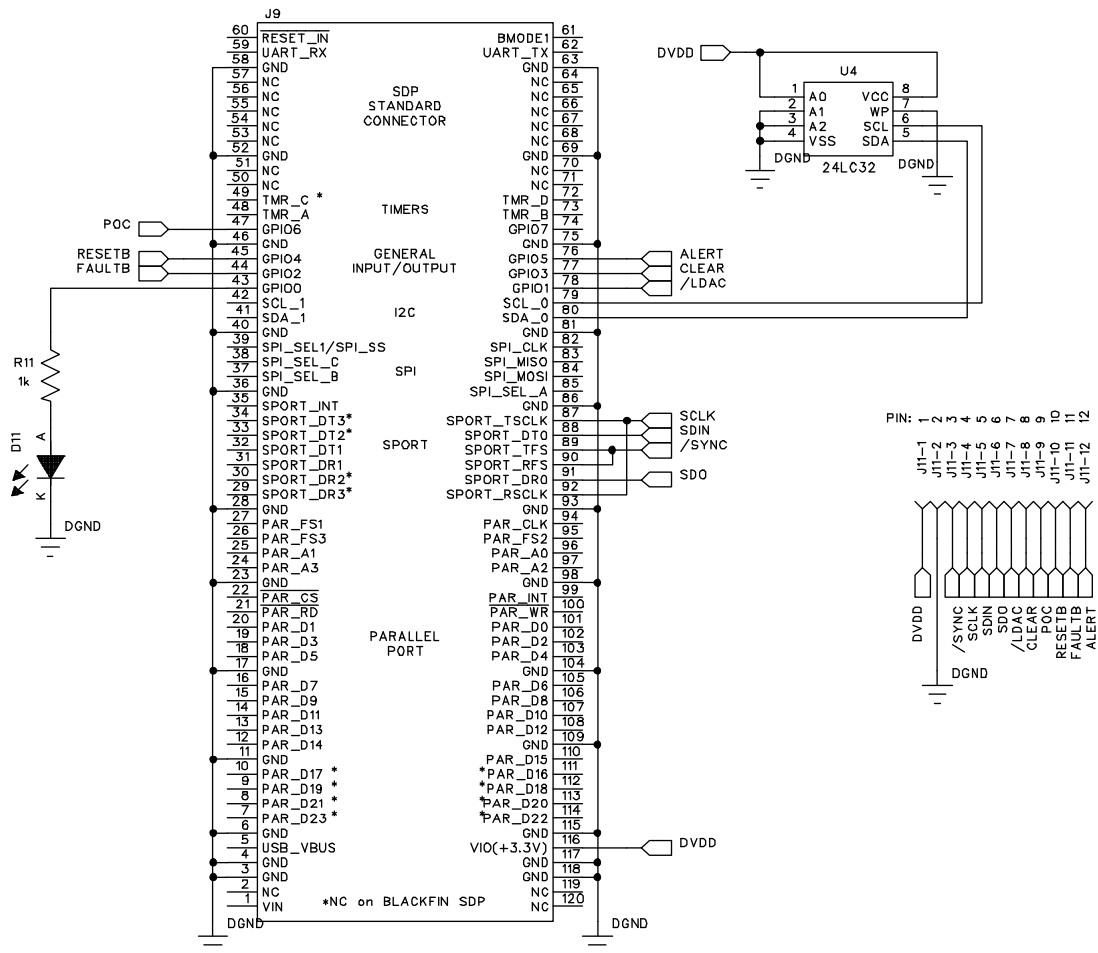
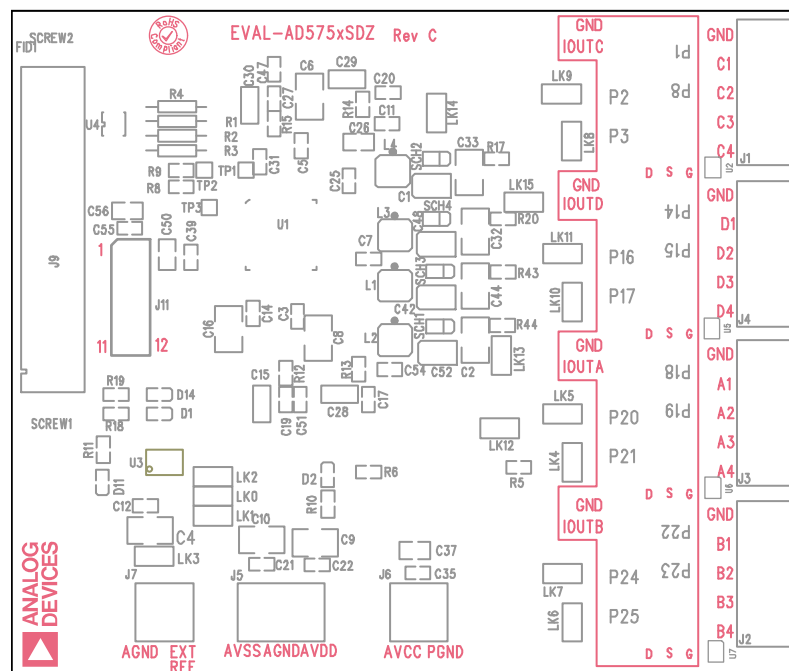
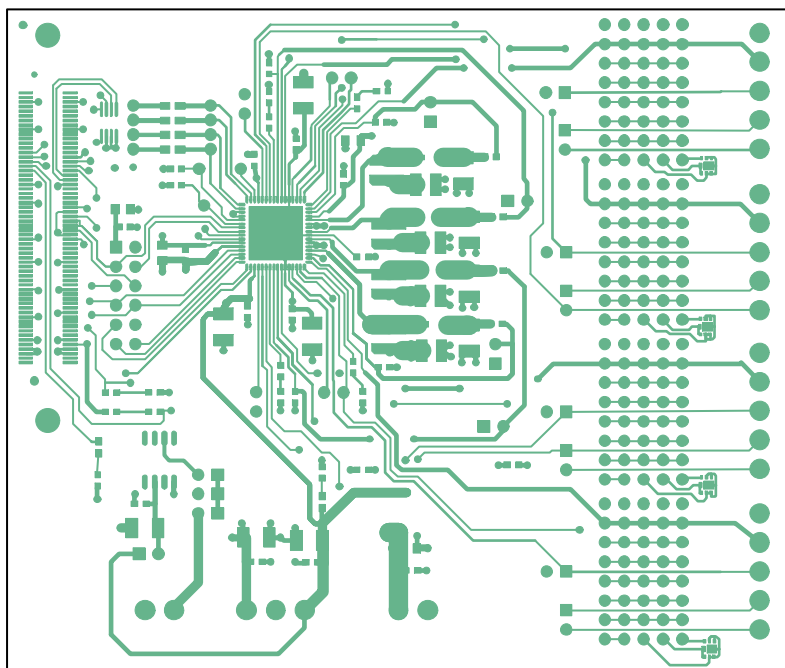


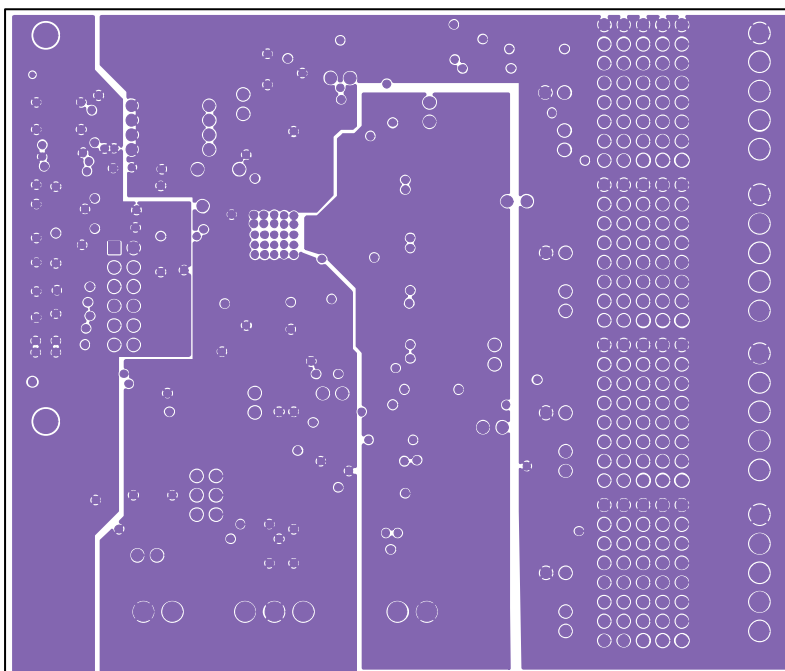
Figure 20. SDP Board Connector





09K33-021

Figure 22. Top PCB Layer



09K33-022

Figure 23. Inner First PCB Layer

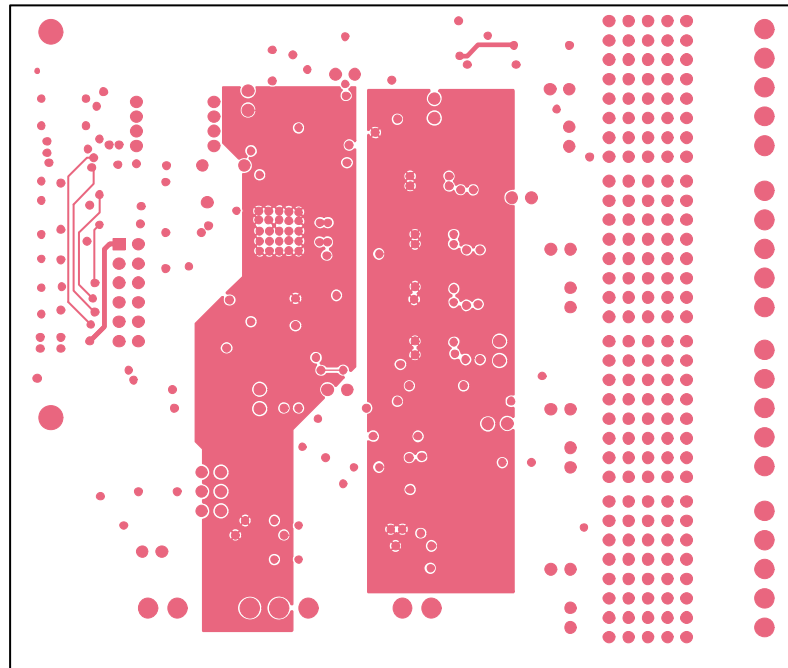


Figure 24. Inner Second PCB Layer

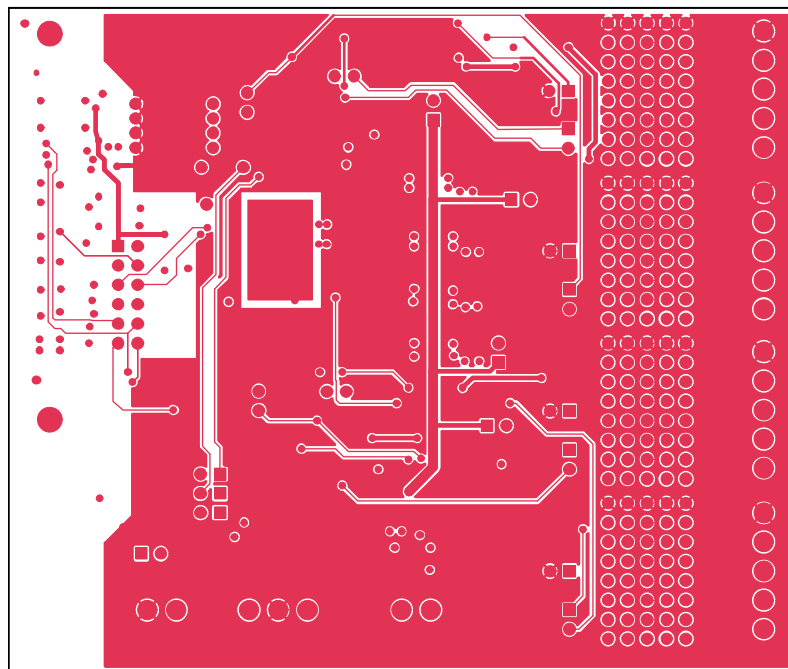


Figure 25. Bottom PCB Layer



## ORDERING INFORMATION

## BILL OF MATERIALS

Table 12.

| Qty | Reference Designator                                                            | Part Description                                            | Part Number            | Stock Code                    |
|-----|---------------------------------------------------------------------------------|-------------------------------------------------------------|------------------------|-------------------------------|
| 4   | C1, C42, C48, C52                                                               | 10 $\mu$ F, 10 V, SMD tantalum capacitor, Case A            | TCJA106M010R0300       | FEC 1135234                   |
| 4   | C2, C32, C33, C44                                                               | 4.7 $\mu$ F, 50 V, X7R ceramic capacitor, 1210              | GRM32ER71H475KA88<br>L | FEC 1404215                   |
| 5   | C4, C6, C8, C10, C16                                                            | 10 $\mu$ F, 50 V, X5R ceramic capacitor, 1210               | UMK325BJ106MM-T        | FEC 1683595                   |
| 17  | C3, C5, C7, C9, C11, C12, C14, C21, C22, C25, C31, C35, C39, C47, C51, C54, C55 | 0.1 $\mu$ F, 50 V, X7R ceramic capacitor, 0603              | C0603C104K5RAC         | FEC 1288255                   |
| 4   | C15, C28 to C30                                                                 | 100 pF, 100 V, C0G ceramic capacitor, radial                | B37979G1101J           | FEC 1200381                   |
| 4   | C17, C19, C20, C27                                                              | 10 nF, 50 V, X7R ceramic capacitor, 0603                    | B37931K5103K60         | FEC 753622                    |
| 4   | C26, C37, C50, C56                                                              | 10 $\mu$ F, 16 V, X5R ceramic capacitor, 0805               | GRM21BR61C106KE15L     | FEC 1762635                   |
| 1   | D1                                                                              | Red, SMD LED, 0603                                          | SML-D12U8WT86          | FEC 1685094                   |
| 3   | D2, D11, D14                                                                    | Green, SMD LED, 0603                                        | SML-512MWT86R          | FEC 1685076                   |
| 4   | J1 to J4                                                                        | 5-pin terminal block (3.81 mm pitch)                        | 3704609                | FEC 3704609                   |
| 1   | J5                                                                              | 3-pin terminal block (3.81 mm pitch)                        | 1727023                | FEC 3704580                   |
| 2   | J6, J7                                                                          | 2-pin terminal block (3.81 mm pitch)                        | 1727010                | FEC 3704579                   |
| 1   | J9                                                                              | 120-way connector, 0.6 mm pitch                             | FX8-120S-SV(21)        | FEC 1324660                   |
| 1   | J11                                                                             | 12-pin (2 $\times$ 6) 0.1" pitch header                     | M20-9980646            | FEC 1022238                   |
| 4   | L1 to L4                                                                        | Inductor                                                    | XAL4040-103            | Coilcraft XAL4040-103         |
| 16  | LK0 to L15                                                                      | 2-pin (0.1" pitch) header and jumper socket                 | M20-9990246            | FEC 1022247 and<br>FEC 150411 |
| 4   | R1, R2, R3, R4                                                                  | 15 k $\Omega$ , low drift, SMD resistor, 0805               | PCF0805-13-15K-B-T1    | FEC 1108896                   |
| 1   | R5                                                                              | 0 $\Omega$ , SMD resistor, 0603                             | CRCW06030000Z0EA       | DNP                           |
| 7   | R6, R8, R9, R12, R13, R14, R15                                                  | 0 $\Omega$ , SMD resistor, 0603                             | CRCW06030000Z0EA       | FEC 1469739                   |
| 1   | R10                                                                             | 2.2 k $\Omega$ , SMD resistor, 0603                         | CRCW06032K20JNEA       | FEC 1652868                   |
| 3   | R11, R18, R19                                                                   | 1 k $\Omega$ , SMD resistor, 0603                           | CRCW06031K00JNEA       | FEC 1652851                   |
| 4   | R17, R20, R43, R44                                                              | 10 $\Omega$ , SMD resistor, 0603                            | CRCW060310R0FKEA       | FEC 1469751                   |
| 4   | SCH1 to SCH4                                                                    | 1 A, 30 V, Schottky diode, SOD323                           | PMEG3010BEA            | FEC 8737991                   |
| 3   | TP1 to TP3                                                                      | Test point                                                  |                        | DNP                           |
| 1   | U1                                                                              | Quad 16-bit DAC with dynamic power control                  | AD5755-1               | AD5755-1ACPZ                  |
| 1   | U3                                                                              | 5 V precision reference, 8-lead SOIC                        | ADR02BRZ               | ADR02BRZ                      |
| 1   | U4                                                                              | 32 kB I <sup>2</sup> C serial EEPROM, 8-lead MSOP           | 24LC32A-I/MS           | FEC 1331330                   |
| 4   | U2, U5, U6, U7                                                                  | MOSFET P-channel, 30 V. Only populate on EVAL-AD5757 boards | NTLJS4149PTAG          | N/A                           |

## RELATED LINKS

| Resource                 | Description                                                                                                                      |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">AD5755</a>   | Product Page, Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC, Dynamic Power Control                    |
| <a href="#">AD5757</a>   | Product Page, Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA Output DAC, Dynamic Power Control, HART Connectivity             |
| <a href="#">AD5755-1</a> | Product Page, Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC, Dynamic Power Control, HART Connectivity |
| <a href="#">ADR02</a>    | Product Page, Ultracompact, Precision 5.0 V Voltage Reference                                                                    |

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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