

# NB3W1900L

## 3.3 V 100/133 MHz Differential 1:19 HCSL-Compatible Push-Pull Clock ZDB/Fanout Buffer for PCIe®

### Description

The NB3W1900L differential clock buffers are designed to work in conjunction with a PCIe compliant source clock synthesizer to provide point-to-point clocks to multiple agents. The device is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI), PCIe Gen1/Gen2/Gen3. The NB3W1900L internal PLL is optimized to support 100 MHz and 133 MHz frequency operation. The NB3W1900L is developed with the low-power NMOS Push-Pull buffer type.

### Features

- 19 Low Power Differential Clock Output Pairs @ 0.7 V
- Output-to-Output Skew Performance: < 85 ps
- Cycle-to-Cycle Jitter (PLL Mode): < 50ps
- Low Phase Jitter (Intel QPI, PCIe Gen 2/Gen 3 Phase Jitter Compliant)
- Input-to-Output Delay Variation: < 50 ps
- Fixed-Feedback for Lowest Input-to-Output Delay Variation
- Spread Spectrum Compatible; Tracks Input Clock Spreading for Low EMI
- 100 MHz and 133 MHz PLL Mode to Meet the Next Generation PCIe Gen2 / Gen 3 and Intel QPI Phase Jitter
- Individual OE Control via SMBus
- Low-Power NMOS Push-Pull HCSL-Compatible Outputs
- PLL Configurable for PLL Mode or Bypass Mode (Fanout Operation)
- SMBus Address Configurable to Allow Multiple Buffers in a Single Control Network
- Programmable PLL Bandwidth
- Two Tri-level Addresses Selection (Nine SMBus Addresses)
- QFN 72-pin Package, 10 mm × 10 mm
- These are Pb-Free Devices



ON Semiconductor®

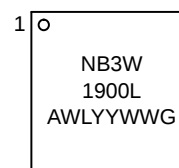
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1 72

QFN72  
MN SUFFIX  
CASE 485DK

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

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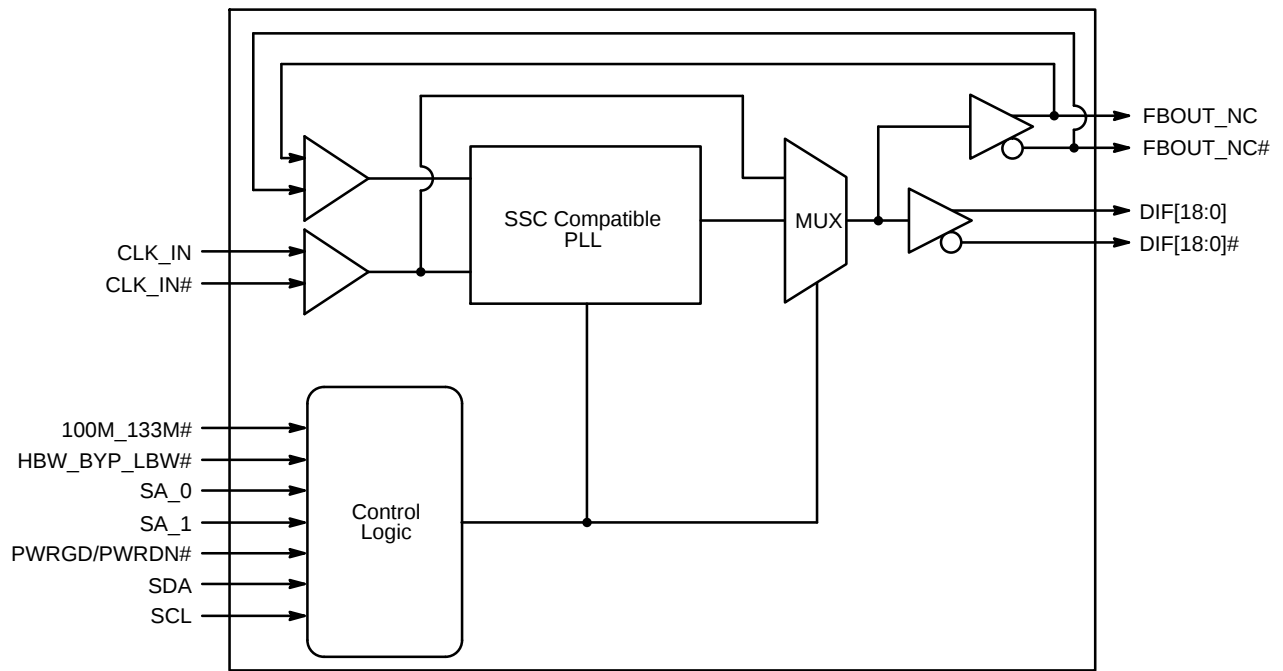


Figure 1. Simplified Block Diagram

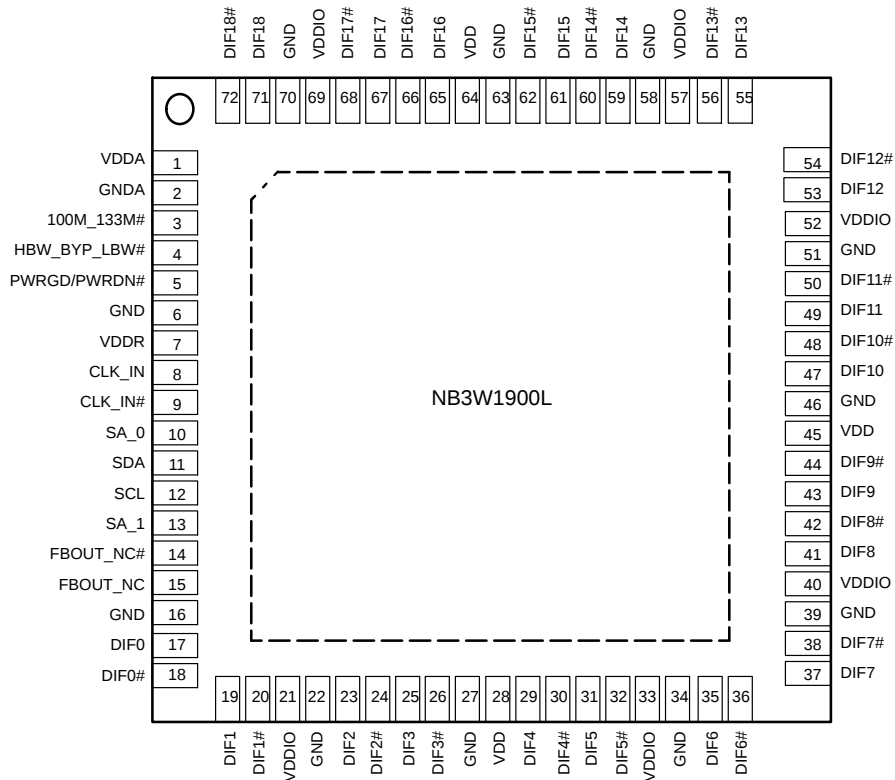


Figure 2. Pin Configuration  
(Top View)

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**Table 1. POWER DOWN PIN TABLE**

| Inputs       |                  | Control Bits | Outputs      |                      | PLL Stage |
|--------------|------------------|--------------|--------------|----------------------|-----------|
| PWRGD/PWRDN# | CLK_IN / CLK_IN# | SMBus EN Bit | DIFx / DIFx# | FBOUT_NC / FBOUT_NC# |           |
| 0            | X                | X            | Low/Low      | Low/Low              | OFF       |
| 1            | Running          | 0            | Low/Low      | Running              | ON        |
|              |                  | 1            | Running      | Running              | ON        |

**Table 2. POWER CONNECTIONS**

| Pin Number |                        |      |                                        | Description  |
|------------|------------------------|------|----------------------------------------|--------------|
| VDD        | VDDIO                  | VDDR | GND                                    |              |
|            |                        | 7    | 2                                      | Analog Input |
| 1          |                        |      | 6                                      | Analog PLL   |
| 28, 45, 64 | 21, 33, 40, 52, 57, 69 |      | 16, 22, 27, 34, 39, 46, 51, 58, 63, 70 | DIF clocks   |

**Table 3. TRI-LEVEL INPUT THRESHOLDS**

| Level | Voltage           |
|-------|-------------------|
| Low   | < 0.8 V           |
| Mid   | 1.2 < Vin < 1.8 V |
| High  | Vin > 2.2 V       |

**Table 5. PLL OPERATING MODE**

| HBW_BYP_LBW# | MODE      |
|--------------|-----------|
| Low          | PLL Lo BW |
| Mid          | Bypass    |
| High         | PLL Hi BW |

NOTE: PLL is OFF in Bypass

**Table 4. FUNCTIONALITY AT POWER-UP (PLL Mode)**

| 100M_133M# | CLK_IN | DIFx   |
|------------|--------|--------|
|            | MHz    | MHz    |
| 1          | 100.00 | CLK_IN |
| 0          | 133.33 | CLK_IN |

**Table 6. MODE TRI-LEVEL INPUT THRESHOLD**

| Level | Voltage           |
|-------|-------------------|
| Low   | < 0.8 V           |
| Mid   | 1.2 < Vin < 1.8 V |
| High  | Vin > 2.2 V       |

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**Table 7. NB3W1900L PIN DESCRIPTIONS**

| Pin Number | Pin Name     | Type | Description                                                                                                                                                                                |
|------------|--------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | VDDA         | PWR  | 3.3 V Power Supply for PLL core.                                                                                                                                                           |
| 2          | GND          | GND  | Ground for PLL core.                                                                                                                                                                       |
| 3          | 100M_133M#   | IN   | Input to select operating frequency. See functionality table for definition.                                                                                                               |
| 4          | HBW_BYP_LBW# | IN   | Tri-level input to select High BW, Bypass or low BW mode. See PLL operating mode table for definition.                                                                                     |
| 5          | PWRGD/PWRDN# | IN   | Notifies device to sample latched inputs and start up on first high assertion, or exit power down mode on subsequent assertions. Low enters power down mode.                               |
| 6          | GND          | GND  | Ground pin                                                                                                                                                                                 |
| 7          | VDDR         | PWR  | 3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.                                                        |
| 8          | CLK_IN       | IN   | 0.7 V differential true input                                                                                                                                                              |
| 9          | CLK_IN#      | IN   | 0.7 V differential complementary input                                                                                                                                                     |
| 10         | SA_0         | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SA_1 to decode 1 of 9 SMBus addresses.                                                                     |
| 11         | SDA          | I/O  | Data pin of SMBus circuitry, 5 V tolerant                                                                                                                                                  |
| 12         | SCL          | IN   | Clock pin of SMBus circuitry, 5 V tolerant                                                                                                                                                 |
| 13         | SA_1         | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SA_0 to decode 1 of 9 SMBus addresses.                                                                     |
| 14         | FBOUT_NC#    | OUT  | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 ps propagation delay. |
| 15         | FBOUT_NC     | OUT  | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 ps propagation delay.          |
| 16         | GND          | GND  | Ground pin                                                                                                                                                                                 |
| 17         | DIF0         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 18         | DIF0#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 19         | DIF1         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 20         | DIF1#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 21         | VDDIO        | PWR  | Power supply for differential outputs                                                                                                                                                      |
| 22         | GND          | GND  | Ground pin                                                                                                                                                                                 |
| 23         | DIF2         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 24         | DIF2#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 25         | DIF3         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 26         | DIF3#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 27         | GND          | GND  | Ground pin                                                                                                                                                                                 |
| 28         | VDD          | PWR  | Power supply nominal 3.3 V                                                                                                                                                                 |
| 29         | DIF4         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 30         | DIF4#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 31         | DIF5         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |
| 32         | DIF5#        | OUT  | 0.7 V differential complementary clock output                                                                                                                                              |
| 33         | VDDIO        | PWR  | Power supply for differential outputs                                                                                                                                                      |
| 34         | GND          | GND  | Ground pin                                                                                                                                                                                 |
| 35         | DIF6         | OUT  | 0.7 V differential true clock output                                                                                                                                                       |

1. All VDD, VDDR, VDDIO, VDDA and GND pins must be externally connected to a power supply for proper operation.

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**Table 7. NB3W1900L PIN DESCRIPTIONS** (continued)

| Pin Number | Pin Name    | Type    | Description                                                                                                                                                                                                                                                                                                       |
|------------|-------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 36         | DIF6#       | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 37         | DIF7        | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 38         | DIF7#       | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 39         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 40         | VDDIO       | PWR     | Power supply for differential outputs                                                                                                                                                                                                                                                                             |
| 41         | DIF8        | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 42         | DIF8#       | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 43         | DIF9        | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 44         | DIF9#       | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 45         | VDD         | PWR     | Power supply nominal 3.3 V                                                                                                                                                                                                                                                                                        |
| 46         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 47         | DIF10       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 48         | DIF10#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 49         | DIF11       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 50         | DIF11#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 51         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 52         | VDDIO       | PWR     | Power supply for differential outputs                                                                                                                                                                                                                                                                             |
| 53         | DIF12       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 54         | DIF12#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 55         | DIF13       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 56         | DIF13#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 57         | VDDIO       | PWR     | Power supply for differential outputs                                                                                                                                                                                                                                                                             |
| 58         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 59         | DIF14       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 60         | DIF14#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 61         | DIF15       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 62         | DIF15#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 63         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 64         | VDD         | PWR     | Power supply nominal 3.3 V                                                                                                                                                                                                                                                                                        |
| 65         | DIF16       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 66         | DIF16#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 67         | DIF17       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 68         | DIF17#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| 69         | VDDIO       | PWR     | Power supply for differential outputs                                                                                                                                                                                                                                                                             |
| 70         | GND         | GND     | Ground pin                                                                                                                                                                                                                                                                                                        |
| 71         | DIF18       | OUT     | 0.7 V differential true clock output                                                                                                                                                                                                                                                                              |
| 72         | DIF18#      | OUT     | 0.7 V differential complementary clock output                                                                                                                                                                                                                                                                     |
| EP         | Exposed Pad | Thermal | The Exposed Pad (EP) on the QFN-72 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

1. All VDD, VDDR, VDDIO, VDDA and GND pins must be externally connected to a power supply for proper operation.

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**Table 8. ABSOLUTE MAXIMUM RATINGS** (Note 2)

| Symbol                       | Parameter                                      | Conditions                 | Min       | Typ  | Max            | Unit |
|------------------------------|------------------------------------------------|----------------------------|-----------|------|----------------|------|
| $V_{DD} / V_{DDA} / V_{DDR}$ | 3.3 V Core Supply Voltage (Note 3)             |                            |           |      | 4.6            | V    |
| $V_{DD} / V_{DDIO}$          | 3.3 V Logic and Output Supply Voltage (Note 3) |                            |           |      | 4.6            | V    |
| $V_{IH}$                     | Input High Voltage                             | Except for SMBus Interface |           |      | $V_{DD} + 0.5$ | V    |
| $V_{IH}$                     | VIHSMB                                         | SMBus Clock and Data Pins  |           |      | 5.5            | V    |
| $V_{IL}$                     | Input Low Voltage                              |                            | GND – 0.5 |      | –              | V    |
| $T_s$                        | Storage Temperature                            |                            | –65       |      | 150            | °C   |
| $T_j$                        | Junction Temperature                           |                            |           |      | 125            | °C   |
| ESD prot.                    | ESD Protection (Human Body)                    | Human Body Model           | 2000      |      |                | V    |
| $\theta_{JA}$                | Thermal Resistance Junction-to-Ambient         | Still air                  |           | 18.1 |                | °C/W |
| $\theta_{JC}$                | Thermal Resistance Junction-to-Case            |                            |           | 5.0  |                | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Guaranteed by design and characterization, not tested in production.

3. Operation under these conditions is neither implied nor guaranteed.

**Table 9. ELECTRICAL CHARACTERISTICS – CLOCK INPUT PARAMETERS**

( $T_A = 0^\circ\text{C} - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDIO} = 1.05\text{ V to } 3.3\text{ V} \pm 5\%$ . See Test Loads for Loading Conditions) (Note 4)

| Symbol      | Parameter                                       | Conditions                                     | Min            | Typ | Max  | Unit          |
|-------------|-------------------------------------------------|------------------------------------------------|----------------|-----|------|---------------|
| $V_{IHDIF}$ | Input High Voltage – CLK_IN                     | Differential Inputs (single-ended measurement) | 600            |     | 1150 | mV            |
| $V_{ILDIF}$ | Input Low Voltage – CLK_IN                      | Differential Inputs (single-ended measurement) | $V_{SS} - 300$ |     | 300  | mV            |
| $V_{COM}$   | Input Common Mode Voltage – CLK_IN (not spec'd) | Common Mode Input Voltage                      | 300            |     | 1000 | mV            |
| $V_{SWING}$ | Input Amplitude – CLK_IN not spec'd             | Peak to Peak Value                             | 300            |     | 1450 | mV            |
| dv/dt       | Input Slew Rate – CLK_IN (Note 5)               | Measured Differentially                        | 0.4            |     | 8    | V/ns          |
| $I_{IN}$    | Input Leakage Current                           | $V_{IN} = V_{DD}$ , $V_{IN} = \text{GND}$      | –5             |     | 5    | $\mu\text{A}$ |
| $d_{tin}$   | Input Duty Cycle                                | Measurement from Differential Waveform         | 45             |     | 55   | %             |
| $J_{DIFin}$ | Input Jitter – Cycle to Cycle                   | Differential Measurement                       | 0              |     | 125  | ps            |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design and characterization, not tested in production.

5. Slew rate measured through  $\pm 75\text{ mV}$  window centered around differential zero

**Table 10. ELECTRICAL CHARACTERISTICS–INPUT/SUPPLY/COMMON OUTPUT PARAMETERS**

( $T_A = 0^\circ\text{C} - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDIO} = 1.05\text{ V to } 3.3\text{ V} \pm 5\%$ . See Test Loads for Loading Conditions) (Note 6)

| Symbol       | Parameter          | Conditions                                                            | Min       | Typ | Max            | Unit          |
|--------------|--------------------|-----------------------------------------------------------------------|-----------|-----|----------------|---------------|
| $V_{IH}$     | Input High Voltage | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2         |     | $V_{DD} + 0.3$ | V             |
| $V_{IL}$     | Input Low Voltage  | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND – 0.3 |     | 0.8            | V             |
| $I_{IN}$     | Input Current      | Single-ended inputs, $V_{IN} = \text{GND}$ , $V_{IN} = V_{DD}$        | –5        |     | 5              | $\mu\text{A}$ |
| $V_{IH\_FS}$ | Input High Voltage | (Note 7)                                                              | 0.7       |     | $V_{DD} + 0.3$ | V             |
| $V_{IL\_FS}$ | Input Low Voltage  | (Note 7)                                                              | GND – 0.3 |     | 0.35           | V             |

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**Table 10. ELECTRICAL CHARACTERISTICS—INPUT/SUPPLY/Common Output Parameters** (continued)

(T<sub>A</sub> = 0°C – 70°C; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V ±5%, V<sub>DDIO</sub> = 1.05 V to 3.3 V ±5%. See Test Loads for Loading Conditions) (Note 6)

| Symbol                | Parameter                           | Conditions                                                                                            | Min    | Typ    | Max                | Unit   |
|-----------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------|--------|--------|--------------------|--------|
| F <sub>ibyp</sub>     | Input Frequency                     | V <sub>DD</sub> = 3.3 V, Bypass mode (Note 8)                                                         | 33     |        | 150                | MHz    |
| F <sub>ipll</sub>     |                                     | V <sub>DD</sub> = 3.3 V, 100.00 MHz PLL mode (Note 8)                                                 | 99     | 100.00 | 101                | MHz    |
| F <sub>ipll</sub>     |                                     | V <sub>DD</sub> = 3.3 V, 133.33 MHz PLL mode (Note 8)                                                 | 132.33 | 133.33 | 134.33             | MHz    |
| L <sub>pin</sub>      | Pin Inductance                      |                                                                                                       |        |        | 7                  | nH     |
| C <sub>IN</sub>       | Capacitance                         | Logic Inputs, except CLK_IN                                                                           | 1.5    |        | 5                  | pF     |
| C <sub>INCLK_IN</sub> |                                     | CLK_IN differential clock inputs (Note 10)                                                            | 1.5    |        | 2.7                | pF     |
| C <sub>OUT</sub>      |                                     | Output pin capacitance                                                                                |        |        | 6                  | pF     |
| T <sub>STAB</sub>     | Clk Stabilization (Note 8)          | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock |        |        | 1                  | ms     |
| f <sub>MODIN</sub>    | Input SS Modulation Frequency       | Allowable Frequency (Triangular Modulation)                                                           | 30     |        | 33                 | kHz    |
| t <sub>LATOE#</sub>   | OE# Latency                         | DIF start after OE# assertion DIF stop after OE# de-assertion                                         | 4      |        | 12                 | clocks |
| t <sub>DRVDPD</sub>   | Tdrive_PD# (Note 9)                 | DIF output enable after PD# de-assertion                                                              |        |        | 300                | μs     |
| t <sub>F</sub>        | Tfall (Note 8)                      | Fall time of control inputs                                                                           |        |        | 5                  | ns     |
| t <sub>R</sub>        | Trise (Note 8)                      | Rise time of control inputs                                                                           |        |        | 5                  | ns     |
| V <sub>ILSMB</sub>    | SMBus Input Low Voltage             |                                                                                                       |        |        | 0.8                | V      |
| V <sub>IHSMB</sub>    | SMBus Input High Voltage            |                                                                                                       | 2.1    |        | V <sub>DDSMB</sub> | V      |
| V <sub>OLSMB</sub>    | SMBus Output Low Voltage            | @ I <sub>PULLUP</sub>                                                                                 |        |        | 0.4                | V      |
| I <sub>PULLUP</sub>   | SMBus Sink Current                  | @ V <sub>OL</sub>                                                                                     | 4      |        |                    | mA     |
| V <sub>DDSMB</sub>    | Nominal Bus Voltage                 | 3 V to 5 V ±10%                                                                                       | 2.7    |        | 5.5                | V      |
| t <sub>RSMB</sub>     | SCL/SDA Rise Time                   | (Max V <sub>IL</sub> – 0.15) to (Min V <sub>IH</sub> + 0.15)                                          |        |        | 1000               | ns     |
| t <sub>FSMB</sub>     | SCL/SDA Fall Time                   | (Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> – 0.15)                                          |        |        | 300                | ns     |
| f <sub>MAXSMB</sub>   | SMBus Operating Frequency (Note 11) | Maximum SMBus operating frequency                                                                     |        |        | 100                | kHz    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design and characterization, not tested in production.

7. 100M\_133M# Frequency Select (FS).

8. Control input must be monotonic from 20% to 80% of input swing.

9. Time from de-assertion until outputs are > 200 mV

10. CLK\_IN input

11. The differential input clock must be running for the SMBus to be active

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**Table 11. ELECTRICAL CHARACTERISTICS – DIF 0.7 V LOW POWER DIFFERENTIAL OUTPUTS**

(T<sub>A</sub> = 0°C – 70°C; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V ±5%, V<sub>DDIO</sub> = 1.05 V to 3.3 V ±5%. See Test Loads for Loading Conditions)  
(Note 12)

| Symbol                 | Parameter                         | Conditions                                                                                            | Min  | Typ | Max  | Unit |
|------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------|------|-----|------|------|
| dV/dt                  | Slew Rate (Notes 13, 14)          | Scope averaging on                                                                                    | 1    |     | 4    | V/ns |
| ΔdV/dt                 | Slew Rate Matching (Notes 13, 15) | Slew rate matching, Scope averaging on                                                                |      |     | 20   | %    |
| V <sub>High</sub>      | Voltage High                      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  |     | 850  | mV   |
| V <sub>Low</sub>       | Voltage Low                       |                                                                                                       | –150 |     | 150  |      |
| V <sub>max</sub>       | Max Voltage                       | Measurement on single ended signal using Absolute value. (Scope averaging off)                        |      |     | 1150 | mV   |
| V <sub>min</sub>       | Min Voltage                       |                                                                                                       | –300 |     |      |      |
| V <sub>swing</sub>     | Vswing (Note 13)                  | Scope averaging off                                                                                   | 300  |     |      | mV   |
| V <sub>cross_abs</sub> | Crossing Voltage (abs) (Note 16)  | Scope averaging off                                                                                   | 250  |     | 550  | mV   |
| ΔV <sub>cross</sub>    | Crossing Voltage (var) (Note 17)  | Scope averaging off                                                                                   |      |     | 140  | mV   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. Guaranteed by design and characterization, not tested in production. C<sub>L</sub> = 2 pF with R<sub>S</sub> = 33 Ω for Z<sub>o</sub> = 50 Ω (100 Ω differential trace impedance).

13. Measured from differential waveform

14. Slew rate is measured through the V<sub>swing</sub> voltage range centered around differential 0 V. This results in a ±150 mV window around differential 0 V.

15. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75 mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

16. V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

17. The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting ΔV<sub>cross</sub> to be smaller than V<sub>cross</sub> absolute.

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**Table 12. ELECTRICAL CHARACTERISTICS – CURRENT CONSUMPTION**

(T<sub>A</sub> = 0°C – 70°C; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V ±5%, V<sub>DDIO</sub> = 1.05 V to 3.3 V ±5%. See Test Loads for Loading Conditions) (Note 18)

| Symbol                  | Parameter                   | Conditions                                                             | Min | Typ | Max | Unit |
|-------------------------|-----------------------------|------------------------------------------------------------------------|-----|-----|-----|------|
| I <sub>DDVDD</sub>      | Operating Supply Current    | All outputs @ 100.00 MHz, C <sub>L</sub> = 2 pF; Z <sub>o</sub> = 85 Ω |     |     | 50  | mA   |
| I <sub>DDVDDA/R</sub>   |                             | All outputs @ 100.00 MHz, C <sub>L</sub> = 2 pF; Z <sub>o</sub> = 85 Ω |     |     | 30  | mA   |
| I <sub>DDVDDIO</sub>    |                             | All outputs @ 100.00 MHz, C <sub>L</sub> = 2 pF; Z <sub>o</sub> = 85 Ω |     |     | 200 | mA   |
| I <sub>DDVDDPD</sub>    | Powerdown Current (Note 19) | All differential pairs low/low                                         |     |     | 4   | mA   |
| I <sub>DDVDDA/RPD</sub> |                             | All differential pairs low/low                                         |     |     | 5   | mA   |
| I <sub>DDVDDIOPD</sub>  |                             | All differential pairs low/low                                         |     |     | 0.2 | mA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

18. Guaranteed by design and characterization, not tested in production.

19. With input clock running. Stopping the input clock will result in lower numbers.

**Table 13. ELECTRICAL CHARACTERISTICS – SKEW AND DIFFERENTIAL JITTER PARAMETERS**

(T<sub>A</sub> = 0°C – 70°C; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V ±5%, V<sub>DDIO</sub> = 1.05 to 3.3 V ±5%. See Test Loads for Loading Conditions)

| Symbol                 | Parameter                                         | Conditions                                                                                      | Min  | Typ | Max | Unit     |
|------------------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------|------|-----|-----|----------|
| t <sub>SPO_PLL</sub>   | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 23, 24 and 27) | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3 V                                    | -100 |     | 100 | ps       |
| t <sub>PD_BYP</sub>    | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 22, 24 and 27) | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3 V                                 | 2.5  |     | 4.5 | ns       |
| t <sub>DSPO_PLL</sub>  | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 22, 24 and 27) | Input-to-Output Skew Variation in PLL mode across voltage and temperature                       |      |     | 100 | ps       |
| t <sub>DSPO_BYP</sub>  | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 22, 24 and 27) | Input-to-Output Skew Variation in Bypass mode across voltage and temperature                    | -250 |     | 250 | ps       |
| t <sub>DTE</sub>       | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 22, 24 and 27) | Random Differential Tracking error between two NB3W1900L devices in Hi BW Mode                  |      |     | 5   | ps (rms) |
| t <sub>DSSTE</sub>     | CLK_IN, DIF[x:0]<br>(Notes 20, 21, 22, 24 and 27) | Random Differential Spread Spectrum Tracking error between two NB3W1900L devices in Hi BW Mode. |      |     | 75  | ps       |
| t <sub>SKEW_ALL</sub>  | DIF[x:0]<br>(Notes 20, 21, 22 and 27)             | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)                        |      |     | 85  | ps       |
| j <sub>peak-hibw</sub> | PLL Jitter Peaking<br>(Notes 26 and 27)           | HBW_BYP_LBW# = 1                                                                                | 0    |     | 2.5 | dB       |
| j <sub>peak-lobw</sub> | PLL Jitter Peaking<br>(Notes 26 and 27)           | HBW_BYP_LBW# = 0                                                                                | 0    |     | 2   | dB       |
| pll <sub>HIBW</sub>    | PLL Bandwidth (Notes 27 and 28)                   | HBW_BYP_LBW# = 1                                                                                | 2    |     | 4   | MHz      |
| pll <sub>LOBW</sub>    | PLL Bandwidth (Notes 27 and 28)                   | HBW_BYP_LBW# = 0                                                                                | 0.7  |     | 1.4 | MHz      |
| t <sub>DC</sub>        | Duty Cycle (Note 20)                              | Measured differentially, PLL Mode                                                               | 45   | 50  | 55  | %        |
| t <sub>DCD</sub>       | Duty Cycle Distortion<br>(Notes 20 and 29)        | Measured differentially, Bypass Mode @ 100.00 MHz                                               | -2   | 0   | 2   | %        |
| t <sub>jcy-cyc</sub>   | Jitter, Cycle-to-Cycle<br>(Notes 20 and 30)       | PLL mode                                                                                        |      |     | 50  | ps       |
|                        |                                                   | Additive Jitter in Bypass Mode                                                                  |      |     | 50  | ps       |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

20. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

21. Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

22. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

23. This parameter is deterministic for a given device

24. Measured with scope averaging on to find mean value.

25. t is the period of the input clock

26. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

27. Guaranteed by design and characterization, not tested in production.

28. Measured at 3 db down or half power point.

29. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

30. Measured from differential waveform

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**Table 14. ELECTRICAL CHARACTERISTICS – PHASE JITTER PARAMETERS**

(T<sub>A</sub> = 0°C – 70°C; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V ±5%, V<sub>DDIO</sub> = 1.05 V to 3.3 V ±5%. See Test Loads for Loading Conditions) (Note 31)

| Symbol                  | Parameter                          | Conditions                                                                            | Min | Typ | Max | Unit     |
|-------------------------|------------------------------------|---------------------------------------------------------------------------------------|-----|-----|-----|----------|
| t <sub>jphPCleG1</sub>  | Phase Jitter, PLL Mode             | PCle Gen 1 (Notes 32 and 33)                                                          |     |     | 86  | ps (p–p) |
| t <sub>jphPCleG2</sub>  |                                    | PCle Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 32)                                     |     |     | 3   | ps (rms) |
|                         |                                    | PCle Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 32)                         |     |     | 3.1 | ps (rms) |
| t <sub>jphPCleG3</sub>  |                                    | PCle Gen 3<br>(PLL BW of 2–4 MHz, CDR = 10 MHz)<br>(Notes 32, 33 and 34)              |     |     | 1   | ps (rms) |
| t <sub>jphQPI_SMI</sub> |                                    | QPI & SMI<br>(100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI)<br>(Note 35)         |     |     | 0.5 | ps (rms) |
|                         |                                    | QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 35)                                      |     |     | 0.3 | ps (rms) |
|                         |                                    | QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 35)                                      |     |     | 0.2 | ps (rms) |
| t <sub>jphPCleG1</sub>  | Additive Phase Jitter, Bypass Mode | PCle Gen 1 (Notes 32 and 33)                                                          |     |     | 10  | ps (p–p) |
| t <sub>jphPCleG2</sub>  |                                    | PCle Gen 2 Lo Band 10 kHz < f < 1.5 MHz<br>(Notes 32 and 36)                          |     |     | 0.3 | ps (rms) |
|                         |                                    | PCle Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz)<br>(Notes 32 and 36)              |     |     | 0.7 | ps (rms) |
| t <sub>jphPCleG3</sub>  |                                    | PCle Gen 3<br>(PLL BW of 2–4 MHz, CDR = 10 MHz)<br>(Notes 32, 34 and 36)              |     |     | 0.3 | ps (rms) |
| t <sub>jphQPI_SMI</sub> |                                    | QPI & SMI<br>(100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI)<br>(Notes 35 and 36) |     |     | 0.3 | ps (rms) |
|                         |                                    | QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI)<br>(Notes 35 and 36)                           |     |     | 0.1 | ps (rms) |
|                         |                                    | QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI)<br>(Notes 35 and 36)                           |     |     | 0.1 | ps (rms) |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

31. Applies to all outputs.

32. See <http://www.pcisig.com> for complete specs

33. Sample size of at least 100k cycles. This figures extrapolates to 108 ps pk-pk @ 1M cycles for a BER of 1–12.

34. Subject to final ratification by PCI SIG.

35. Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

36. For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)<sup>2</sup> = (total jitter)<sup>2</sup> – (input jitter)<sup>2</sup>

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**Table 15. CLOCK PERIODS-DIFFERENTIAL OUTPUTS WITH SPREAD SPECTRUM DISABLED**

| SSC OFF | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                         | Unit | Notes      |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|-------------------------|------|------------|
|         |                  | 1 Clock                | 1 $\mu$ s                   | 0.1 s                       | 0.1s                 | 0.1s                        | 1 $\mu$ s                   | 1 Clock                 |      |            |
|         |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter Abs Per Max |      |            |
| DIF     | 1 00.00          | 9.94900                |                             | 9.99900                     | 10 .0000 0           | 1 0.001 00                  |                             | 10.05100                | ns   | 37, 38, 39 |
|         | 1 33.33          | 7.44925                |                             | 7.49925                     | 7.50000              | 7.50075                     |                             | 7.55 075                | ns   | 37, 38, 40 |

37. Guaranteed by design and characterization, not tested in production.

38. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements ( $\pm 100$  ppm). The NB3W1900L it self does not contribute to ppm error.

39. Driven by SRC out put of main clock, 100.00 MHz PLL Mode or Bypass mode.

40. Driven by CPU out put of main clock, 133.33 MHz PLL Mode or Bypass mode.

**Table 16. CLOCK PERIODS-DIFFERENTIAL OUTPUTS WITH SPREAD SPECTRUM ENABLED**

| SSC ON | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Unit | Notes      |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|------|------------|
|        |                  | 1 Clock                | 1 $\mu$ s                   | 0.1s                        | 0.1s                 | 0.1s                        | 1 $\mu$ s                   | 1 Clock                |      |            |
|        |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |      |            |
| DIF    | 99.75            | 9.94906                | 9. 99906                    | 10.02406                    | 10.02506             | 10.02607                    | 10.05107                    | 10.10107               | ns   | 41, 42, 43 |
|        | 133.00           | 7.44930                | 7. 49930                    | 7.51805                     | 7.51880              | 7.51955                     | 7.53830                     | 7.58830                | ns   | 41, 42, 44 |

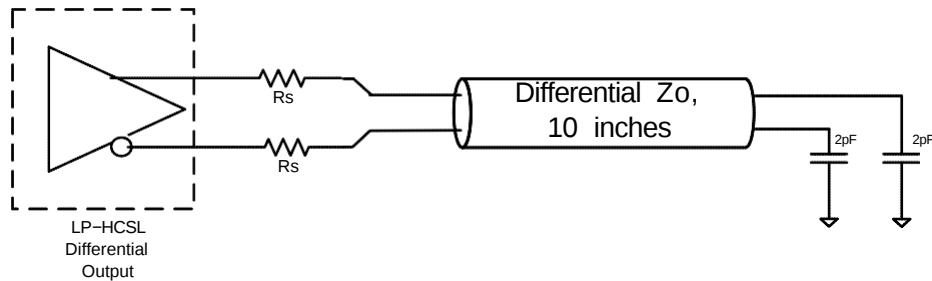
41. Guaranteed by design and characterization, not tested in production.

42. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/ CK410B+ accuracy requirements ( $\pm 100$  ppm). The NB3W1900L it self does not contribute to ppm error.

43. Driven by SRC out put of main clock, 100.00 MHz PLL Mode or Bypass mode.

44. Driven by CPU out put of main clock, 133.33 MHz PLL Mode or Bypass mode.

## TEST LOADS



**Figure 3. NB3W1900L Differential Test Loads**

**Table 17. DIFFERENTIAL OUTPUT TERMINATIONS**

| DIF $Z_o$ ( $\Omega$ ) | $R_s$ ( $\Omega$ ) |
|------------------------|--------------------|
| 100                    | 33                 |
| 85                     | 27                 |

## PWRGD/PWRDN#

PWRGD/PWRDN# is a dual function pin. PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the NB3W1900L to sample initial configurations such as frequency select condition and SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low **prior to shutting off the input clock or power** to ensure all clocks shut down in a glitch free manner. When PWRDN# is

asserted low by two consecutive rising edges of DIF#, all differential outputs are held tri-stated on the next DIF# high to low transition. The assertion and de-assertion of PWRDN# is absolutely asynchronous.

**WARNING:** Disabling of the CLK\_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches, excessive frequency shifting, etc.

**Table 18. PWRGD/PWRDN# FUNCTIONALITY**

| PWRGD/PWRDN# | DIF       | DIF#      |
|--------------|-----------|-----------|
| 0            | Tri-state | Tri-state |
| 1            | Running   | Running   |

## Buffer Power-Up State Machine

Table 19. BUFFER POWER-UP STATE MACHINE

| State | Description                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | 3.3 V Buffer power off                                                                                                                  |
| 1     | After 3.3 V supply is detected to rise above 3.135 V, the buffer enters State 1 and initiates a 0.1 ms–0.3 ms delay.                    |
| 2     | Buffer waits for a valid clock on the CLK input and PWRDN# de-assertion (or PWRGD assertion low to high)                                |
| 3     | Once the PLL is locked to the CLK_IN input clock, the buffer enters state 3 and enables outputs for normal operation.<br>(Notes 45, 46) |

45. The total power up latency from power on to all outputs active must be less than 1.8 ms (assuming a valid clock is present on CLK\_IN input).  
 46. If power is valid and powerdown is de-asserted (PWRGD asserted) but no input clocks are present on the CLK\_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, PWRDN# de-asserted (PWRGD asserted) with the PLL locked/stable and the DIF outputs enabled.

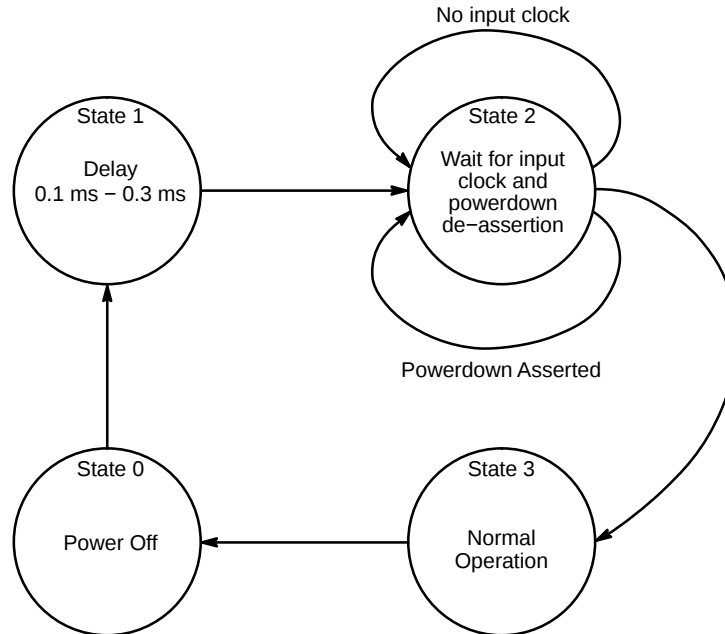


Figure 4. Buffer Power-Up State Diagram

## Device Power-Up Sequence

Follow the power-up sequence below for proper device functionality:

1. PWRGD/PWRDN# pin must be Low.
2. Assign remaining control pins to their required state (100M\_133M#, HBW\_BYPASS\_LBW#, SDA, SCL)

3. Apply power to the device.

4. Once the VDD pin has reached a valid VDDmin level (3.3V –5%), the PWRGD/PWRDN# pin must be asserted High. See Figure 5.

Note: If no clock is present on the CLK\_IN/CLK\_IN# pins when device is powered up, there will be no clock on DIF/DIF# outputs.

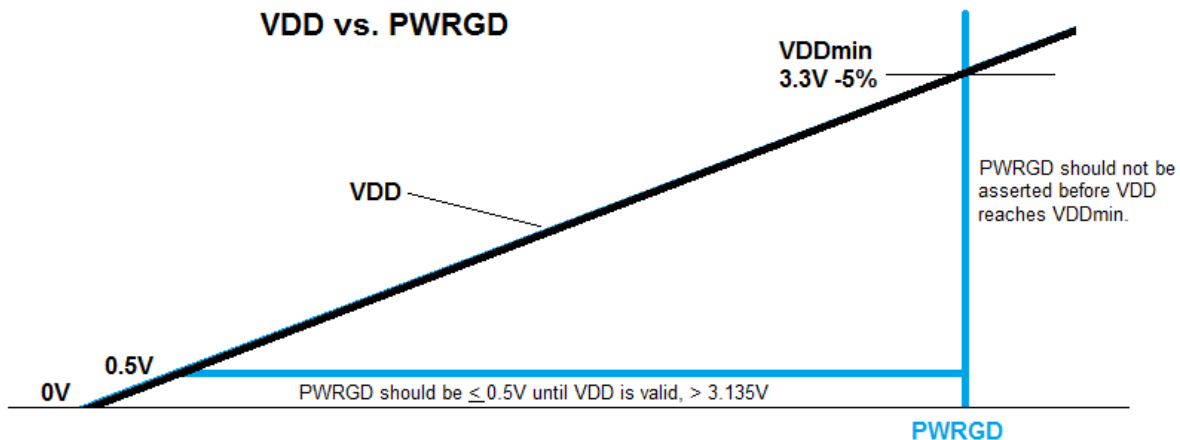


Figure 5. PWRGD and VDD Relationship Diagram

## GENERAL SMBus SERIAL INTERFACE INFORMATION

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Clock (device) will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Clock (device) will **acknowledge**
- Controller (host) sends the byte count = X
- Clock (device) will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Clock (device) will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Table 20. INDEX BLOCK WRITE OPERATION

| Controller (Host)   |           |        | Clock (Device) |
|---------------------|-----------|--------|----------------|
| T                   | starT bit | X Byte |                |
| Slave Address       |           |        |                |
| WR                  | WRite     |        |                |
|                     |           |        | ACK            |
| Beginning Byte = N  |           |        |                |
|                     |           |        | ACK            |
| Data Byte Count = X |           |        |                |
|                     |           |        | ACK            |
| Beginning Byte N    |           |        |                |
|                     |           |        | ACK            |
| O                   |           |        |                |
| O                   |           |        | O              |
| O                   |           |        | O              |
|                     |           |        | O              |
| Byte N + X - 1      |           |        |                |
|                     |           |        | ACK            |
| P                   | stoP bit  |        |                |

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Clock (device) will **acknowledge**

- Controller (host) sends the beginning byte location = N
- Clock (device) will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Clock (device) will **acknowledge**
- Clock (device) will send the data byte count = X
- Clock (device) sends Byte N + X - 1
- Clock (device) sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Table 21. INDEX BLOCK READ OPERATION

| Controller (Host)  |                 |        | Clock (Device)      |
|--------------------|-----------------|--------|---------------------|
| T                  | starT bit       | X Byte |                     |
| Slave Address      |                 |        |                     |
| WR                 | WRite           |        |                     |
|                    |                 |        | ACK                 |
| Beginning Byte = N |                 |        |                     |
|                    |                 |        | ACK                 |
| RT                 | Repeat starT    |        |                     |
| Slave Address      |                 |        |                     |
| RD                 | ReaD            |        |                     |
|                    |                 |        | ACK                 |
|                    |                 |        |                     |
|                    |                 |        | Data Byte Count = X |
| ACK                |                 |        |                     |
|                    |                 |        | Beginning Byte N    |
| ACK                |                 |        |                     |
|                    |                 |        | O                   |
| O                  |                 |        | O                   |
| O                  |                 |        | O                   |
| O                  |                 |        |                     |
|                    |                 |        | Byte N + X - 1      |
| N                  | Not acknowledge |        |                     |
| P                  | stoP bit        |        |                     |

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**Table 22. SMBus ADDRESSING**

| SA_1 and SA_0 | SMBus 8-bit Address (Rd/Wrt bit = 0) |
|---------------|--------------------------------------|
| 00            | D8                                   |
| 0M            | DA                                   |
| 01            | DE                                   |
| M0            | C2                                   |
| MM            | C4                                   |
| M1            | C6                                   |
| 10            | CA                                   |
| 1M            | CC                                   |
| 11            | CE                                   |

**Table 23. SMBus Table: PLL MODE, AND FREQUENCY SELECT REGISTER**

| Byte 0 | Pin # | Name       | Control Function                 | Type | 0                                     | 1       | Default |
|--------|-------|------------|----------------------------------|------|---------------------------------------|---------|---------|
| Bit 7  | 4     | PLL Mode 1 | PLL Operating Mode Rd back 1     | R    | See PLL Operating Mode Readback Table |         | Latch   |
| Bit 6  | 4     | PLL Mode 0 | PLL Operating Mode Rd back 0     | R    |                                       |         | Latch   |
| Bit 5  | 72/71 | DIF_18_En  | Output Control overrides OE# pin | RW   | Low/Low                               | Enable  | 1       |
| Bit 4  | 68/67 | DIF_17_En  | Output Control overrides OE# pin | RW   | Low/Low                               | Enable  | 1       |
| Bit 3  | 66/65 | DIF_16_En  | Output Control overrides OE# pin | RW   | Low/Low                               | Enable  | 1       |
| Bit 2  |       | Reserved   |                                  |      |                                       |         | 0       |
| Bit 1  |       | Reserved   |                                  |      |                                       |         | 0       |
| Bit 0  | 3     | 100M_133M# | Frequency Select Readback        | R    | 133 MHz                               | 100 MHz | Latch   |

**Table 24. SMBus TABLE: OUTPUT CONTROL REGISTER**

| Byte 1 | Pin # | Name     | Control Function                 | Type | 0       | 1      | Default |
|--------|-------|----------|----------------------------------|------|---------|--------|---------|
| Bit 7  | 38/37 | DIF_7_En | Output Control overrides OE# pin | RW   | Low/Low | Enable | 1       |
| Bit 6  | 35/36 | DIF_6_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 5  | 31/32 | DIF_5_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 4  | 29/30 | DIF_4_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 3  | 25/26 | DIF_3_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 2  | 23/24 | DIF_2_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 1  | 19/20 | DIF_1_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 0  | 17/18 | DIF_0_En | Output Control overrides OE# pin | RW   |         |        | 1       |

**Table 25. SMBus TABLE: OUTPUT CONTROL REGISTER**

| Byte 2 | Pin # | Name      | Control Function                 | Type | 0       | 1      | Default |
|--------|-------|-----------|----------------------------------|------|---------|--------|---------|
| Bit 7  | 62/61 | DIF_15_En | Output Control overrides OE# pin | RW   | Low/Low | Enable | 1       |
| Bit 6  | 60/59 | DIF_14_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 5  | 56/55 | DIF_13_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 4  | 54/53 | DIF_12_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 3  | 50/49 | DIF_11_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 2  | 48/47 | DIF_10_En | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 1  | 44/43 | DIF_9_En  | Output Control overrides OE# pin | RW   |         |        | 1       |
| Bit 0  | 42/41 | DIF_8_En  | Output Control overrides OE# pin | RW   |         |        | 1       |

Table 26. SMBus TABLE: RESERVED REGISTER

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

Table 27. SMBus TABLE: RESERVED REGISTER

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

Table 28. SMBus TABLE: VENDOR & REVISION ID REGISTER

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | –     | RID3 | REVISION ID      | R    | – | – | X       |
| Bit 6  | –     | RID2 |                  | R    | – | – | X       |
| Bit 5  | –     | RID1 |                  | R    | – | – | X       |
| Bit 4  | –     | RID0 |                  | R    | – | – | X       |
| Bit 3  | –     | VID3 | VENDOR ID        | R    | – | – | 1       |
| Bit 2  | –     | VID2 |                  | R    | – | – | 1       |
| Bit 1  | –     | VID1 |                  | R    | – | – | 1       |
| Bit 0  | –     | VID0 |                  | R    | – | – | 1       |

Table 29. SMBus TABLE: DEVICE ID

| Byte 6 | Pin # | Name              | Control Function | Type | 0                                   | 1 | Default |
|--------|-------|-------------------|------------------|------|-------------------------------------|---|---------|
| Bit 7  | –     | Device ID 7 (MSB) |                  | R    | Device ID is 130 decimal or 82 hex. |   | 1       |
| Bit 6  | –     | Device ID 6       |                  | R    |                                     |   | 1       |
| Bit 5  | –     | Device ID 5       |                  | R    |                                     |   | 0       |
| Bit 4  | –     | Device ID 4       |                  | R    |                                     |   | 1       |
| Bit 3  | –     | Device ID 3       |                  | R    |                                     |   | 1       |
| Bit 2  | –     | Device ID 2       |                  | R    |                                     |   | 0       |
| Bit 1  | –     | Device ID 1       |                  | R    |                                     |   | 1       |
| Bit 0  | –     | Device ID 0       |                  | R    |                                     |   | 1       |

Table 30. SMBus TABLE: BYTE COUNT REGISTER

| Byte 7 | Pin # | Name     | Control Function                                                      | Type | 0                                                                         | 1 | Default |
|--------|-------|----------|-----------------------------------------------------------------------|------|---------------------------------------------------------------------------|---|---------|
| Bit 7  |       | Reserved |                                                                       |      |                                                                           |   | 0       |
| Bit 6  |       | Reserved |                                                                       |      |                                                                           |   | 0       |
| Bit 5  |       | Reserved |                                                                       |      |                                                                           |   | 0       |
| Bit 4  | –     | BC4      | Writing to this register configures how many bytes will be read back. | RW   | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. |   | 0       |
| Bit 3  | –     | BC3      |                                                                       | RW   |                                                                           |   | 1       |
| Bit 2  | –     | BC2      |                                                                       | RW   |                                                                           |   | 0       |
| Bit 1  | –     | BC1      |                                                                       | RW   |                                                                           |   | 0       |
| Bit 0  | –     | BC0      |                                                                       | RW   |                                                                           |   | 0       |

Table 31. SMBus TABLE: RESERVED REGISTER

| Byte 8 | Pin # | Name     | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7  |       | Reserved |                  |      |   |   | 0       |
| Bit 6  |       | Reserved |                  |      |   |   | 0       |
| Bit 5  |       | Reserved |                  |      |   |   | 0       |
| Bit 4  |       | Reserved |                  |      |   |   | 0       |
| Bit 3  |       | Reserved |                  |      |   |   | 0       |
| Bit 2  |       | Reserved |                  |      |   |   | 0       |
| Bit 1  |       | Reserved |                  |      |   |   | 0       |
| Bit 0  |       | Reserved |                  |      |   |   | 0       |

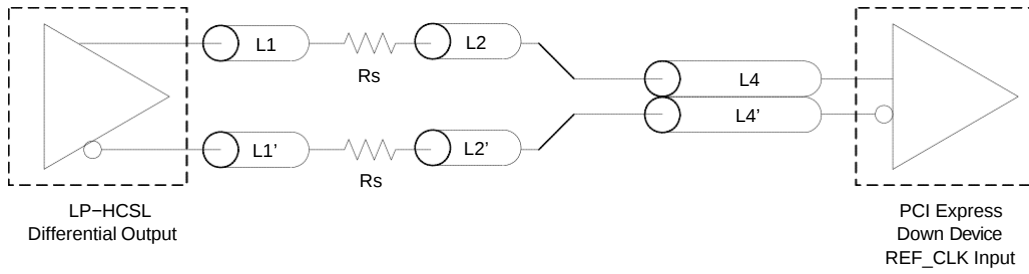
Table 32. DIF REFERENCE CLOCK

| Common R Recommendations for Differential Routing                |  | Dimension or Value | Unit     |
|------------------------------------------------------------------|--|--------------------|----------|
| L1 length, route as non-coupled 50 $\Omega$ trace (see Figure 6) |  | 0.5 max            | inch     |
| L2 length, route as non-coupled 50 $\Omega$ trace (see Figure 6) |  | 0.2 max            | inch     |
| L3 length, route as non-coupled 50 $\Omega$ trace (see Figure 6) |  | 0.2 max            | inch     |
| Rs (100 $\Omega$ differential traces) (see Figure 6)             |  | 33                 | $\Omega$ |
| Rs (85 $\Omega$ differential traces) (see Figure 6)              |  | 27                 | $\Omega$ |

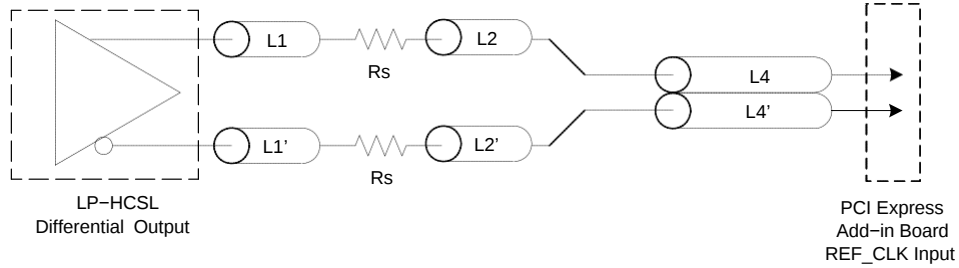
| Down Device Differential Routing                                                       |  |                     |      |
|----------------------------------------------------------------------------------------|--|---------------------|------|
| L4 length, route as coupled micro strip 100 $\Omega$ differential trace (see Figure 6) |  | 2 min to 16 max     | inch |
| L4 length, route as coupled strip line 100 $\Omega$ differential trace (see Figure 6)  |  | 1.8 min to 14.4 max | inch |

| Differential Routing to PCI Express Connector                                         |  |                       |      |
|---------------------------------------------------------------------------------------|--|-----------------------|------|
| L4 length, route as coupled microstrip 100 $\Omega$ differential trace (see Figure 7) |  | 0.25 to 14 max        | inch |
| L4 length, route as coupled stripline 100 $\Omega$ differential trace (see Figure 7)  |  | 0.225 min to 12.6 max | inch |

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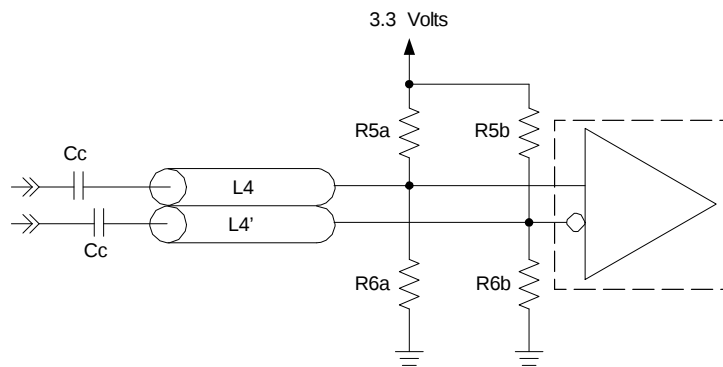
**Figure 6. Down Device Routing**



**Figure 7. PCI Express Connector Routing**

**Table 33. CABLE CONNECTED AC COUPLED APPLICATION (Figure 8)**

| Component | Value       | Note |
|-----------|-------------|------|
| R5a, R5b  | 8.2k 5%     |      |
| R6a, R6b  | 1k 5%       |      |
| Cc        | 0.1 $\mu$ F |      |
| Vcm       | 0.350 V     |      |



**Figure 8.**

# NB3W1900L

## POWER FILTERING EXAMPLE

### Ferrite Bead Power Filtering

Recommended ferrite bead filtering equivalent to the following:

600  $\Omega$  impedance at 100.00 MHz,  $\leq 0.1 \Omega$  DCR max.,  $\geq 400$  mA current rating.

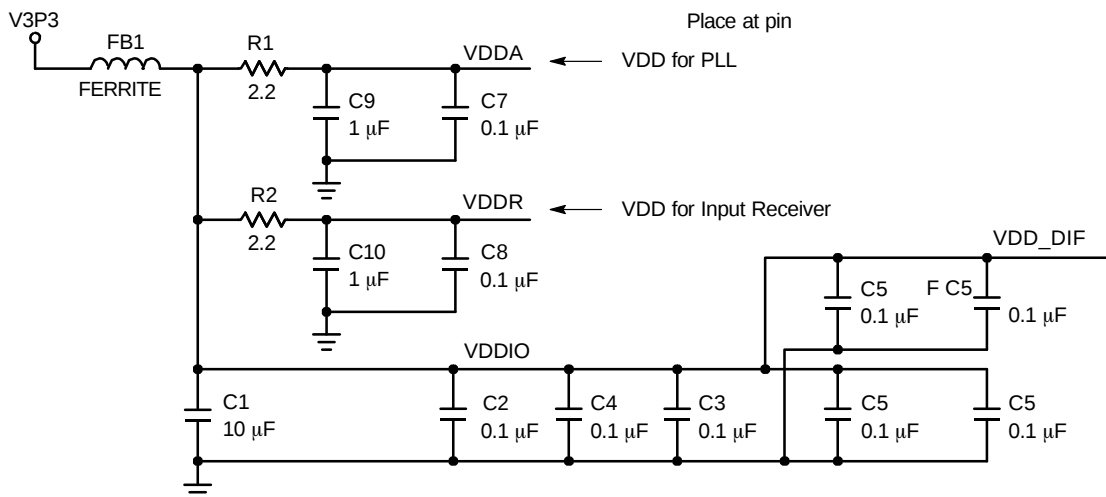


Figure 9. Schematic Example of the NB3W1900L Power Filtering

Table 34. ORDERING INFORMATION

| Device         | Package             | Shipping <sup>†</sup> |
|----------------|---------------------|-----------------------|
| NB3W1900LMNG   | QFN-72<br>(Pb-Free) | 168 Units / Tray      |
| NB3W1900LMNTXG | QFN-72<br>(Pb-Free) | 1,000 / Tape & Reel   |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

