Data Sheet

COMLINEAR® CLC1005, CLC2005

Low Cost, +2.7V to 5.5V, 260MHz Rail-to-Rail Amplifiers

FEATURES

- 260MHz bandwidth
- Fully specified at +2.7V and +5V supplies
- Output voltage range: 0.036V to 4.953V; V_S = +5; R_L = 2kΩ
- Input voltage range: -0.3V to +3.8V; V_S = +5
- 145V/µs slew rate
- 4.2mA supply current per amplifier
- ±55mA linear output current
- ±85mA short circuit current
- CLC2005 directly replaces AD8052, AD8042 and AD8092 in single supply applications
- CLC1005 directly replaces AD8051, AD8041 and AD8091 in single supply applications
- CLC2005: Pb-free SOIC-8 package
- CLC1005: Pb-free SOIC-8, SOT23-5 pkgs

APPLICATIONS

- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Telecom and optical terminals
- Video driver

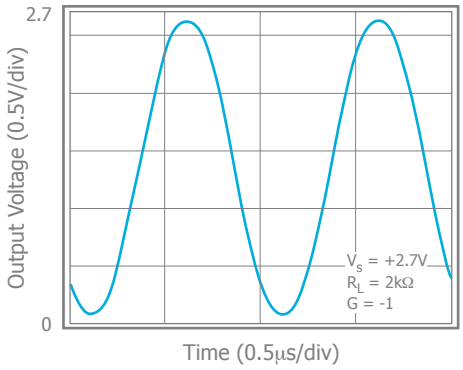
General Description

The COMLINEAR CLC1005 (single) and CLC2005 (dual) are low cost, voltage feedback amplifiers. These amplifiers are designed to operate on +2.7V to +5V, or ±2.5V supplies. The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

The CLC1005 and CLC2005 offer superior dynamic performance with a 260MHz small signal bandwidth and 145V/µs slew rate. The combination of low power, high output current drive, and rail-to-rail performance make these amplifiers well suited for battery-powered communication/computing systems.

The combination of low cost and high performance make the CLC1005 and CLC2005 suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, and color copiers.

Output Swing



Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1005ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC1005IST5X	SOT23-5	Yes	Yes	-40°C to +85°C	Reel
CLC2005ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC2005IMP8X	MSOP-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

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48720 Kato Road, Fremont CA 94538, USA

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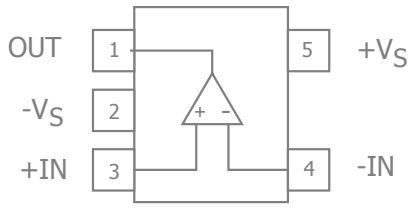
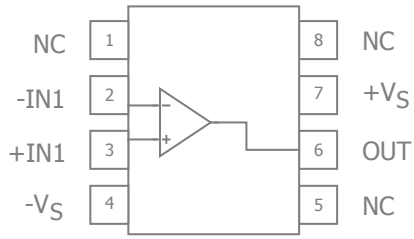
CLC1005 Pin Configurations

SOT23-5



SOIC-8



CLC1005 Pin Assignments

SOT23-5

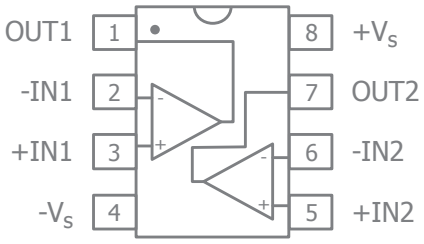
Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

SOIC-8

Pin No.	Pin Name	Description
1	NC	No Connect
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	NC	No Connect
6	OUT	Negative input
7	$+V_S$	Positive supply
8	NC	No Connect

CLC2005 Pin Configuration

SOIC-8



CLC2005 Pin Assignments

SOIC-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	+6	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8
Human Body Model (HBM)	2.5kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		5.5	V

Electrical Characteristics at 2.7V

V_S = +2.7V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth(2)	G = +1, V_{OUT} = 0.05V_{pp}		215		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		85		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		36		MHz
GBWP	Gain Bandwidth Product			86		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time(2)	V_{OUT} = 0.2V step		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		9		%
SR	Slew Rate	2.7V step, G = -1		130		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion(2)	1V_{pp}, 5MHz		79		dBc
HD3	3rd Harmonic Distortion(2)	1V_{pp}, 5MHz		82		dBc
		1V_{pp}, 5MHz		77		dB
e_n	Input Voltage Noise	> 1MHz		16		nV/√Hz
i_n	Input Current Noise	> 1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk(1)	CLC2005, 10MHz		65		dB
DC Performance						
V_{IO}	Input Offset Voltage			-1.6		mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current			3		µA
dI_b	Average Drift			7		nA/°C
I_{IO}	Input Offset Current			0.1		µA
PSRR	Power Supply Rejection Ratio(1)	DC	52	57		dB
A_{OL}	Open-Loop Gain			75		dB
I_S	Quiescent Current	Per Amplifier		3.9		mA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, V_{cm} = 0V to V_s -1.5		87		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_s/2		0.023 to 2.66		V
		R_L = 2kΩ to V_s/2		0.025 to 2.653		V
		R_L = 150Ω to V_s/2		0.065 to 2.55		V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short-Circuit Output Current			±85		mA
V_s	Power Supply Operating Range		2.5	2.7	5.5	V

Notes:

1. 100% tested at 25°C.
2. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0).

Electrical Characteristics at 5V

V_S = 5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth(2)	G = +1, V_{OUT} = 0.05V_{pp}		260		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		90		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		40		MHz
GBWP	Gain Bandwidth Product			90		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time(2)	V_{OUT} = 0.2V step		3.6		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		7		%
SR	Slew Rate	5V step, G = -1		145		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion(2)	2V_{pp}, 5MHz		71		dBc
HD3	3rd Harmonic Distortion(2)	2V_{pp}, 5MHz		78		dBc
		2V_{pp}, 5MHz		70		dB
DG	Differential Gain	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.06		%
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.08		%
DP	Differential Phase	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.07		°
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	>1MHz		16		nV/√Hz
i_n	Input Current Noise	>1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk(2)	CLC2005, 10MHz		62		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-8	1.4	+8	mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current(1)		-8	3	+8	µA
dI_b	Average Drift			7		nA/°C
I_{IO}	Input Offset Current(1)		-0.8	0.1	+0.8	µA
PSRR	Power Supply Rejection Ratio(1)	DC	52	57		dB
A_{OL}	Open-Loop Gain(1)		68	78		dB
I_S	Quiescent Current(1)	Per Amplifier		4.2	5.2	mA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio(1)	DC, V_{cm} = 0V to V_s -1.5	72	87		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_s/2		0.027 to 4.97		V
		R_L = 2kΩ to V_s/2		0.036 to 4.953		V
		R_L = 150Ω to V_s/2(1)	0.3	0.12 to 4.8	4.625	V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short-Circuit Output Current			±85		mA
V_s	Power Supply Operating Range		2.5	5	5.5	V

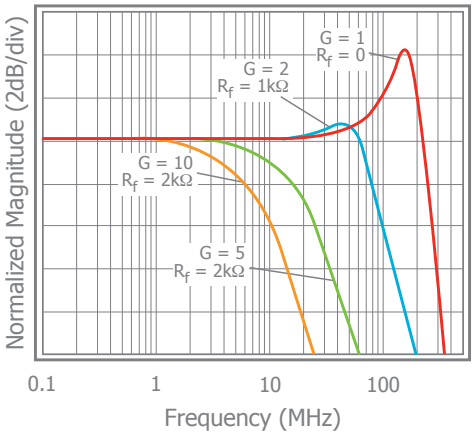
Notes:

1. 100% tested at 25°C.
2. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0).

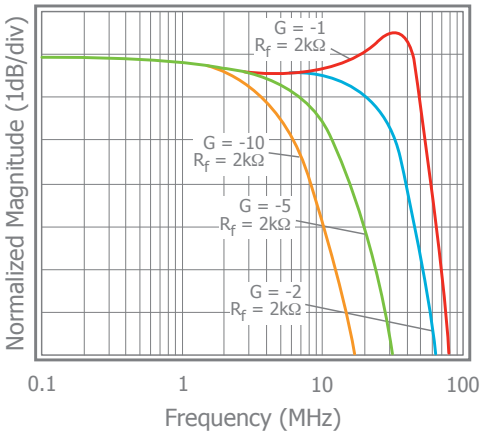
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

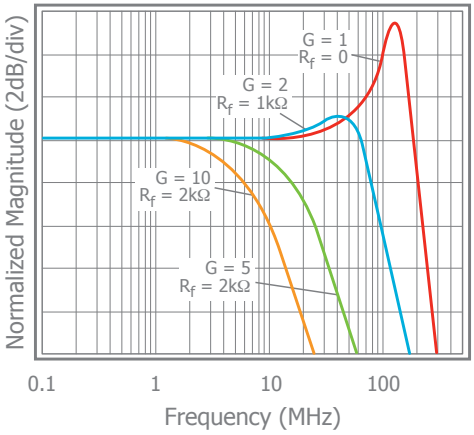
Non-Inverting Frequency Response V_S = +5V



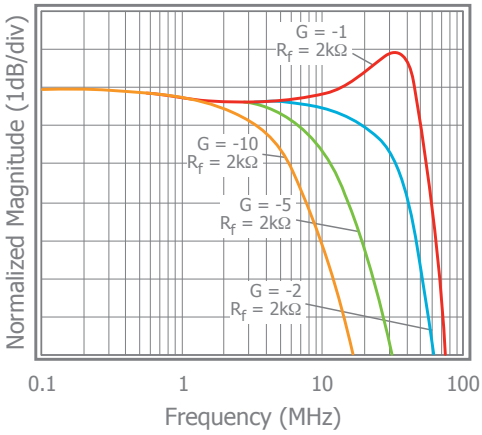
Inverting Frequency Response V_S = +5V



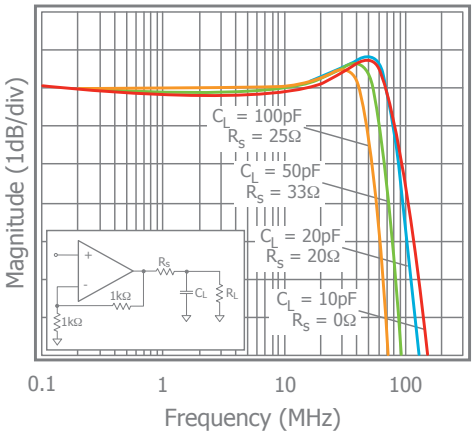
Non-Inverting Frequency Response V_S = +2.7V



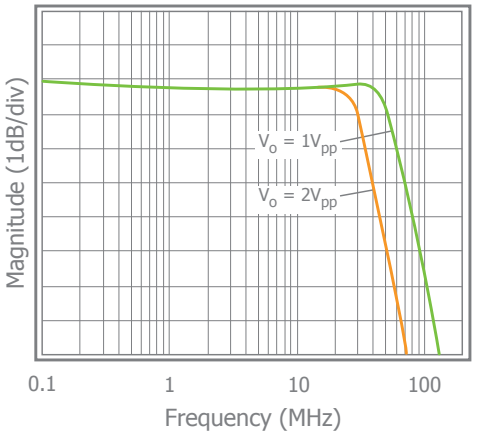
Inverting Frequency Response V_S = +2.7V



Frequency Response vs. C_L



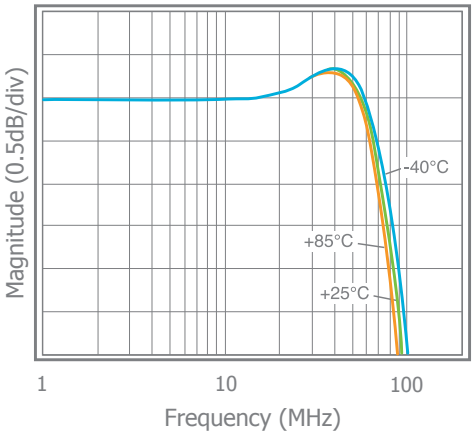
Large Signal Frequency Response



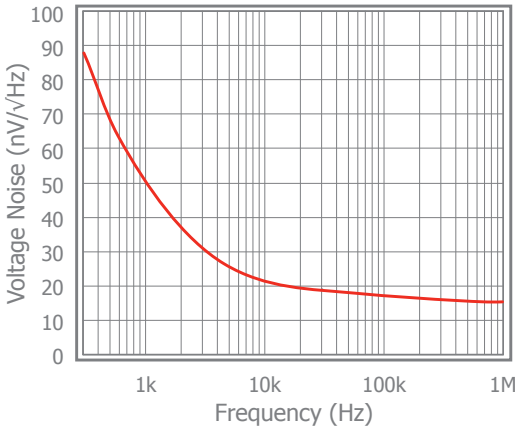
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

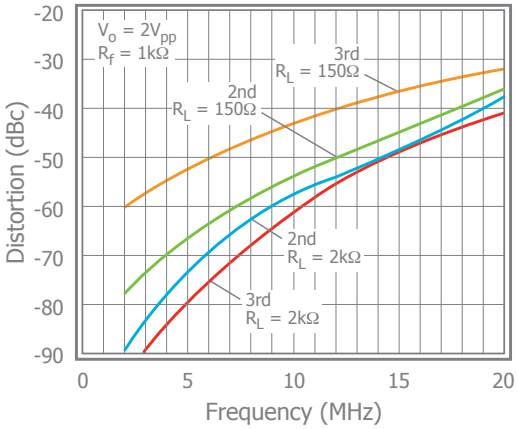
Frequency Response vs. Temperature



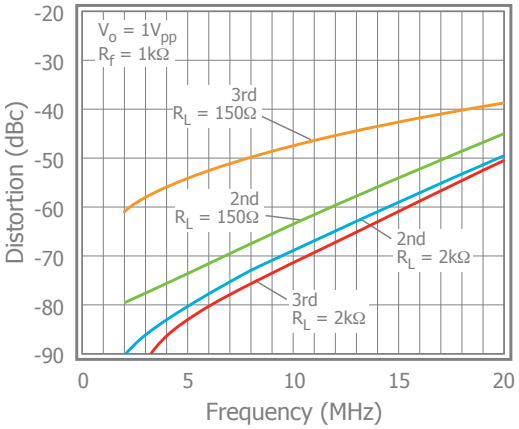
Input Voltage Noise



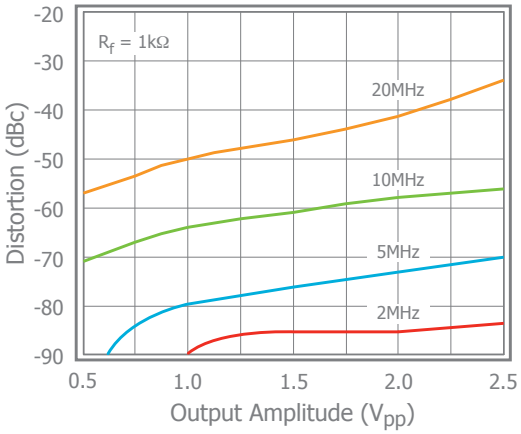
2nd & 3rd Harmonic Distortion; V_S = +5V



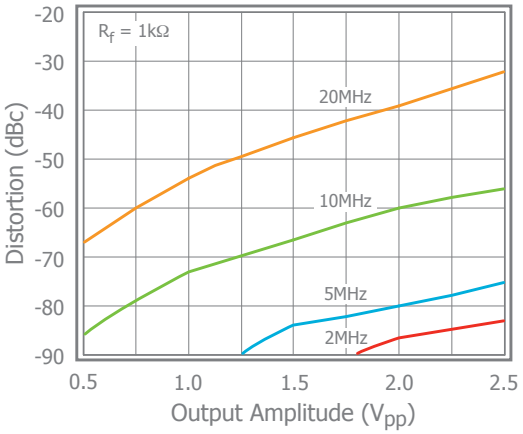
2nd & 3rd Harmonic Distortion; V_S = +2.7V



2nd Harmonic Distortion vs. V_o



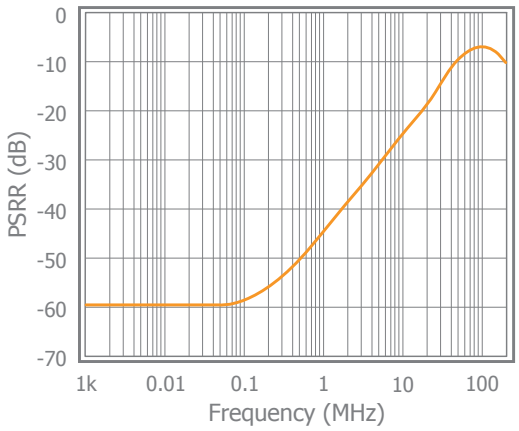
3rd Harmonic Distortion vs. V_o



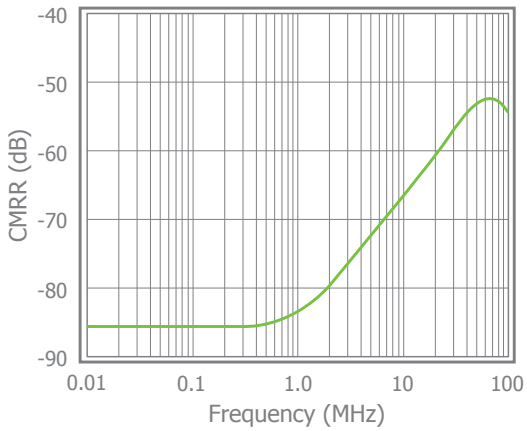
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

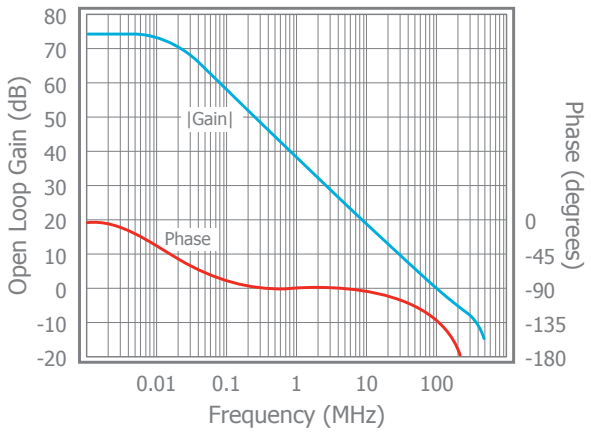
PSRR



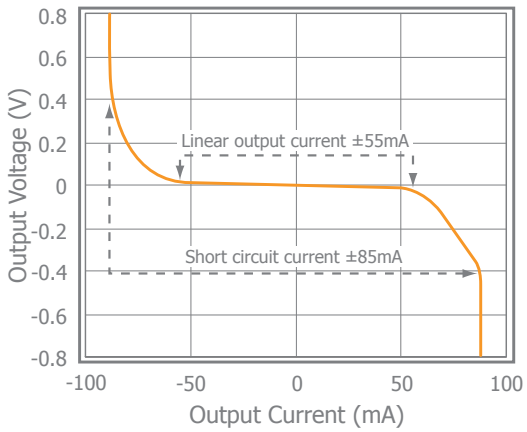
CMRR



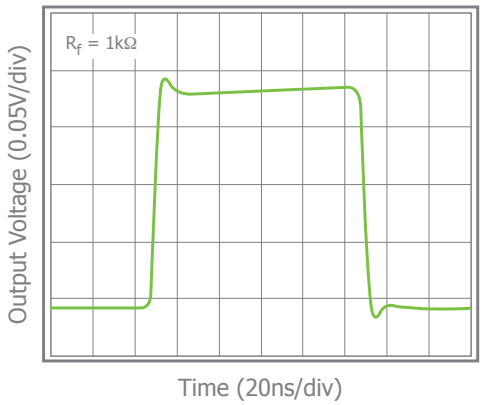
Open Loop Gain & Phase vs. Frequency



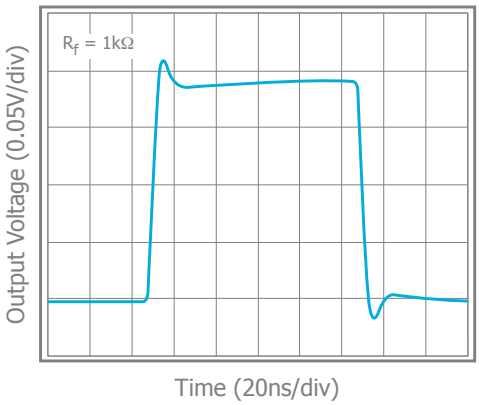
Output Current



Small Signal Pulse Response V_S = +5V



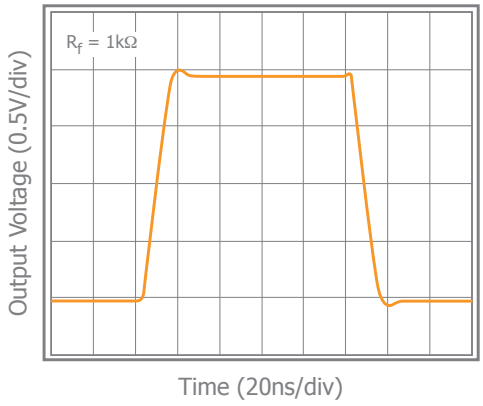
Small Signal Pulse Response V_S = +2.7V



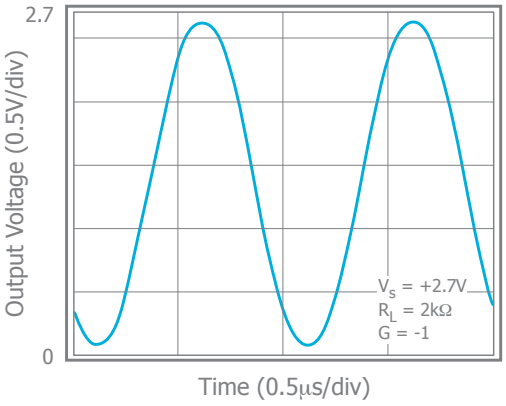
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

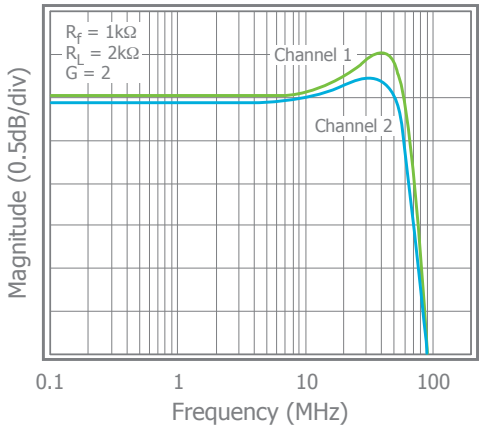
Large Signal Pulse Response V_S = +5V



Output Swing



Channel Matching V_S = +5V



Application Information

General Description

The CLC1005 and CLC2005 are single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process using a patent pending topography. They feature a rail-to-rail output stage and is unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 1.2V below V_S. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applicaitons.

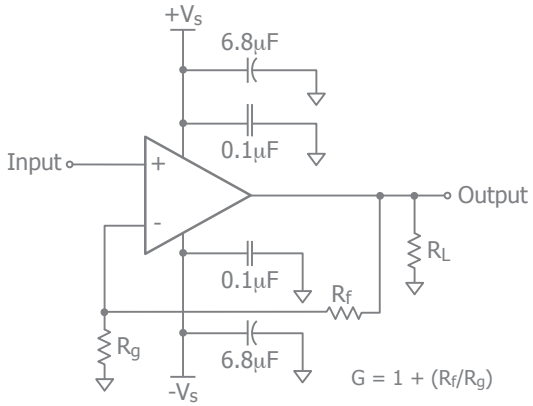


Figure 1. Typical Non-Inverting Gain Circuit

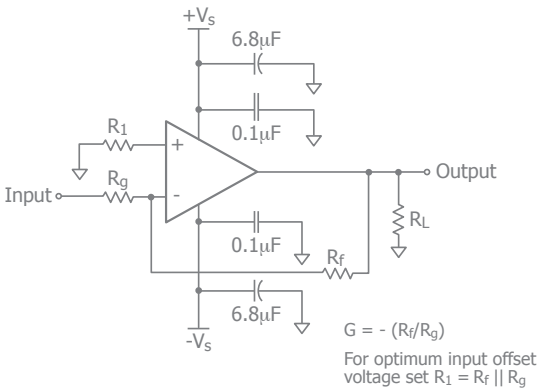


Figure 2. Typical Inverting Gain Circuit

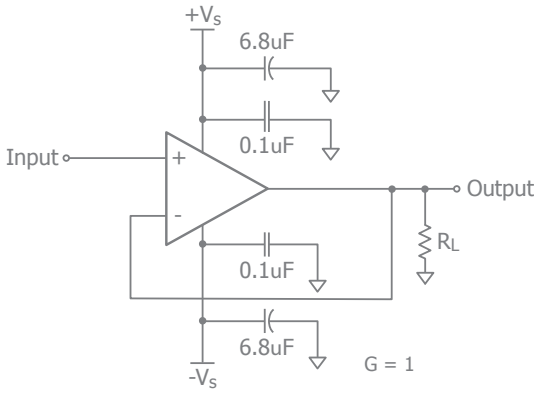


Figure 3. Unity Gain Circuit

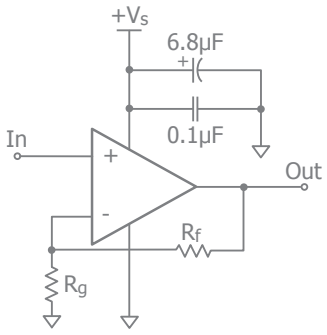


Figure 4. Single Supply Non-Inverting Gain Circuit

At non-inverting gains other than G = +1, keep R_g below 1kΩ to minimize peaking; thus, for optimum response at a gain of +2, a feedback resistor of 1kΩ is recommended. Figure 5 illustrates the CLC1005 and CLC2005 frequency response with both 1kΩ and 2kΩ feedback resistors.

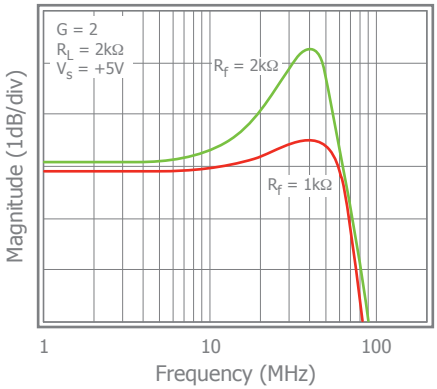


Figure 5: Frequency Response vs. R_f

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is over-driven and by how much the ranges are exceeded. The CLC1005 and CLC2005 will typically recover in less than 20ns from an overdrive condition. Figure 6 shows the CLC2005 in an overdriven condition.

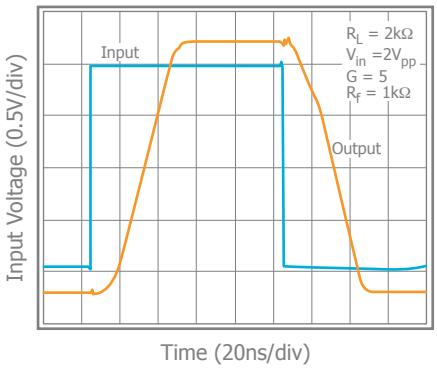


Figure 6: Overdrive Recovery

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS^2})/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC1009 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 7

shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

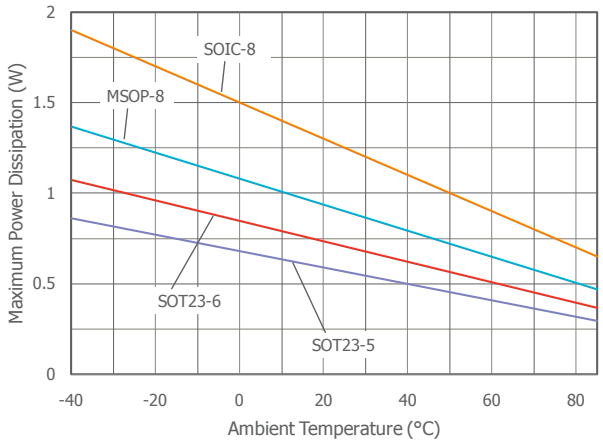


Figure 7. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 8.

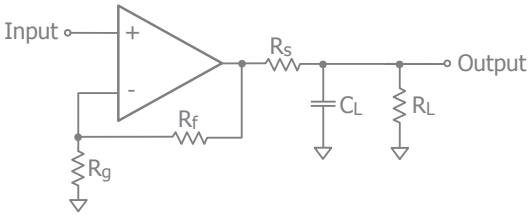


Figure 8. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response.

C_L (pF)	R_S (Ω)	-3dB BW (kHz)
10pF	0	100
20pF	20	94
50pF	33	72
100pF	25	58

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1005 in SOT23
CEB003	CLC1005 in SOIC
CEB006	CLC2005 in SOIC
CEB010	CLC2005 in MSOP

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 10-18. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

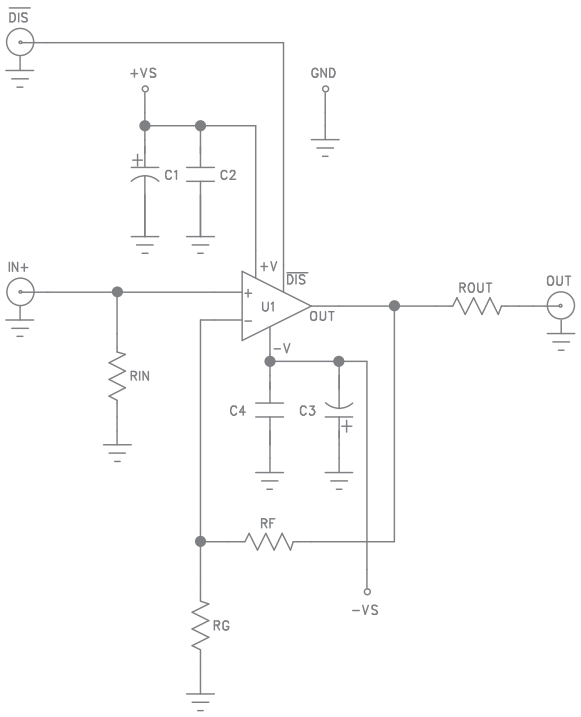


Figure 9. CEB002 & CEB003 Schematic

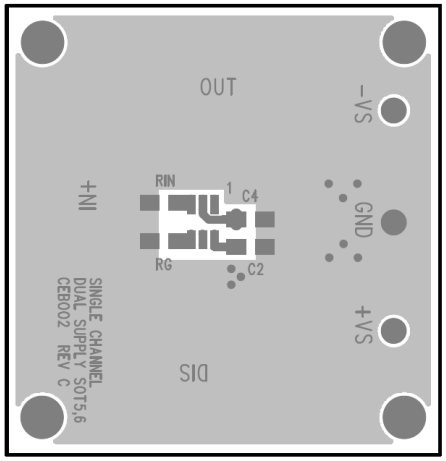


Figure 10. CEB002 Top View

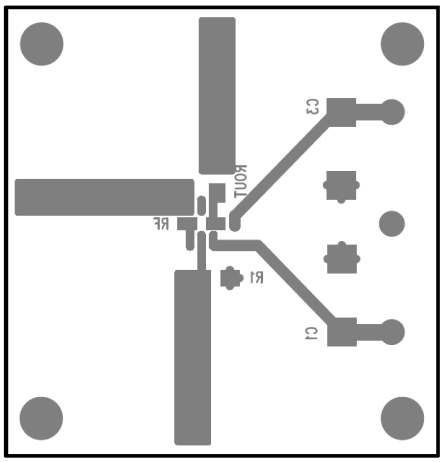


Figure 11. CEB002 Bottom View

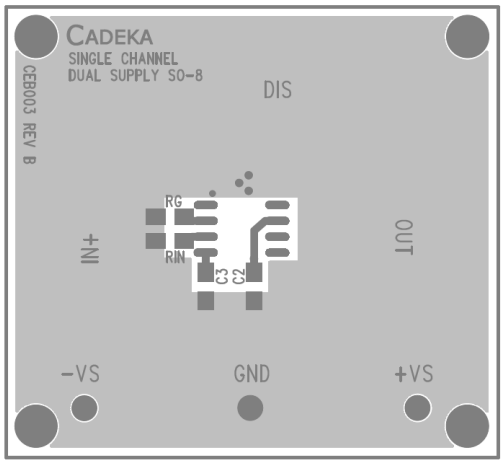


Figure 12. CEB003 Top View

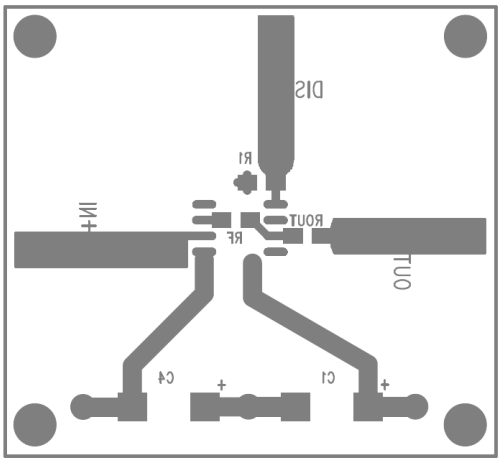


Figure 13. CEB003 Bottom View

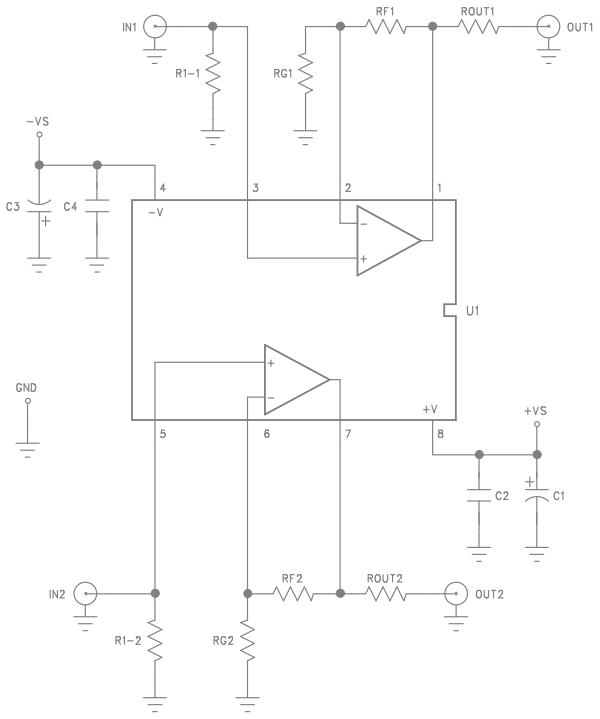


Figure 14. CEB006 & CEB010 Schematic

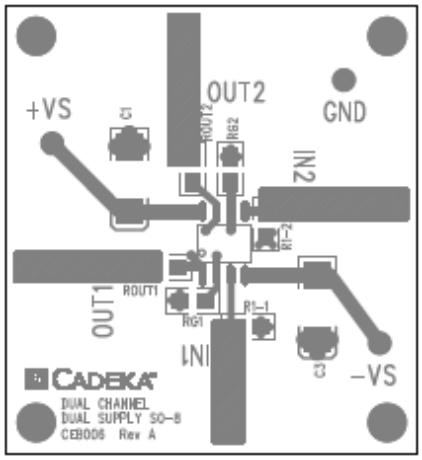


Figure 15. CEB006 Top View

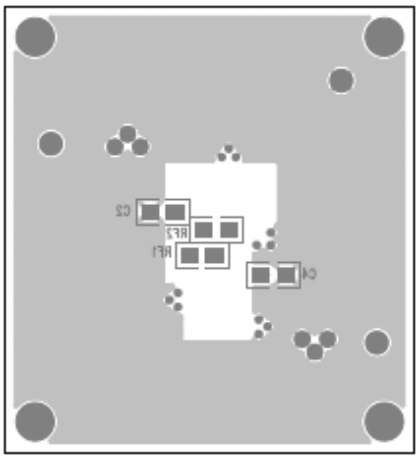


Figure 16. CEB006 Bottom View

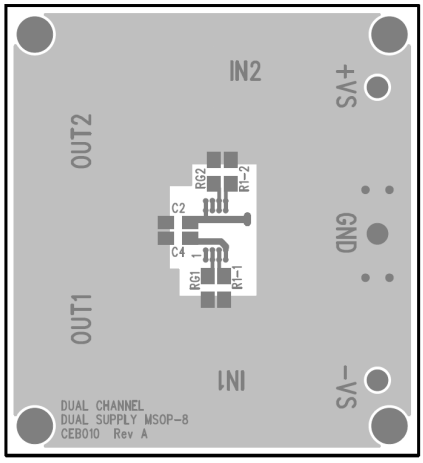


Figure 17. CEB010 Top View

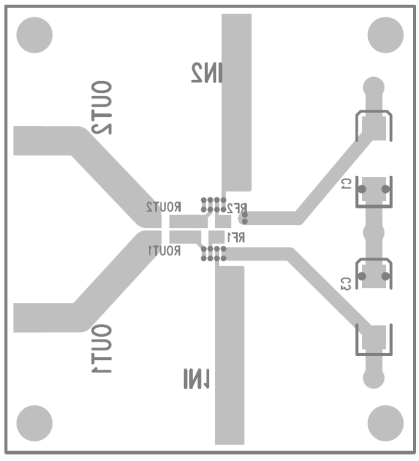
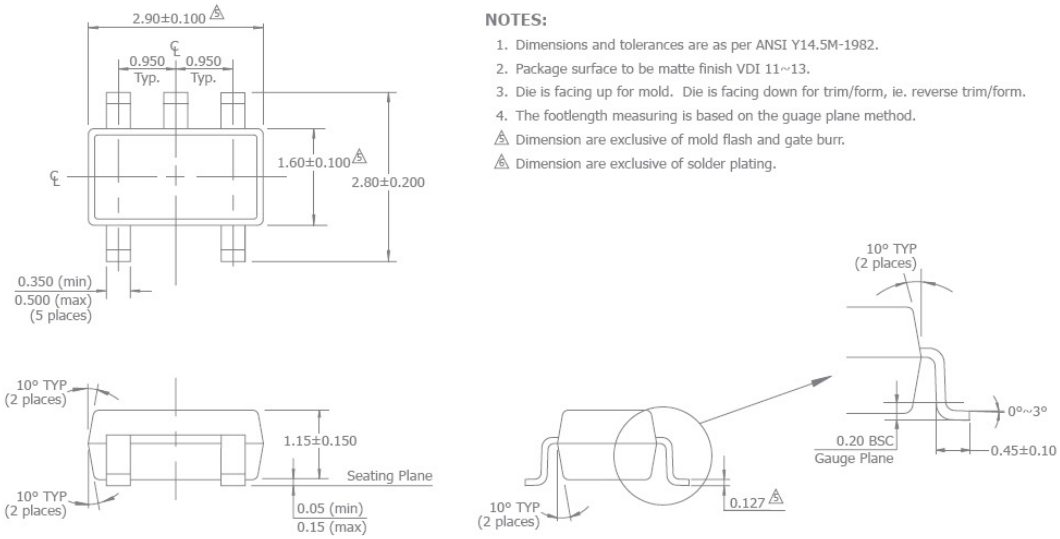


Figure 18. CEB010 Bottom View

Mechanical Dimensions

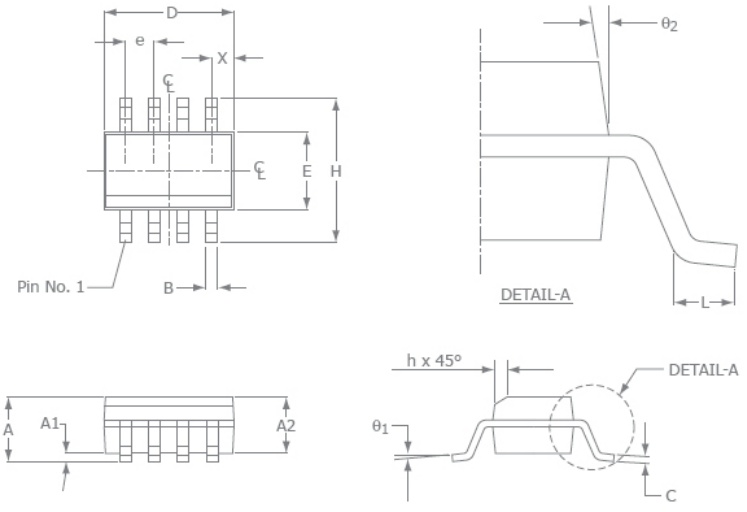
SOT23-5 Package



NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.
5. Dimension are exclusive of mold flash and gate burr.
6. Dimension are exclusive of solder plating.

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For Further Assistance:

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