Two-wire Serial Electrically Erasable and Programmable Read-only Memory

128K (16,384 x 8)

Atmel AT24C128C

Features

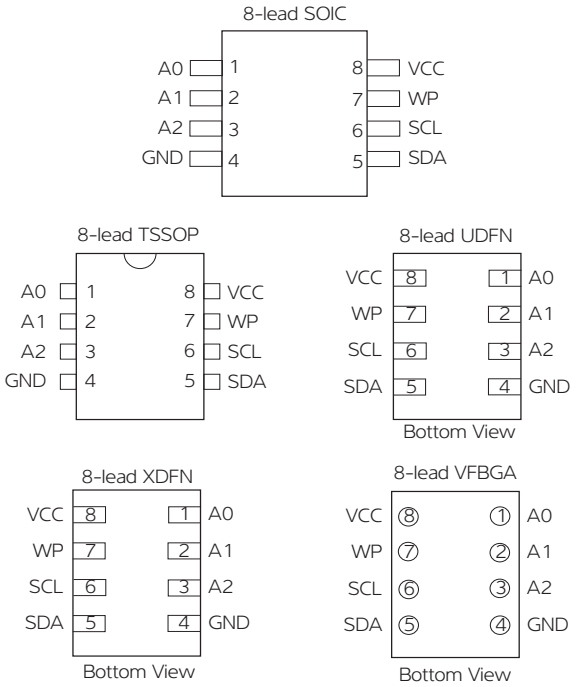
- Low-voltage and standard-voltage operation
  - V_{CC} = 1.7V to 5.5V
- Internally organized as 16,384 x 8
- Two-wire serial interface
- Schmitt trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 1MHz (5.5V, 2.5V), and 400kHz (1.7V) compatibility
- Write protect pin for hardware and software data protection
- 64-byte page write mode (partial page writes allowed)
- Self-timed write cycle (5ms max)
- High reliability
  - Endurance: One million write cycles
  - Data retention: 40 years
- Lead-free/halogen-free
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, and 8-ball VFBGA packages
- Die sales: Wafer form, tape and reel, and bumped wafers

Description

The Atmel® AT24C128C provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 16,384 words of 8 bits each. The cascadable feature of the device allows up to eight devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The device is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, and 8-ball VFBGA packages. This device operates from 1.7V to 5.5V.

Table 0-1. Pin Configurations

Pin Name	Function
A0–A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground



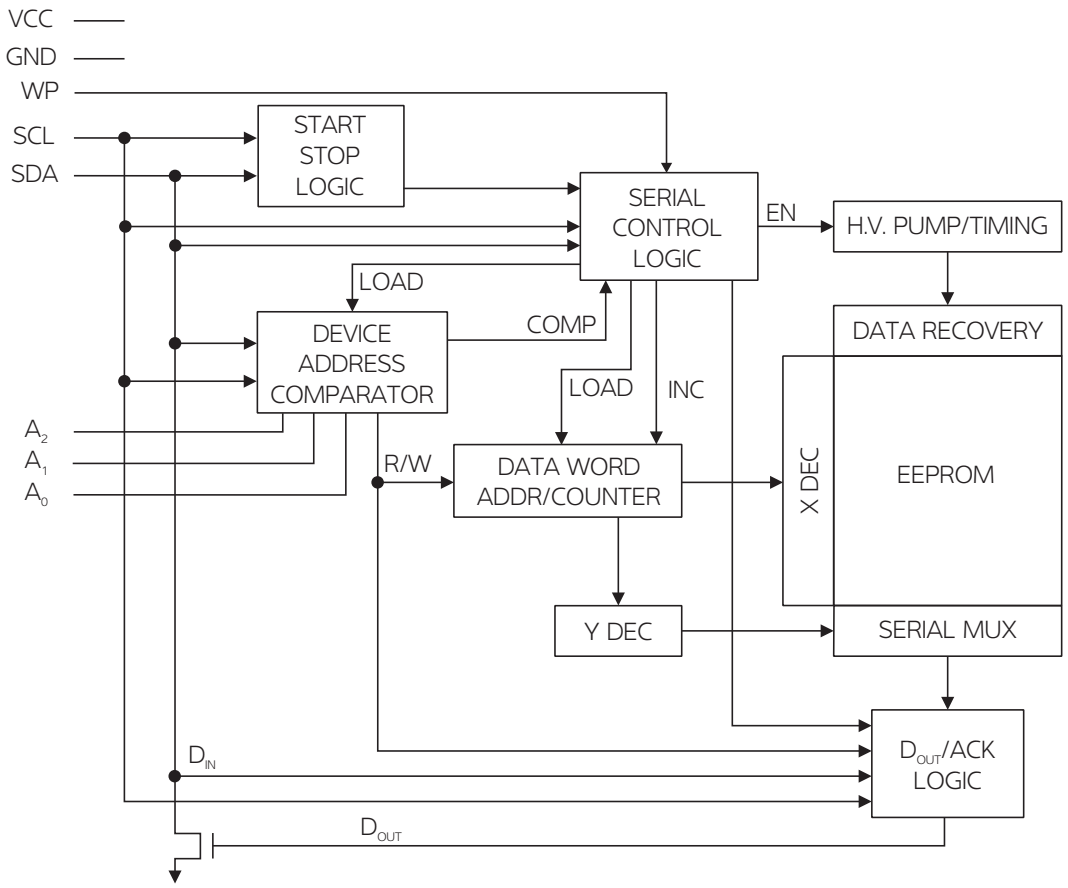
8734A–SEEPR–1/11

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only,and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram



2. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven, and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1, and A0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other Atmel AT24Cxx devices. When the pins are hardwired, as many as eight 128K devices may be addressed on a single bus system. (Device addressing is discussed in detail in Section 5. "Device Addressing" on page 8) A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A2, A1, and A0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to Vcc, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pin to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

3. Memory Organization

Atmel AT24C128C, 128K SERIAL EEPROM: The 128K is internally organized as 256 pages of 64 bytes each. Random word addressing requires a 14-bit data word address.

Table 3-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, SCL)	6	pF	V_{IN} = 0V

Notes: 1. This parameter is characterized, and is not 100% tested

Table 3-2. DC Characteristics

Applicable over recommended operating range from T_{AI} = - 40°C to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{CC} = 5.0V	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			- 0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Notes: 1. V_{IL} min and V_{IH} max are reference only, and are not tested

Table 3-3. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from T_{AI} = - 40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

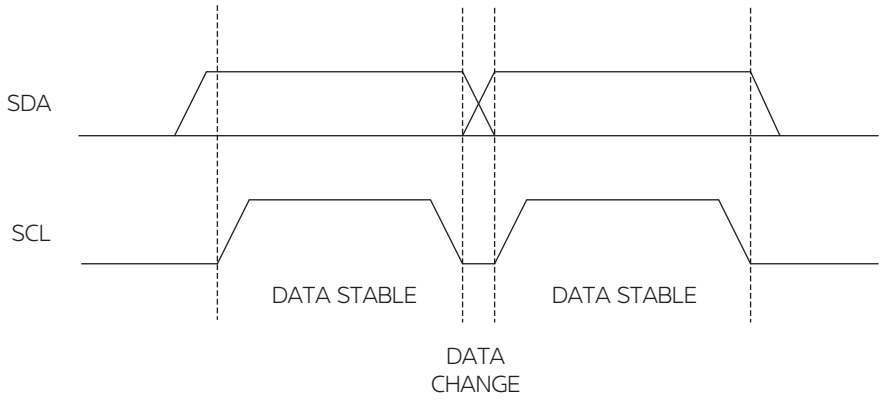
Symbol	Parameter	1.7V		2.5, 5.5V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_i	Noise Suppression Time[1]		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start[1]	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time[1]		0.3		0.3	µs
t_F	Inputs Fall Time[1]		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes:
1. This parameter is ensured by characterization, and is not 100% tested
2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50ns
   Input and output timing reference voltages: 0.5V_{CC}

4. Device Operation

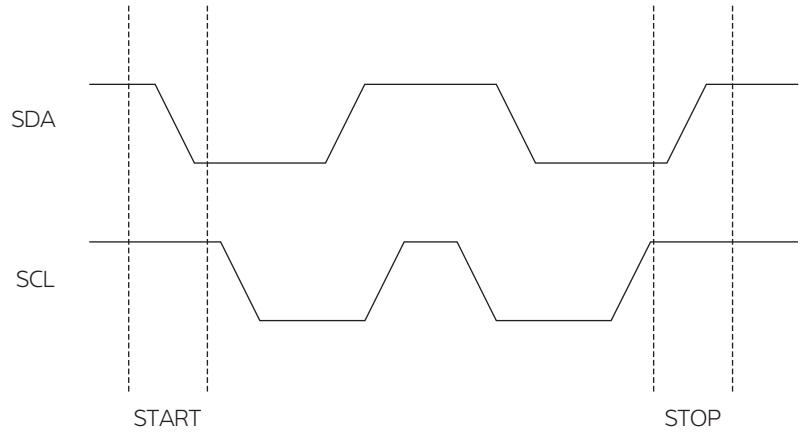
CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition, as defined below.

Figure 4-1. Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (see Figure 4-2).

Figure 4-2. Start and Stop Definition



STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 4-2).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The Atmel AT24C128C features a low-power standby mode that is enabled upon power-up and after the receipt of the stop bit and the completion of any internal operations.

SOFTWARE RESET: After an interruption in protocol, power loss, or system reset, any two-wire part can be protocol reset by following these steps: (a) Create a start bit condition, (b) clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-3. Software Reset

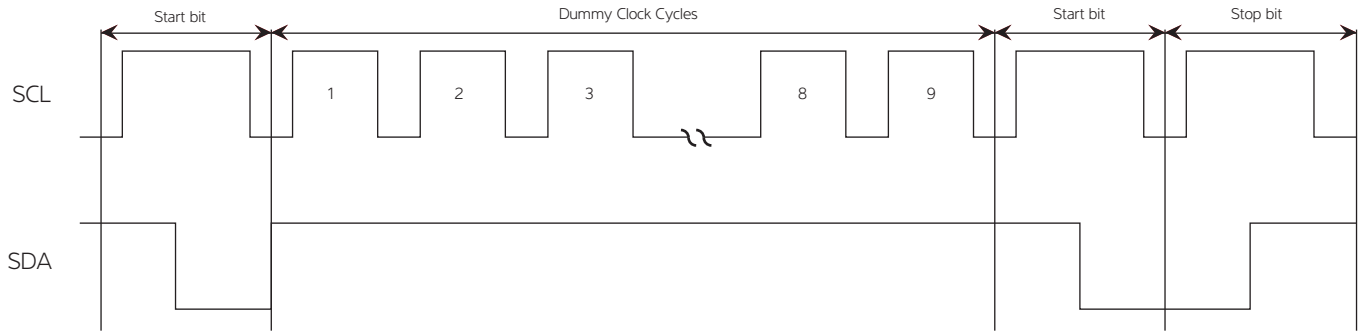


Figure 4-4. Bus Timing

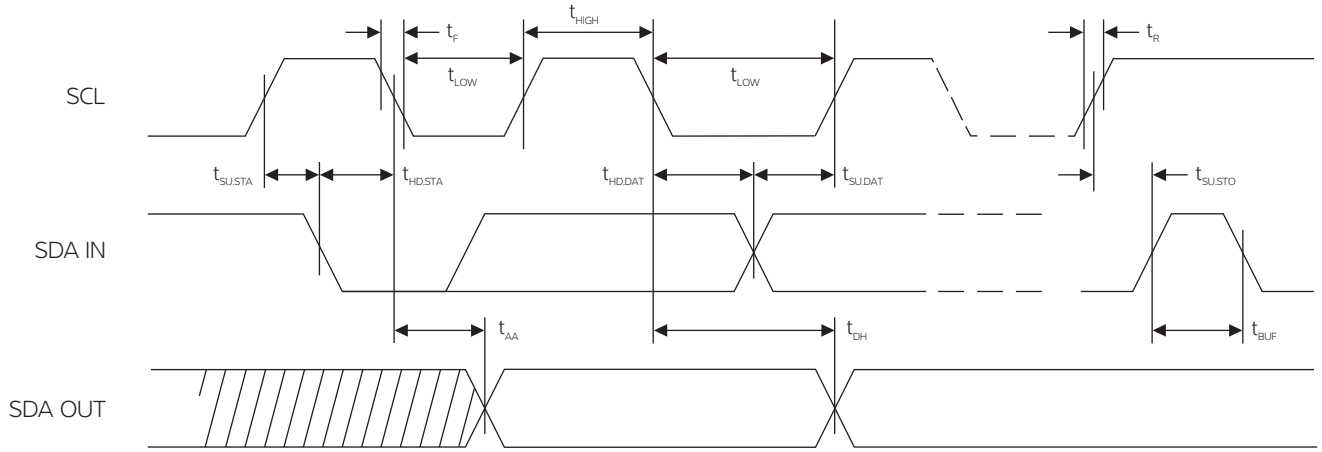
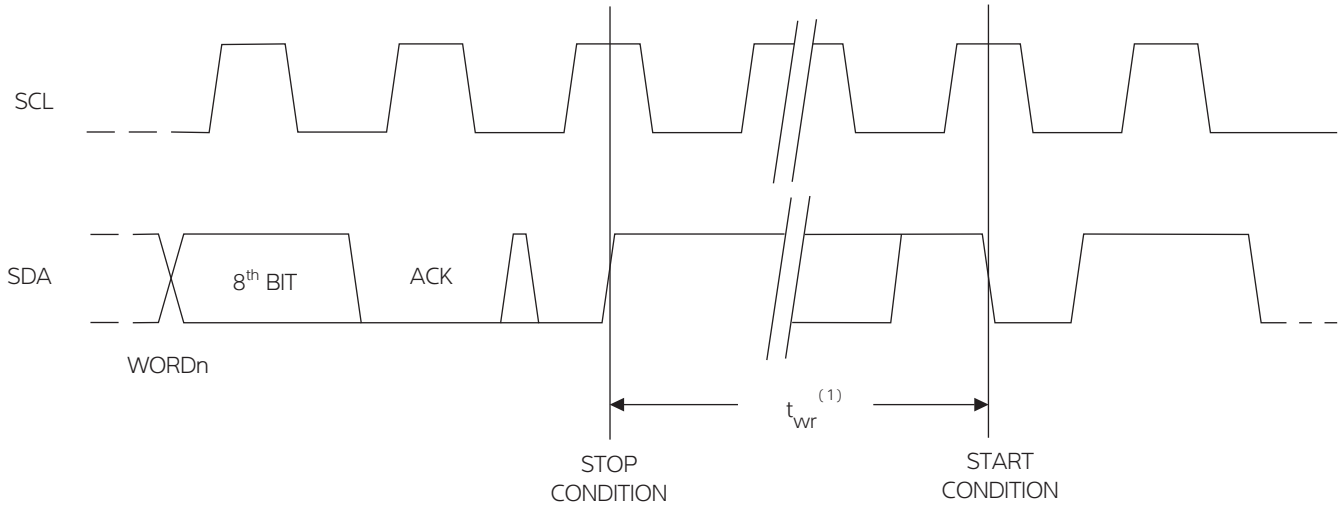
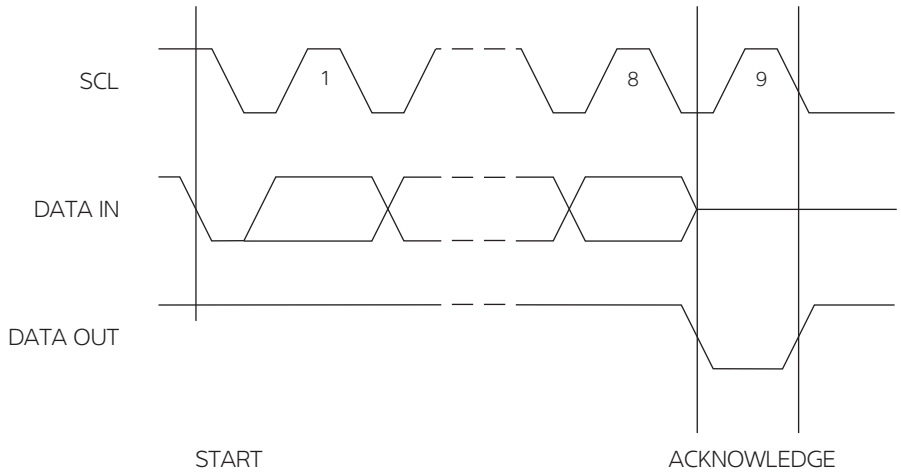


Figure 4-5. Write Cycle Timing



Note: 1. The write cycle time, t_{WR}, is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

Figure 4-6. Output Acknowledge



5. Device Addressing

The 128K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 5-1). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown. This is common to all two-wire EEPROM devices.

Figure 5-1. Device Address

1	0	1	0	A2	A1	A0	R/W

MSB LSB

The next three bits are the A2, A1, and A0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

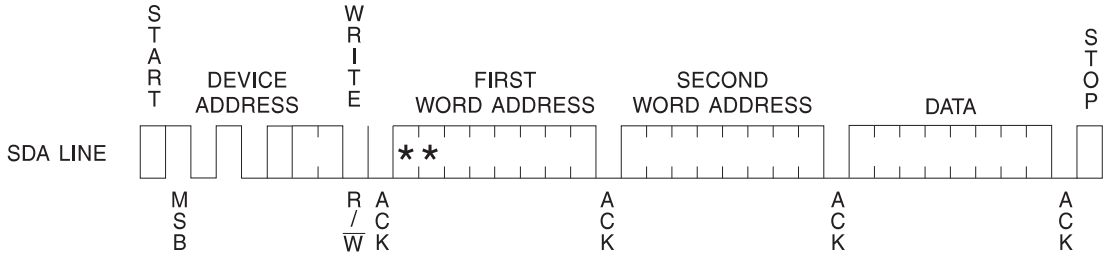
Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

DATA SECURITY: The Atmel AT24C128C has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at V_{CC}.

6. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, must then terminate the write sequence with a stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete (see Figure 6-1).

Figure 6-1. Byte Write

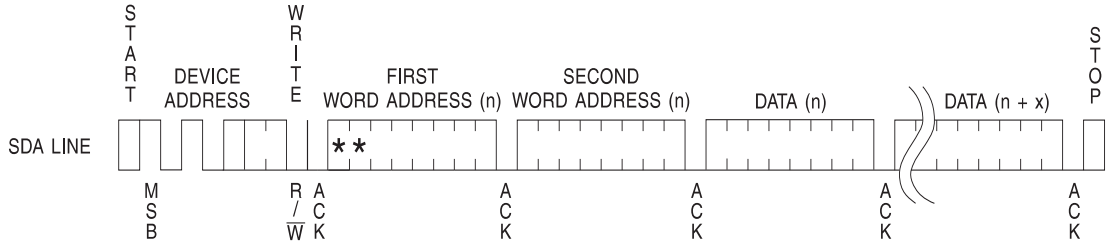


Note: * = Don't-care bit

PAGE WRITE: The 128K EEPROM is capable of 64-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6-2).

Figure 6-2. Page Write



Note: * = Don't-carebit

The lower six bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over," and previous data will be overwritten. The address roll over during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write select bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

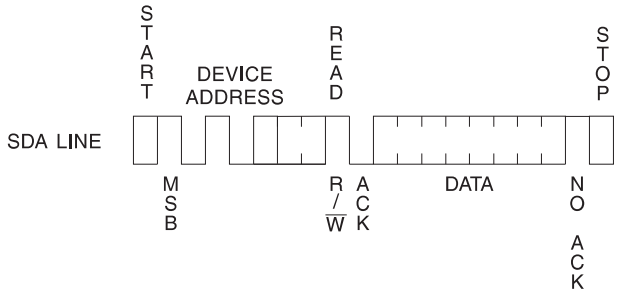
7. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read, and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read is from the last byte of the last memory page to the first byte of the first page.

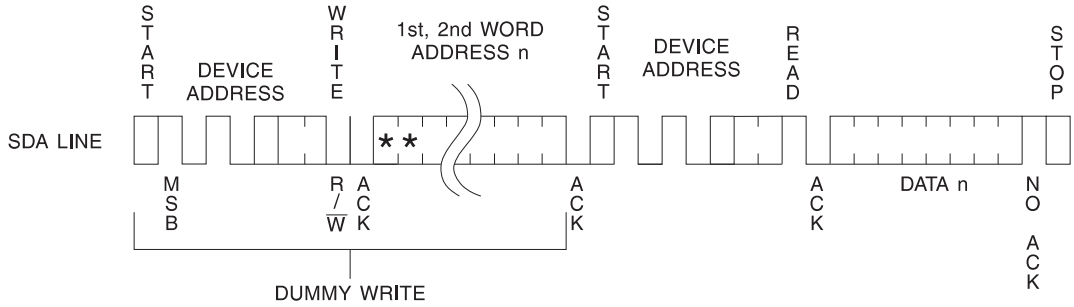
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero, but does generate a following stop condition (see Figure 7-1).

Figure 7-1. Current Address Read



RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero, but does generate a following stop condition (see Figure 7-2).

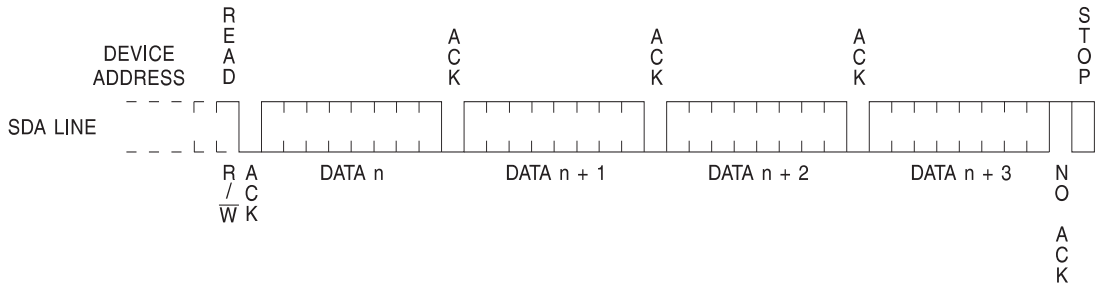
Figure 7-2. Random Read



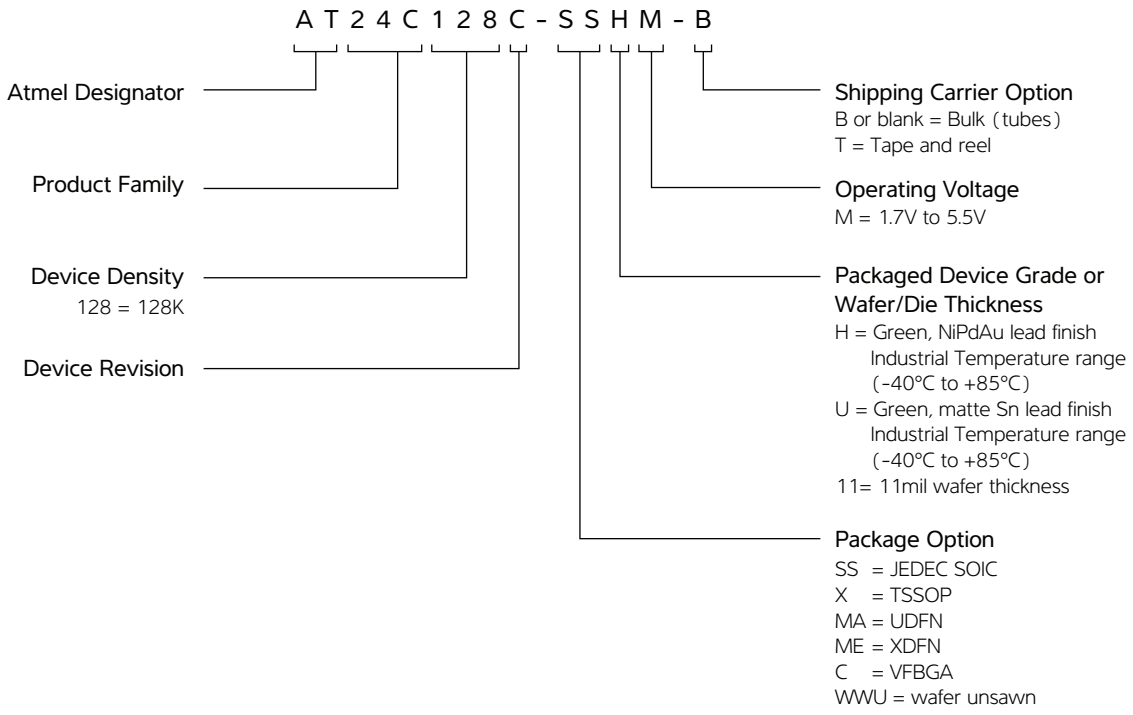
Note: * = Don't-carebit

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero, but does generate a following stop condition (see Figure 7-3).

Figure 7-3. Sequential Read



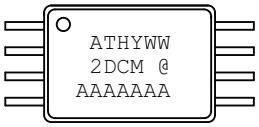
8. Ordering Code Detail



9. Atmel AT24C128C Part Markings

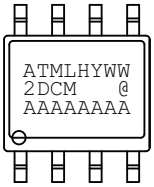
8 lead TSSOP

3 Rows
2 of 6 and 1 of 7 Characters



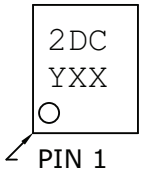
8 lead SOIC

3 Rows of 8 Characters



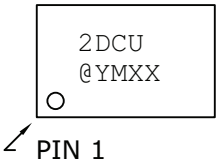
8 lead XDFN - 1.8x2.2mm

2 Rows of 3 Characters



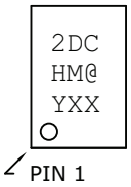
8-ball VFBGA - 2.35x3.73mm

2 Rows
1 of 4 and 1 of 5 Characters



8 lead UDFN -2.0x3.0mm

3 Rows of 3 Characters



Catalog Number: AT24C128C Catalog Truncation: 2DC

Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	Blank: 2.7v min
0: 2010 4: 2014	A: January	02: Week 2	D: 2.5v min
1: 2011 5: 2015	B: February	04: Week 4	L: 1.8v min
2: 2012 6: 2016	" " "	" " "	M: 1.7v min
3: 2013 7: 2017	L: December	52: Week 52	P: 1.5v min

Trace Code	Grade/Lead Finish Material
XX = Trace Code (ATMEL Lot Numbers to Correspond Code) (e.g. XX: AA, AB...YZ, ZZ)	U: Industrial/Matt Tin H: Industrial/NiPdAu
Lot Number AAAAAAA = ATMEL Wafer Lot Number	
Country of Assembly	ATMEL Truncation
@ = Country of Assembly B = PHILIPPINES W = THAILAND Q = MALAYSIA H,Y = CHINA	AT: ATMEL ATM: ATMEL ATML: ATMEL

12/21/10

Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE 24C128CSM, AT24C128C Standard Marking Information for Package Offering	DRAWING NO. 24C128CSM	REV. A

10. Ordering Codes

10.1 Atmel AT24C128C Ordering Information

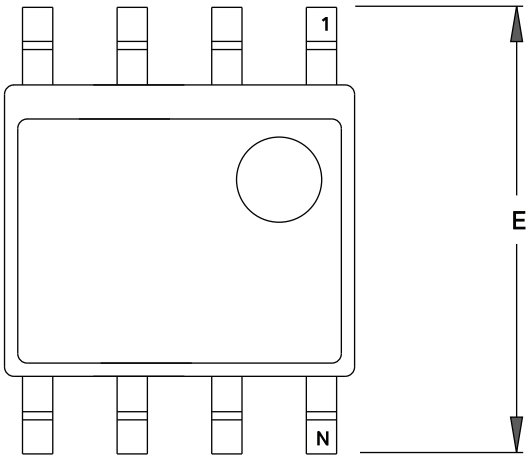
Ordering Code	Voltage	Package	Operation Range
AT24C128C-SSHM-B(1) (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	Lead-free/Halogen-free Industrial Temperature (–40°C to 85°C)
AT24C128C-SSHM-T(2) (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	
AT24C128C-XHM-B(1) (NiPdAu Lead Finish)	1.7V to 5.5V	8A2	
AT24C128C-XHM-T(2) (NiPdAu Lead Finish)	1.7V to 5.5V	8A2	
AT24C128C-MAHM-T(2) (NiPdAu Lead Finish)	1.7V to 5.5V	8Y6	
AT24C128C-MEHM-T(2) (NiPdAu Lead Finish)	1.7V to 5.5V	8ME1	
AT24C128C-CUM-T(2) (Matte Sn Finish)	1.7V to 5.5V	8U2-1	
AT24C128C-WWU11M(3)	1.7V to 5.5V	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes:
1. "-B" denotes bulk
2. "-T" denotes tape and reel. SOIC = 4K. UDFN, XDFN, and VFBGA = 5K/reel
3. For wafer sales, please contact Atmel sales

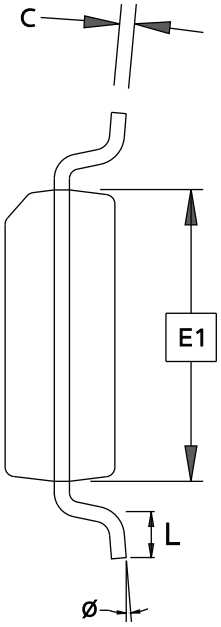
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing, Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch Ultra Thin Dual No Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body (XDFN)
8U2-1	8-ball, 2.35 x 3.73mm Body, 0.75mm Pitch, Small Die Ball Grid Array (VFBGA)

11. Packaging Information

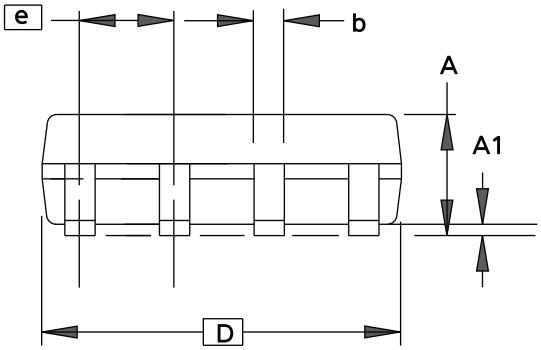
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

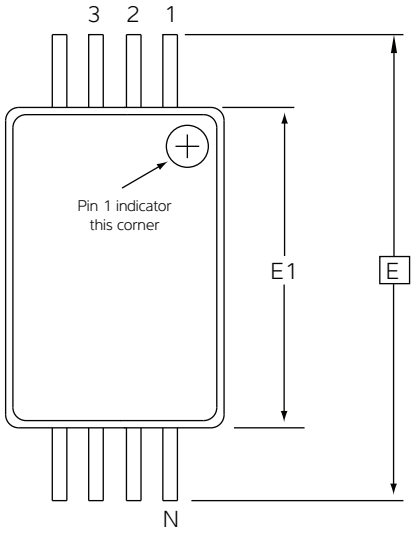
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

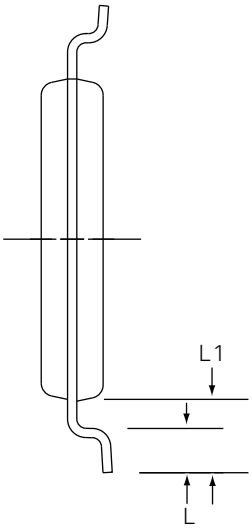
5/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8S1, 8-lead (0.150″ Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	F

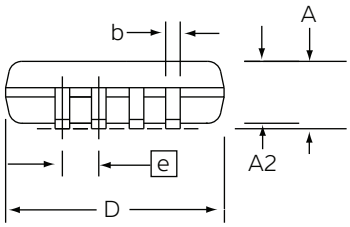
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

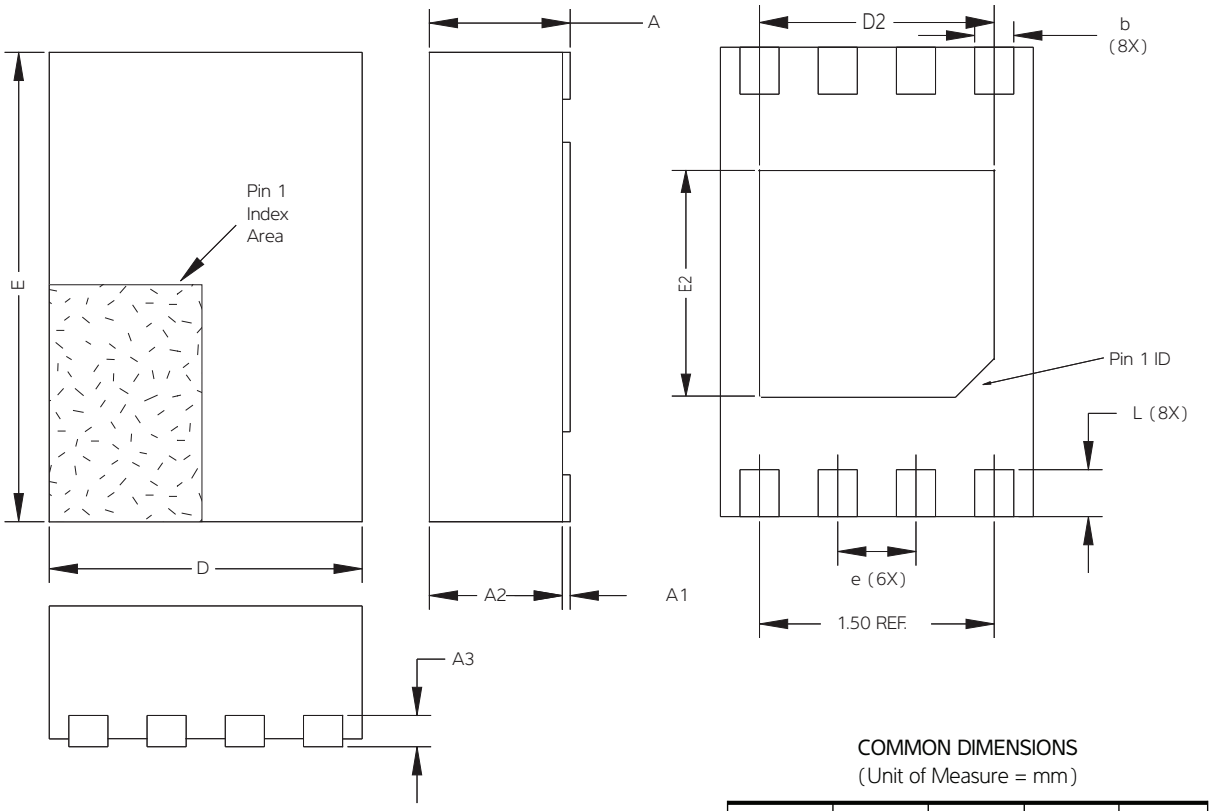
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/19/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8A2, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	E

8Y6 – UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

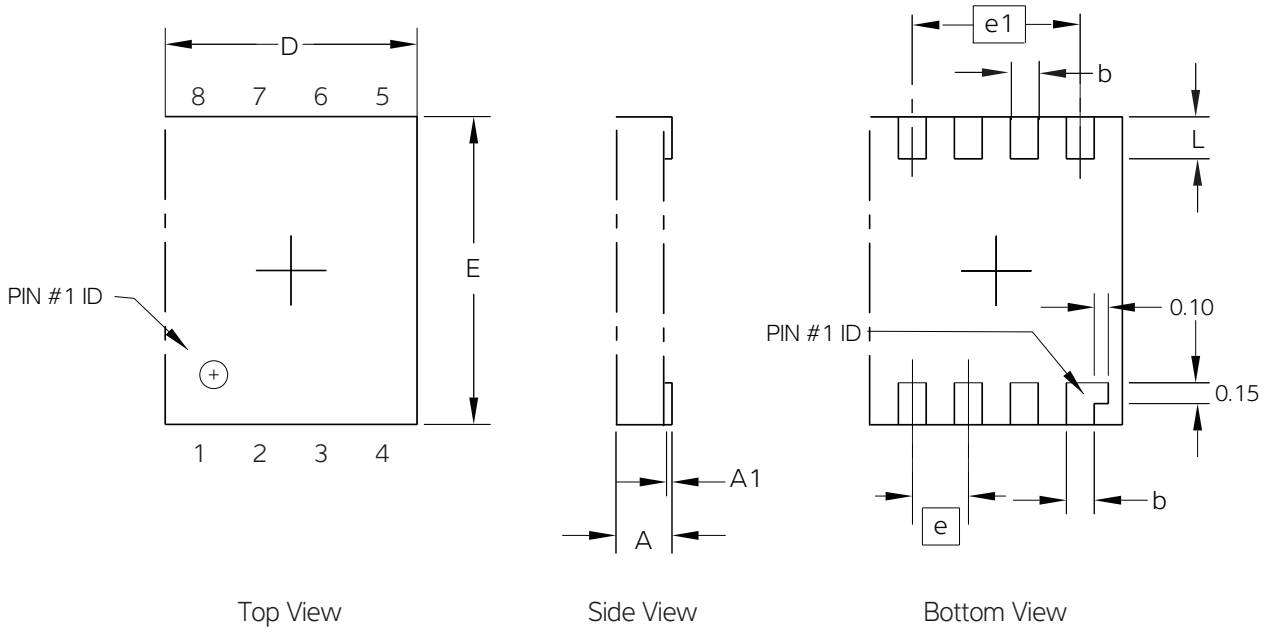
SYMBOL	MIN	NOM	MAX	NOTE
D	2.00 BSC			
E	3.00 BSC			
D2	1.40	1.50	1.60	
E2	–	–	1.40	
A	–	–	0.60	
A1	0.00	0.02	0.05	
A2	–	–	0.55	
A3	0.20 REF			
L	0.20	0.30	0.40	
e	0.50 BSC			
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

11/21/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8Y6, 8-lead, 2.0x3.0mm Body, 0.50mm Pitch, UltraThin Mini-MAP, Dual No Lead Package (Sawn) (UDFN)	YNZ	8Y6	E

8ME1 – XDFN



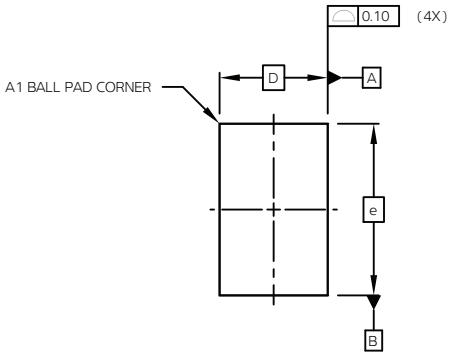
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

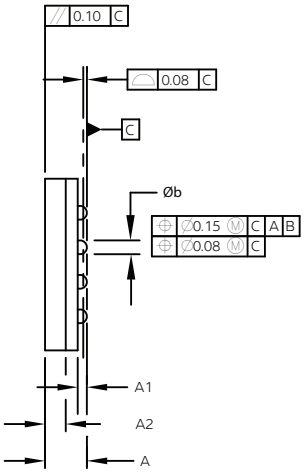
8/3/09

Package Drawing Contact: packagedrawings@atmel.com	TITLE 8ME1, 8-lead (1.80 x 2.20mm Body) Extra Thin DFN (XDFN)	GPC DTP	DRAWING NO. 8ME1	REV. A

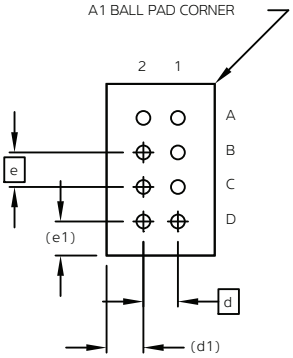
8U2-1 – VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW

8 SOLDER BALLS

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.81	0.91	1.00	
A1	0.15	0.20	0.25	
A2	0.40	0.45	0.50	
b	0.25	0.30	0.35	
D	2.35 BSC			
E	3.73 BSC			
e	0.75 BSC			
e1	0.74 REF			
d	0.75 BSC			
d1	0.80 REF			

Notes:

1. This drawing is for general information.
2. Dimension 'b' is measured at the maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

07/14/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8U2-1**, 8-ball, 2.35 x 3.73mm Body, 0.75mm pitch, VFBGA Package (dBGA2)	GWW	8U2-1	D

12. Revision History

Doc. Rev.	Date	Comments
8732A	01/2011	Initial document release

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
JAPAN
Tel: (+81) (3) 3523-3551
Fax: (+81) (3) 3523-7581

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