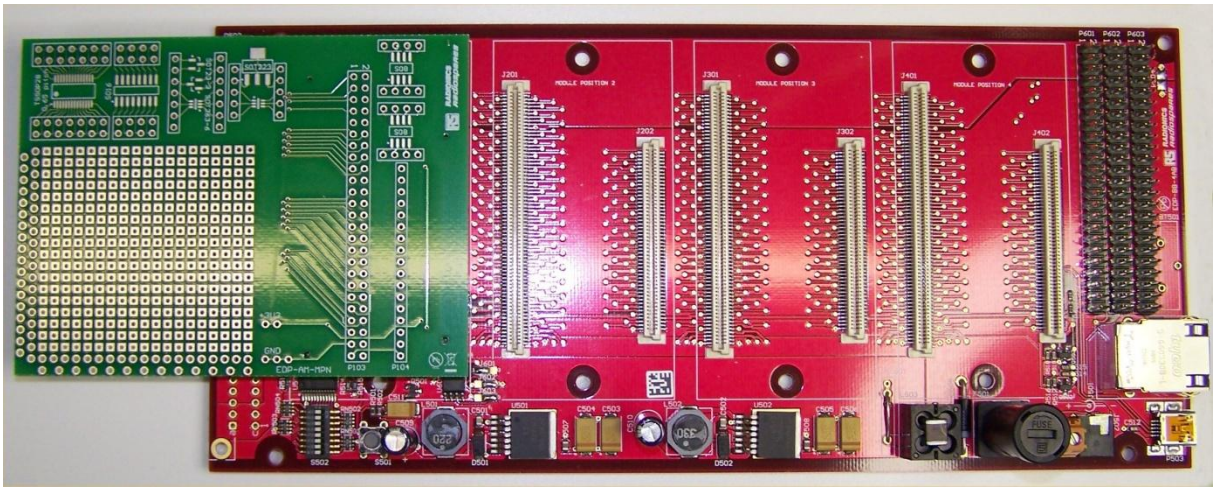
Embedded Development Platform

EDP-AM-MATRIX1 Prototyping Application Module User Manual

This document contains information on the EDP-AM-MATRIX1 prototyping module for the RS-EDP system.



Version v1.0, 18/11/2010

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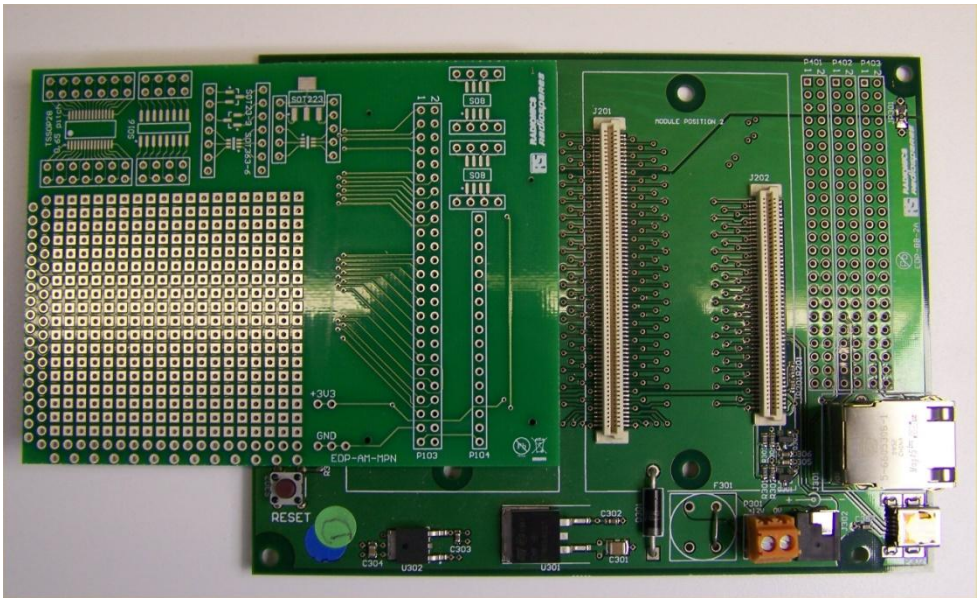
1. Introduction

This prototyping PCB is designed for use with the RS-EDP modular development platform.
The board has two surface mount connectors, which allow it to connect to an RS-EDP base board unit. The prototyping module is designed to fit both the two slot and the four sot base boards, utilising the left hand most slot. The board is designed to hang over the end of the base board and be large enough to accommodate the additional electronic components required for a user to complete a typical small to medium sized design.

Power from the base board is bought out on to the prototype area as well as a collection of useful signals that the user may require from the base board.

The PCB is designed as a consumable item and as such has minimal components mounted on it to help reduce the cost.



Picture of the 2 slot base board with the EDP-AM-MATRIX1 prototyping module fitted.

2. Features

The main features of the board are as follows:

- Compatible with both 2 slot and 4 slot base boards.
- 2 x SOT23-3 footprints.
- 2 x SOT363-6 footprints.
- 1 x SOT223 footprint.
- 1 x SOT26-6 footprint.
- 1 x TO252 footprint.
- 3 x SO8 footprints.
- 2 x TSSOP8 footprints.
- 1 x TSSOP28 footprint.
- 1 x wide TSSOP28 footprint.
- 1 x SO16 footprint.
- 1 x wide SO16 footprint.
- 20 x 19 through plated holes on a general purpose on 0.1 inch pitch matrix.
- An additional row of holes with larger holes and pads for use with power connectors.
- An additional row of holes on 0.15 inch pitch for use with D connector and wider pitch devices
- 12V, 12VGND, Vcc_CM, SGND, VAGND power pads.

- Access the various RS-EDP back plane signals which are bought out onto two through plated connectors one 25 x 2 way and one 17x1 way.

2.1 Prototype Area

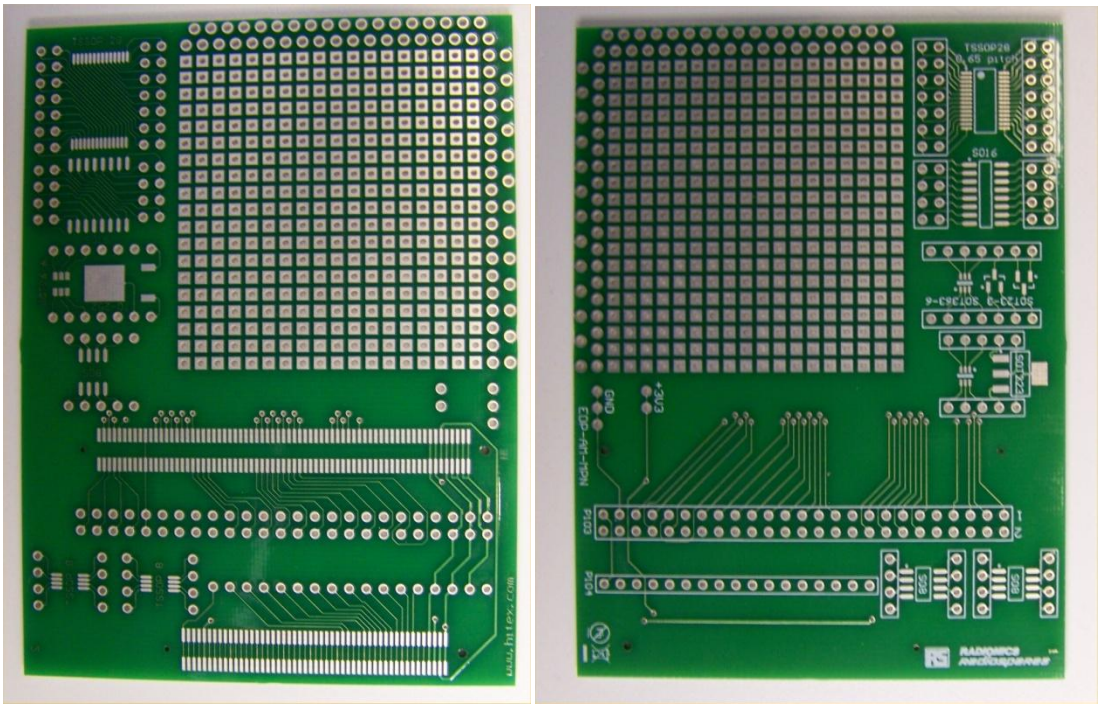
All of the SMT footprints can be soldered by hand when required. For best results, solder paste and a hot air gun can be used especially on the smaller pitch devices.

The board is populated with foot prints on both sides which are bought out to a common 0.1 inch pitch array of through-hole pads. This means an SO8 footprint for example has on the reverse a TSSOP8 footprint, which means the user has the option of either placing an SO8 device or a TSSOP8 but not both.

A similar arrangement is used with the TSSOP28 which has a standard width and a wide bodied variant on the opposite sides of the PCB. The user can use either one but not both at the same time. The larger TSSOP28 footprint can for example be also used to mount more TSSOP8 if this is required in the system.

There is a pretty good mix of footprints, which allow for D connectors, power connector, Pentawatt packages and standard DIP IC's to be placed on the board, along with the more tricky SMT footprints.

The matrix area is primarily designed for through-hole parts and a square pad shape has been used to facilitate solder bridging between the pads.



Pictures of the top side and reverse sides of the blank PCB. (Note: Connectors not fitted)

3. Power Supply

The power for the prototyping board is bought up from the base board unit. You should refer to the user manual for both the two slot and four slot boards to see if these boards are capable of powering your application. Remember the two slot board PSU is linear so make sure you do not overload it. The four slot base board is able to deliver a much higher power as it uses switching regulators rather than linear ones.

In addition to the 12V supply the user has access to the Vcc_CM signal which will be either 3.3V or 5.0V depending upon the CPU module fitted. The CPU module dictates this voltage.

4. Connectivity to the Back Plane

The signals that are available to the user are as follows:

4.1 Connector P103 (25x2)

Pin	Back Plane Signal
1	AN0
2	AN1
3	AN2
4	AN3
5	AN4
6	AN5
7	AN6
8	AN7
9	VAGND
10	VAGND
11	GPIO2_MCIDAT0
12	GPIO4_MCIDAT1
13	GPIO6_MCIDAT2
14	GPIO8_MCIDAT3
15	GPIO10_MCICLK
16	GPIO12_MCICMD
17	GPIO14_MCIPWR
18	IRQ_GPIO16_CNTRL_I2C_INT
19	CPU_DACO0_GPIO17
20	CPU_DACO1_GPIO19
21	EVG0_GPIO40
22	EVM0_GPIO21
23	EVG1_GPIO42
24	EVM1_GPIO23
25	EVG2_GPIO44
26	EVM2_GPIO41_CAPADC
27	EVG3_GPIO46
28	EVM3_GPIO43
29	EVG4_GPIO48
30	EVM4_GPIO45
31	EVG5_GPIO50
32	EVM5_GPIO47
33	EVG6_GPIO52
34	EVM6_GPIO49
35	EVG7_GPIO54
36	EVM7_GPIO51
37	EVG8_GPIO56
38	EVM8_GPIO53
39	EVG9_GPIO57
40	EVM9_GPIO55
41	ASC0_RX_TTL
42	ASC0_TX_TTL
43	ASC1_RX_TTL
44	ASC1_TX_TTL
45	ASC1_RX_TTL_ASC0_DSR

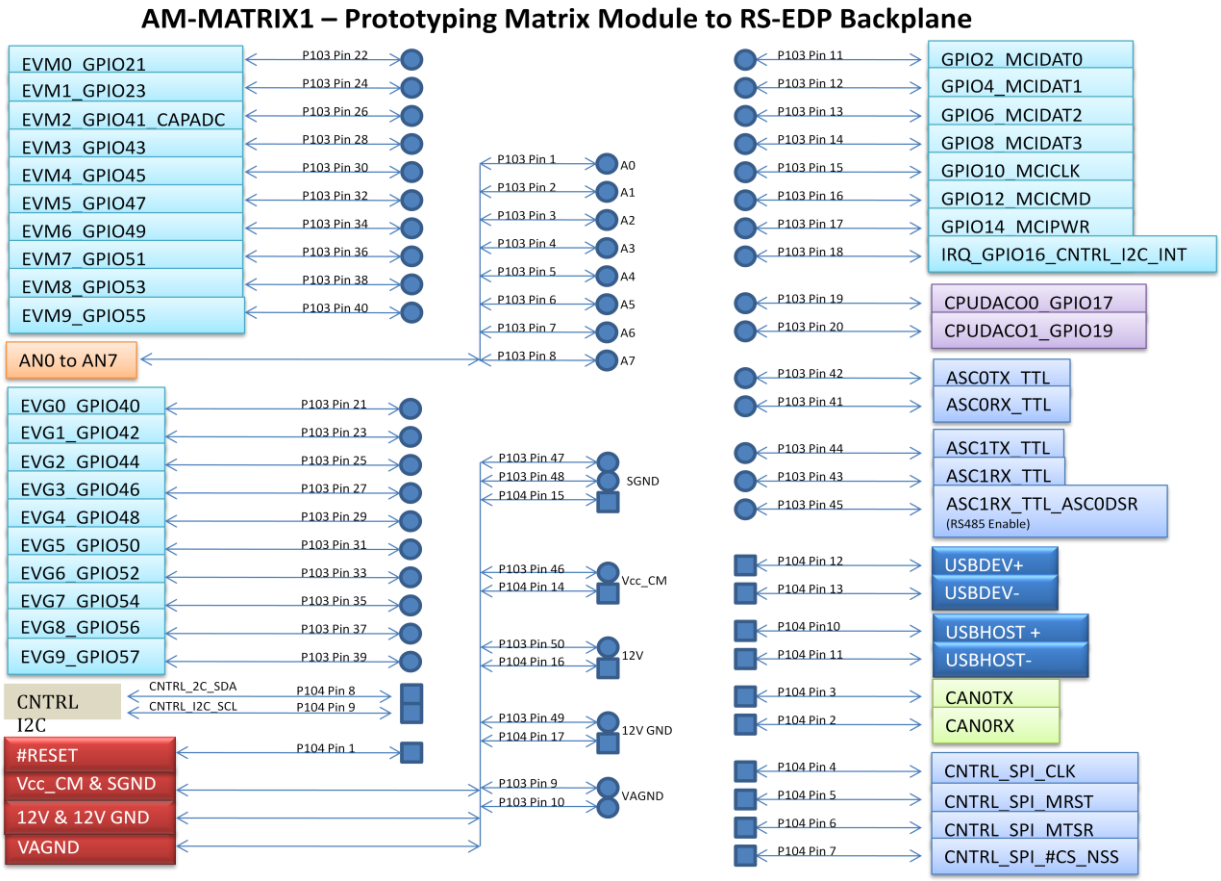
46	VCC_CM
47	SGND
48	SGND
49	12VGND
50	12V

4.2 Connector P104 (17x1)

Pin	Back Plane Signal
1	#RESET
2	CAN0_RX
3	CAN0_TX
4	CNTRL_SPICLK
5	CNTRL_SPIMRST
6	CNTRL_SPIMTSR
7	CNTRL_SPI#CS_NSS
8	CNTRL_I2C_SDA
9	CNTRL_I2C_SCL
10	USB_HOST_D+
11	USB_HOST_D-
12	USB_DEV_D+
13	USB_DEV_D-
14	VCC_CM
15	SGND
16	12V
17	12VGND

5. Mapping Aid

A separate mapping aid exists for each CPU and Application Module. The brief details are detailed below for this item.



Note: The square pad shapes indicate the single row connector (P104), whilst the round pad shape indicates the double row connector (P103).

6. Complete Back Plane Signal Listing

Base Board Signal Name	EDPCON1	EDPCON2	Base Board Break Out Connector	Base Board Connector Pin
#CS0		53 & 54		
#CS1		55 & 56		
#CS2		57 & 58		
#CS3		59 & 60		
#PSEN		51 & 52		
#RD		45 & 46		
#RESIN		1 & 2	P603	26
#RESOUT		3 & 4	P603	27
#WR		47 & 48		
#WRH		49 & 50		
12V	133		P603	47
12V	134		P603	47
12V	135		P603	47
12V	136		P603	47
12V GND	137		P603	48

12V GND	138		P603	48
12V GND	139		P603	48
12V GND	140		P603	48
3.3V	127		P603	44
3.3V	128		P603	44
3.3V		95 & 96	P603	44
3V BAT	124		P603	42
5.0V	129		P603	45
5.0V	130		P603	45
5.0V		97 & 98	P603	45
A0_AD0		41 & 42		
A1_AD1		39 & 40		
A2_AD2		37 & 38		
A3_AD3		35 & 36		
A4_AD4		33 & 34		
A5_AD5		31 & 32		
A6_AD6		29 & 30		
A7_AD7		27 & 28		
A8_AD8		25 & 26		
A9_AD9		23 & 24		
A10_AD10		21 & 22		
A11_AD11		19 & 20		
A12_AD12		17 & 18		
A13_AD13		15 & 16		
A14_AD14		13 & 14		
A15_AD15		11 & 12		
ALE		43 & 44		
AN_REF	1		P601	6
AN0	3		P603	2
AN1	4		P603	6
AN2	5		P603	1
AN3	6		P603	5
AN4	7		P602	2
AN5	8		P602	4
AN6	9		P602	1
AN7	10		P602	3
AN8	11		P601	2
AN9	12		P601	4
AN10	13		P601	1
AN11	14		P601	3
AN12	15		P603	4
AN13	16		P602	6
AN14	17		P603	3
AN15	18		P602	5
ASC0_RX_TTL	89		P602	30
ASC0_TX_TTL	91		P602	31
ASC1_RX_TTL	93		P602	32
ASC1_RX_TTL_ASC0_DSR	99		P602	35
ASC1_TX_TTL	95		P602	33
ASC1_TX_TTL_ASC0_DTR	97		P602	34
CAN0_RX		61 & 62		
CAN0_TX		63 &64		
CAN1_RX	121		P602	46
CAN1_TX	123		P602	47
CANH0		89 & 90	P603	40
CANL0		91 & 92	P603	41
CNTRL_I2C_SCL		79 & 80	P603	35
CNTRL_I2C_SDA		77 & 78	P603	34
CNTRL_SPI_#CS_NSS		75 & 76	P603	33
CNTRL_SPI_CLK		69 & 70	P603	30
CNTRL_SPI_MRST		71 & 72	P603	31

CNTRL_SPI_MTSR		73 & 74	P603	32
CPU_DACO0_GPIO17	38		P603	7
CPU_DACO1_GPIO19	40		P601	7
EMG_TRAP	114		P601	44
ETH_LNK_LED	111		P602	41
ETH_RX-	109		P602	40
ETH_RX_LED	113		P602	42
ETH_RX+	107		P602	39
ETH_SPD_LED	115		P602	43
ETH_TX-	105		P602	38
ETH_TX+	103		P602	37
EVG0_GPIO40	61		P602	16
EVG1_GPIO42	63		P602	17
EVG2_GPIO44	65		P602	18
EVG3_GPIO46	67		P602	19
EVG4_GPIO48	69		P602	20
EVG5_GPIO50	71		P602	21
EVG6_GPIO52	73		P602	22
EVG7_GPIO54	75		P602	23
EVG8_GPIO56	77		P602	24
EVG9_GPIO57	78		P601	26
EVG10_GPIO58	79		P602	25
EVG11_GPIO59	80		P601	27
EVG12_GPIO60	81		P602	26
EVG13_GPIO61	82		P601	28
EVG14_GPIO62	83		P602	27
EVG15_GPIO63	84		P601	29
EVG16_GPIO64	85		P602	28
EVG17_GPIO65	86		P601	30
EVG18_GPIO66	87		P602	29
EVG19_GPIO67	88		P601	31
EVG20_GPIO69_ASCO_RTS	92		P601	33
EVM0_GPIO21	42		P601	8
EVM1_GPIO23	44		P601	9
EVM2_GPIO41_CAPADC	62		P601	18
EVM3_GPIO43	64		P601	19
EVM4_GPIO45	66		P601	20
EVM5_GPIO47	68		P601	21
EVM6_GPIO49	70		P601	22
EVM7_GPIO51	72		P601	23
EVM8_GPIO53	74		P601	24
EVM9_GPIO55	76		P601	25
EVM10_GPIO68_ASCO_CTS	90		P601	32
GPIO0	21		P603	13
GPIO1	22		P603	15
GPIO2_MCI_DAT0	23		P603	14
GPIO3	24		P603	16
GPIO4_MCI_DAT1	25		P603	17
GPIO5_I2S_TX_WS	26		P603	19
GPIO6_MCI_DAT2	27		P603	18
GPIO7_I2S_RX_CLK	28		P603	20
GPIO8_MCI_DAT3	29		P603	22
GPIO9_I2S_RX_WS	30		P603	21
GPIO10_MCI_CLK	31		P603	23
GPIO11_I2S_RX_SDA	32		P603	24
GPIO12_MCI_CMD	33			
GPIO13_I2S_TX_CLK	34		P603	25
GPIO14_MCI_PWR	35		P603	12
GPIO15_I2S_TX_SDA	36		P603	8
GPIO24_AD7	45		P602	8
GPIO25_AD15	46		P601	10

GPIO26_AD6	47		P602	9
GPIO27_AD14	48		P601	11
GPIO28_AD5	49		P602	10
GPIO29_AD13	50		P601	12
GPIO30_AD4	51		P602	11
GPIO31_ADI2	52		P601	13
GPIO32_AD3	53		P602	12
GPIO33_AD11	54		P601	14
GPIO34_AD2	55		P602	13
GPIO35_AD10	56		P601	15
GPIO36_AD1	57		P602	14
GPIO37_AD9	58		P601	16
GPIO38_AD0	59		P602	15
GPIO39_AD8	60		P601	17
I2C_GEN0_SCL		7 & 8	P603	29
I2C_GEN0_SDA		5 & 6	P603	28
I2C_GEN1_SCL	119		P602	45
I2C_GEN1_SDA	117		P602	44
IRQ_GPIO16_CNTRL_I2C_INT	37		P603	11
IRQ_GPIO18_I2C_GEN0_INT	39		P603	10
IRQ_GPIO20_I2C_GEN1_INT	41		P603	9
IRQ_GPIO22_I2C_INT	43		P602	7
MOTOR_TCO_FB	122		P601	48
MOTORH0_ENC0	116		P601	45
MOTORH1_ENC1	118		P601	46
MOTORH2_ENC2	120		P601	47
MOTORP0H	102		P601	38
MOTORP0L	100		P601	37
MOTORP1H	106		P601	40
MOTORP1L	104		P601	39
MOTORP2H	110		P601	42
MOTORP2L	108		P601	41
MOTORPWM	112		P601	43
SGND	131		P603	46
SGND	132		P603	46
SGND		9 & 10	P603	46
SGND		99 & 100	P603	46
SPI_SSC_#CS_NSS	101		P602	36
SPI_SSC_CLK	98		P601	36
SPI_SSC_MRST_MISO	94		P601	34
SPI_SSC_MTSR_MOSI	96		P601	35
USB_DEBUG_D-		67 & 68		
USB_DEBUG_D+		65 & 66		
USB_DEV_D-		87 & 88	P603	39
USB_DEV_D+		85 & 86	P603	38
USB_HOST_D-		83 & 84	P603	37
USB_HOST_D+		81 & 82	P603	36
VAGND	19		P601	5
VAGND	20		P601	5
Vcc_CM	125		P603	43
Vcc_CM	126		P603	43
Vcc_CM		93 & 94	P603	43

7. Circuit Schematics and Overlay

The schematic diagram and components overlay are detailed at the back of this manual.

PROTOTYPING AREA

EXTRA SMT FOOTPRINTS ON PCB

SOT23-3 (x2)
SOT363-6 (x2)
SOT223
SOT26-6
TO252
SO8 (x3)
TSSOP8 (x2)
TSSOP28 (0.65MM PITCH, 4.4MM WIDE BODY)
TSSOP28 (0.65MM PITCH, 12.6MM WIDE BODY)
SO16 (PITCH 1.27MM, 3.9MM WIDE BODY)
SO16 (PITCH 1.27MM, 7.5MM WIDE BODY)

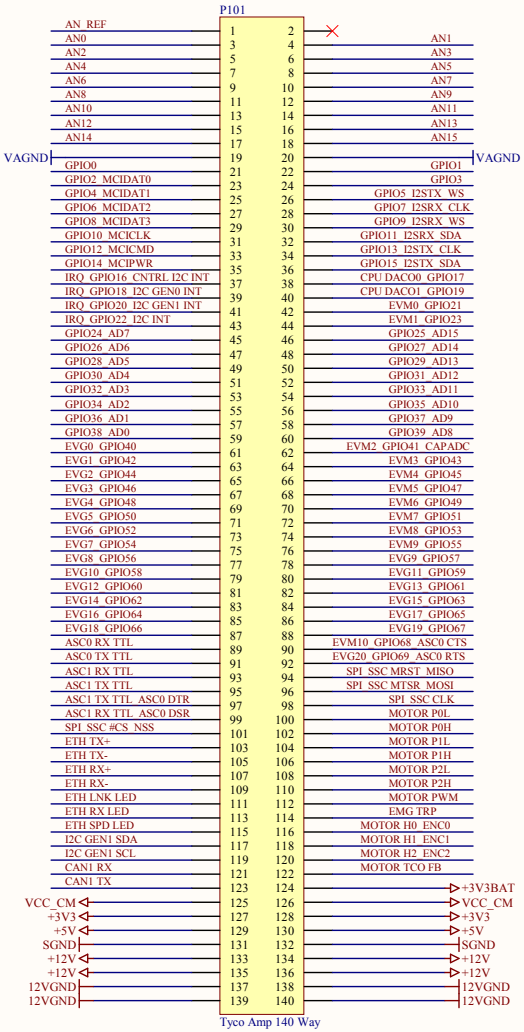
All SMT footprints fan out to 0.1" pitch holes
for easy connection.

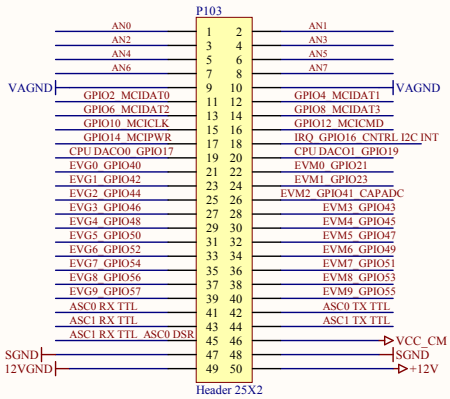
2.54mm grid prototyping area for through hole components.
Includes offset 1.27mm row along one side for D-Type
connectors and other FETS etc. requiring it.

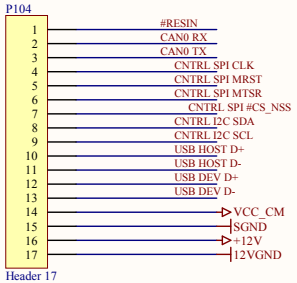
3.81mm pitch row for screw terminals.

3.2mm mounting holes on each corner.

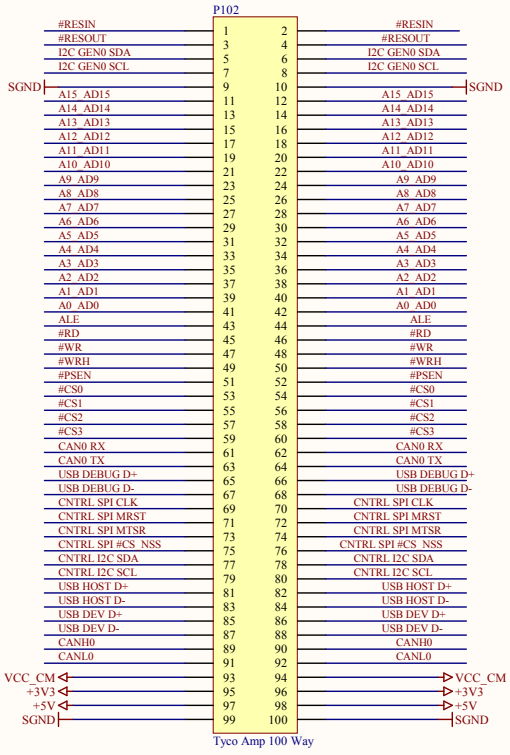
EDPCON1 IO Connector



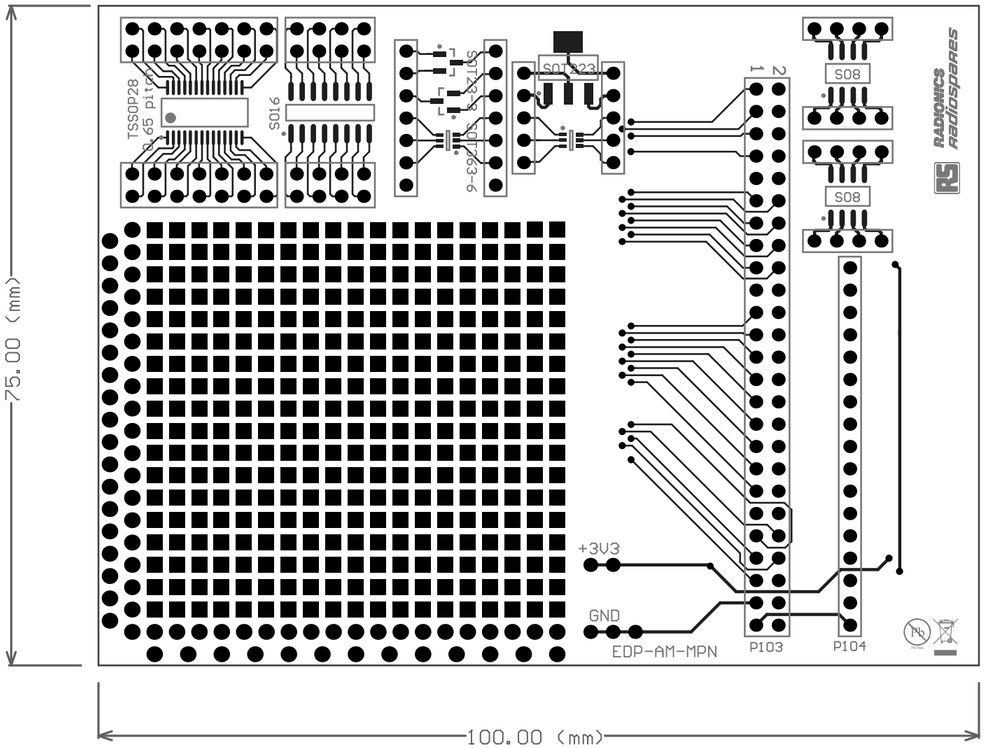




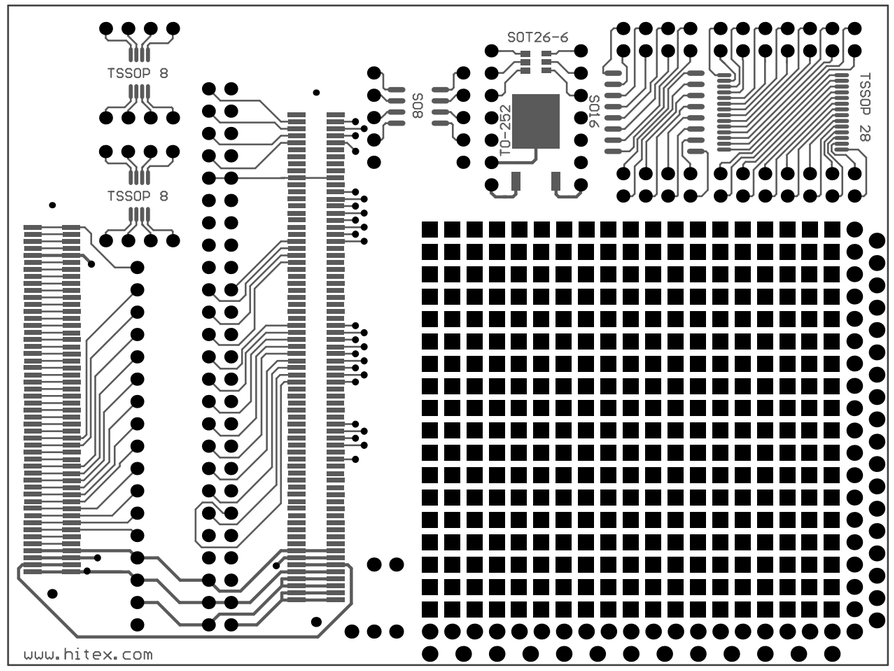
EDPCON2 Bus/Control Connector



Checked By:	Title: EDP-AM-MPN		Hitex (UK) Ltd. Sir William Lyons Road University of Warwick Science Park Coventry
Approved By:	Size: A3	Number: 4204.30303	Revision: 0.1
	Date: 23/09/2010	(c) Hitex (UK) Ltd.	Sheet1 of 1
	File: D:\PCB Designs\DXP\EDP-AM-MPN\MPN Matrix.SchDoc		Author: A.Davison



HITEX (UK) LTD. Sir William Lyons Road Coventry CV4 7EZ ENGLAND	ENGINEER: A.Davison	TITLE: EDP-AM-MPN	
	PCB DESIGNER: A.Davison		
	DATE: 28/10/2010	PART NO.: EDP-AM-MPN	REV: 1
	FILE NAME: EDP-AM-MPN_1.PcbDoc	DWG NO: 4204.30303	SCALE:



HITEX (UK) LTD. Sir William Lyons Road Coventry CV4 7EZ ENGLAND	ENGINEER: A.Davison	TITLE: EDP-AM-MPN	
	PCB DESIGNER: A.Davison		
	DATE: 28/10/2010	PART NO.: EDP-AM-MPN	REV: 1
	FILE NAME: EDP-AM-MPN_1.PcbDoc	DWG NO: 4204.30303	SCALE: