CCFL/LCD Contrast Switching Regulators

FEATURES

- **Wide Input Voltage Range: 3V to 30V**
- Low Quiescent Current
- High Switching Frequency: 200kHz
- CCFL Switch: 1.25A, LCD Switch: 625mA
- **Grounded or Floating Lamp Configurations**
- **Open-Lamp Protection**
- Positive or Negative Contrast Capability

APPLICATIONS

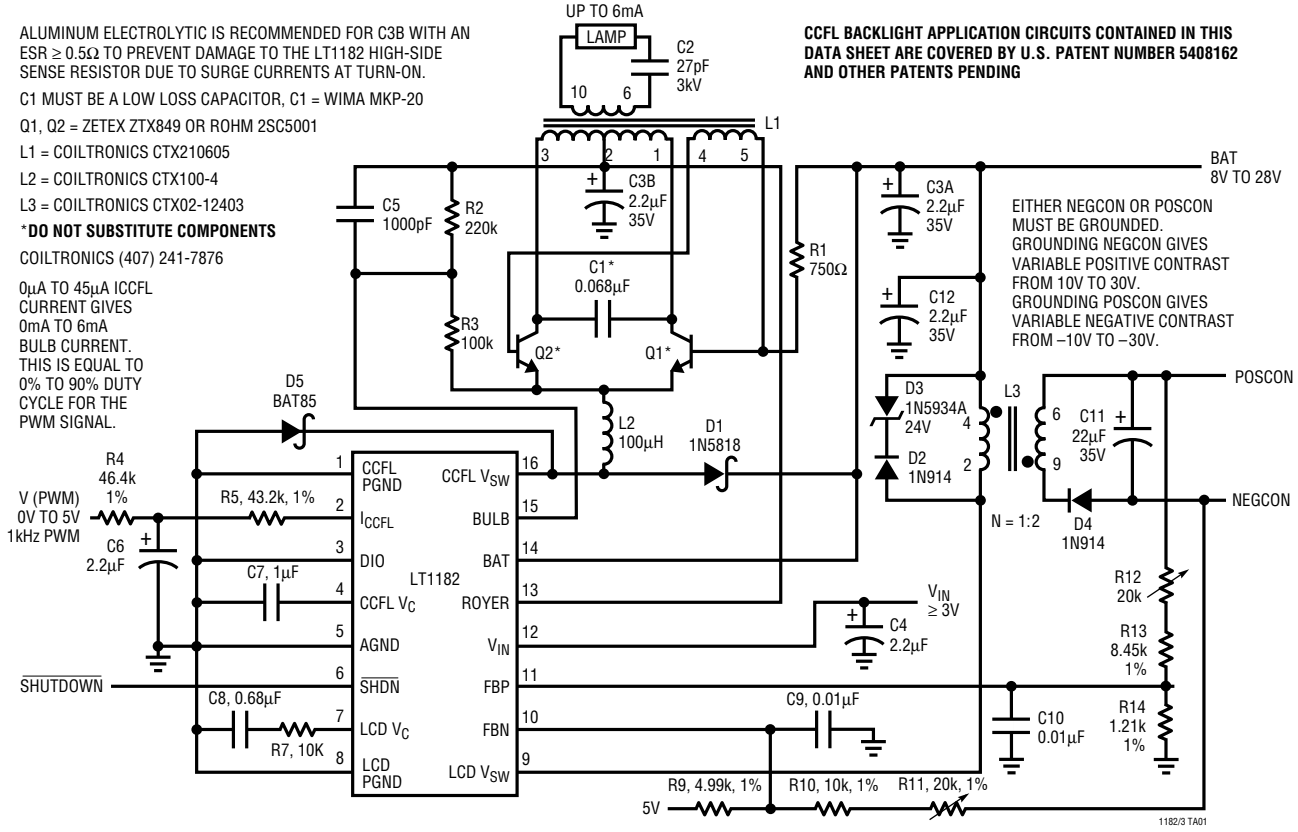
- Notebook and Palmtop Computers
- Portable Instruments
- Automotive Displays
- Retail Terminals

DESCRIPTION

The LT®1182/LT1183 are dual current mode switching regulators that provide the control function for Cold Cathode Fluorescent Lighting (CCFL) and Liquid Crystal Display (LCD) Contrast. The LT1184/LT1184F provide only the CCFL function. The ICs include high current, high efficiency switches, an oscillator, a reference, output drive logic, control blocks and protection circuitry. The LT1182 permits positive or negative voltage LCD contrast operation. The LT1183 permits unipolar contrast operation and pins out an internal reference. The LT1182/LT1183 support grounded and floating lamp configurations. The LT1184F supports grounded and floating lamp configurations. The LT1184 supports only grounded lamp configurations. The

TYPICAL APPLICATION

90% Efficient Floating CCFL Configuration with Dual Polarity LCD Contrast



DESCRIPTION

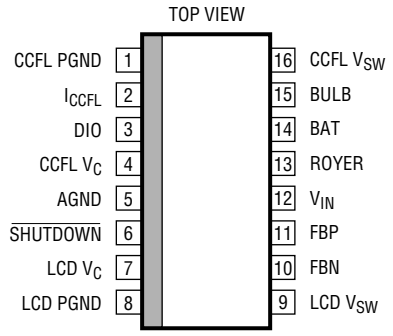
LT1184/LT1184F pin out the reference for simplified programming of lamp current.

The LT1182/LT1183/LT1184/LT1184F operate with input supply voltages from 3V to 30V. The ICs also have a battery supply voltage pin that operates from 4.5V to 30V. The LT1182/LT1183 draw 9mA typical quiescent current while the LT1184/LT1184F draw 6mA typical quiescent current. An active low shutdown pin typically reduces total supply current to 35μA for standby operation. A 200kHz switching frequency minimizes the size of required magnetic components. The use of current mode switching techniques with cycle-by-cycle limiting gives high reliability and simple loop frequency compensation. The LT1182/LT1183/LT1184/LT1184F are all available in 16-pin narrow SO packages.

ABSOLUTE MAXIMUM RATINGS

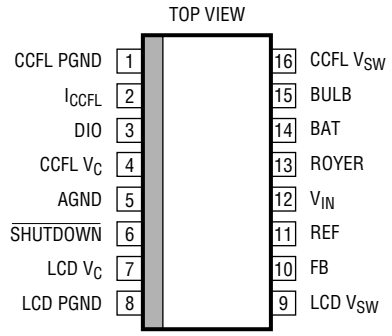
V_{IN}, BAT, Royer, Bulb 30V
CCFL V_{SW}, LCD V_{SW} 60V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current (Peak, < 100ms) 100mA
LT1182: FBP, FBN, LT1183: FB Pin Current ..... ±2mA
LT1183/LT1184/1184F: REF Pin Source Current 1mA
Junction Temperature (Note 1) ..... 100°C
Operating Ambient Temperature Range ..... 0°C to 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



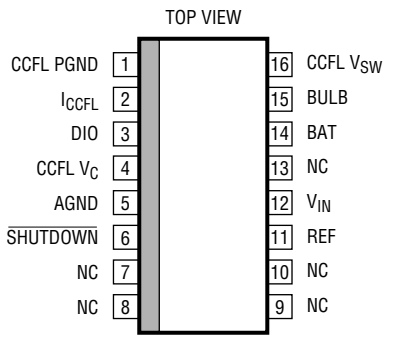
S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1182CS



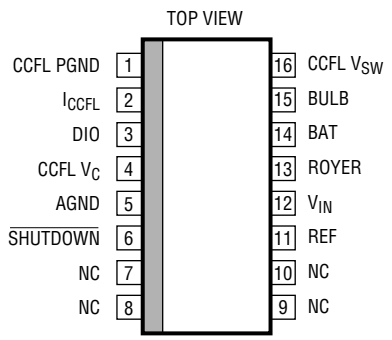
S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1183CS



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1184CS



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1184FCS

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, I_{CCFL} = $\overline{SHUTDOWN}$ = CCFL V_{SW} = Open, DIO = GND, CCFL V_C = 0.5V, (LT1182/LT1183) LCD V_C = 0.5V, LCD V_{SW} = Open, (LT1182) FBN = FBP = GND, (LT1183) FB = GND, (LT1183/LT1184/LT1184F) REF = Open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	LT1182/LT1183: 3V ≤ V_{IN} ≤ 30V	●		9	14	mA
		LT1184/LT1184F: 3V ≤ V_{IN} ≤ 30V	●		6	9.5	mA
$I_{\overline{SHDN}}$	$\overline{SHUTDOWN}$ Supply Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = LCD V_C = Open (Note 2)			35	70	µA
	$\overline{SHUTDOWN}$ Input Bias Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = LCD V_C = Open			3	6	µA
	$\overline{SHUTDOWN}$ Threshold Voltage		●	0.6	0.85	1.2	V
f	Switching Frequency	Measured at CCFL V_{SW} and LCD V_{SW}, I_{SW} = 50mA,		175	200	225	kHz
		I_{CCFL} = 100µA, CCFL V_C = Open, (LT1182) FBN = FBP = 1V, (LT1183) FB = 1V, (LT1182/LT1183) LCD V_C = Open	●	160	200	240	kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW} and LCD V_{SW}		80	85		%
			●	75	85		%
BV	Switch Breakdown Voltage	Measured at CCFL V_{SW} and LCD V_{SW}		60	70		V
	Switch Leakage Current	V_{SW} = 12V, Measured at CCFL V_{SW} and LCD V_{SW}				20	µA
		V_{SW} = 30V, Measured at CCFL V_{SW} and LCD V_{SW}				40	µA
	I_{CCFL} Summing Voltage	3V ≤ V_{IN} ≤ 30V, Measured on LT1182/LT1183		0.41	0.45	0.49	V
			●	0.37	0.45	0.54	V
		3V ≤ V_{IN} ≤ 30V, Measured on LT1184/LT1184F		0.425	0.465	0.505	V
			●	0.385	0.465	0.555	V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			5	15	mV
	CCFL V_C Offset Sink Current	CCFL V_C = 1.5V, Positive Current Measured into Pin		–5	5	15	µA
	ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 25µA, 50µA, 75µA, 100µA, CCFL V_C = 1.5V	●	4.70	4.95	5.20	µA/µA
	CCFL V_C to DIO Current Servo Ratio	DIO = 5mA out of Pin, Measure I_{VC} at CCFL V_C = 1.5V	●	94	99	104	µA/mA
	CCFL V_C Low Clamp Voltage	V_{BAT} – V_{BULB} = Bulb Protect Servo Voltage	●		0.1	0.3	V
	CCFL V_C High Clamp Voltage	I_{CCFL} = 100µA	●	1.7	2.1	2.4	V
	CCFL V_C Switching Threshold	CCFL V_{SW} DC = 0%	●	0.6	0.95	1.3	V
	CCFL High-Side Sense Servo Current	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V	●	0.93	1.00	1.07	A
	CCFL High-Side Sense Servo Current Line Regulation	BAT = 5V to 30V, I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V			0.1	0.16	%/V
	CCFL High-Side Sense Supply Current	Current Measured into BAT and Royer Pins	●	50	100	150	µA
	Bulb Protect Servo Voltage	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V, Servo Voltage Measured Between BAT and Bulb Pins	●	6.5	7.0	7.5	V
	Bulb Input Bias Current	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V			5	9	µA
I_{LIM1}	CCFL Switch Current Limit	Duty Cycle = 50%	●	1.25	1.9	3.0	A
		Duty Cycle = 75% (Note 3)	●	0.9	1.6	2.6	A
V_{SAT1}	CCFL Switch On-Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW1}}$	Supply Current Increase During CCFL Switch On-Time	CCFL I_{SW} = 1A			20	30	mA/A
V_{REF}	Reference Voltage	Measured at REF (Pin 11) on LT1183/LT1184/LT1184F		1.224	1.244	1.264	V
			●	1.214	1.244	1.274	V
	Reference Output Impedance	Measured at REF (Pin 11) on LT1183	●	20	45	70	Ω
		Measured at REF (Pin 11) on LT1184/LT1184F	●	5	15	30	Ω

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, I_{CCFL} = $\overline{SHUTDOWN}$ = CCFL V_{SW} = Open, DIO = GND, CCFL V_C = 0.5V, (LT1182/LT1183) LCD V_C = 0.5V, LCD V_{SW} = Open, (LT1182) FBN = FBP = GND, (LT1183) FB = GND, (LT1183/LT1184/LT1184F) REF = Open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{REF} – I_{CCFL} Summing Voltage	Measured on LT1183		0.760	0.795	0.830	V
			●	0.725	0.795	0.865	V
	V_{REF} – I_{CCFL} Summing Voltage	Measured on LT1184/LT1184F		0.740	0.775	0.810	V
			●	0.705	0.775	0.845	V
REF1	LCD FBP/FB Reference Voltage	LT1182: Measured at FBP Pin, FBN = 1V, LCD V_C = 0.8V		1.224	1.244	1.264	V
		LT1183: Measured at FB Pin, LCD V_C = 0.8V	●	1.214	1.244	1.274	V
	REF1 Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V, LCD V_C = 0.8V	●		0.01	0.03	%/V
	FBP/FB Input Bias Current	LT1182: FBP = REF1, FBN = 1V, LCD V_C = 0.8V					
		LT1183: FB = REF1, LCD V_C = 0.8V	●		0.35	1.0	µA
	LCD FBN/FB Offset Voltage	LT1182: Measured at FBN Pin, FBP = 0V, LCD V_C = 0.8V		–20	–12	–4	mV
		LT1183: Measured at FB Pin, LCD V_C = 0.8V	●	–27	–12	–1	mV
	Offset Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V, LCD V_C = 0.8V	●		0.01	0.2	%/V
	FBN/FB Input Bias Current	LT1182: FBN = Offset Voltage, FBP = 0V, LCD V_C = 0.8V					
		LT1183: FB = Offset Voltage, LCD V_C = 0.8V	●	–3.0	– 1.0		µA
g_m	FBP/FB to LCD V_C Transconductance	LT1182: ΔI_{VC} = ±25µA, FBN = 1V		650	900	1150	µmhos
		LT1183: ΔI_{VC} = ±25µA	●	500	900	1300	µmhos
	FBN/FB to LCD V_C Transconductance	LT1182: ΔI_{VC} = ±25µA, FBP = GND		550	800	1050	µmhos
		LT1183: ΔI_{VC} = ±25µA	●	400	800	1200	µmhos
	LCD Error Amplifier Source Current	LT1182: FBP = FBN = 1V or 0.25V,	●	50	100	175	µA
		LT1183: FB = 1V or 0.25V					
	LCD Error Amplifier Sink Current	LT1182: FBP = FBN = 1.5V or –0.25V,	●	35	100	175	µA
		LT1183: FB = 1.5V or –0.25V					
	LCD V_C Low Clamp Voltage	LT1182: FBP = FBN = 1.5V, LT1183: FB = 1.5V			0.01	0.3	V
	LCD V_C High Clamp Voltage	LT1182: FBP = FBN = 1V, LT1183: FB = 1V		1.7	2.0	2.4	V
	LCD V_C Switching Threshold	LT1182: FBP = FBN = 1V, LT1183: FB = 1V, V_{SW} DC = 0%		0.6	0.95	1.3	V
I_{LIM2}	LCD Switch Current Limit	Duty Cycle = 50%	●	0.625	1.00	1.5	A
		Duty Cycle = 75% (Note 3)	●	0.400	0.85	1.3	A
V_{SAT2}	LCD Switch On-Resistance	LCD I_{SW} = 0.5A	●		1.0	1.65	Ω
$\frac{\Delta I_Q}{\Delta I_{SW2}}$	Supply Current Increase During LCD Switch On-Time	LCD I_{SW} = 0.5A			20	30	mA/A
	Switch Minimum On-Time	Measured at CCFL V_{SW} and LCD V_{SW}			0.45		µs

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

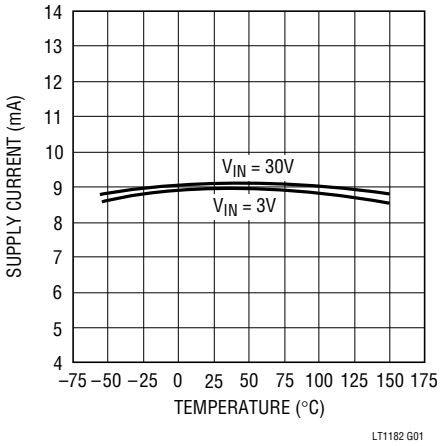
LT1182CS/LT1183CS/LT1184CS/LT1184FCS: $T_J = T_A + (P_D \times 100°C/W)$

Note 2: Does not include switch leakage.

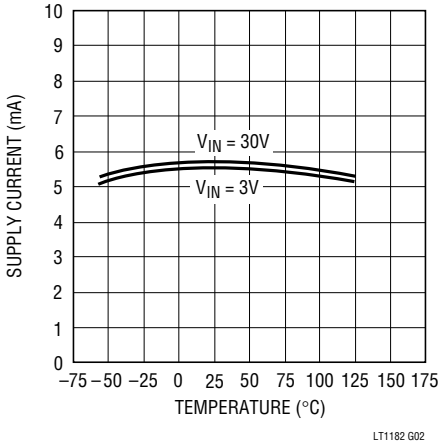
Note 3: For duty cycles (DC) between 50% and 75%, minimum guaranteed switch current is given by I_{LIM} = 1.4(1.393 – DC) for the CCFL regulator and I_{LIM} = 0.7(1.393 – DC) for the LCD contrast regulator due to internal slope compensation circuitry.

TYPICAL PERFORMANCE CHARACTERISTICS

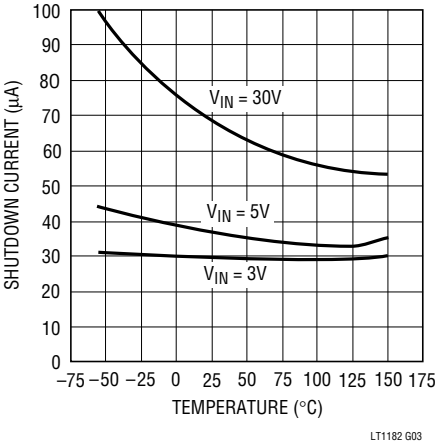
LT1182/LT1183 Supply Current vs Temperature



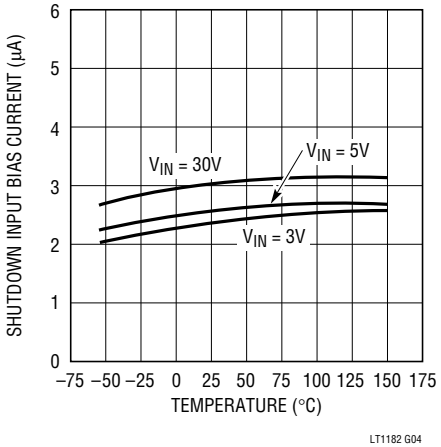
LT1184/LT1184F Supply Current vs Temperature



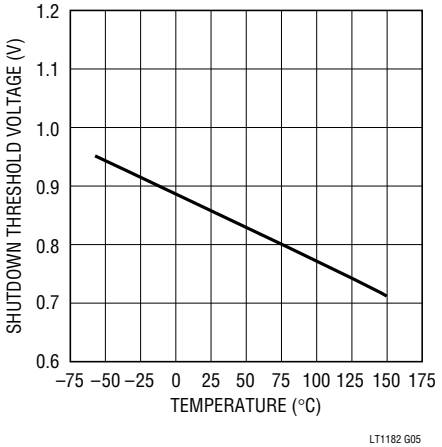
Shutdown Current vs Temperature



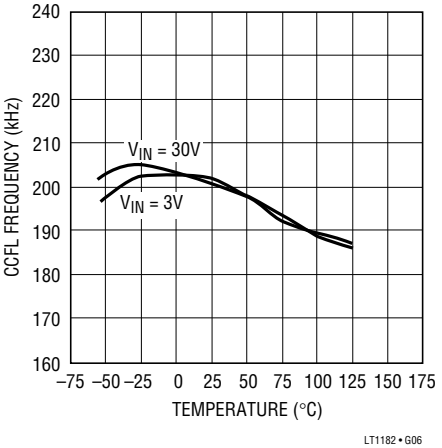
Shutdown Input Bias Current vs Temperature



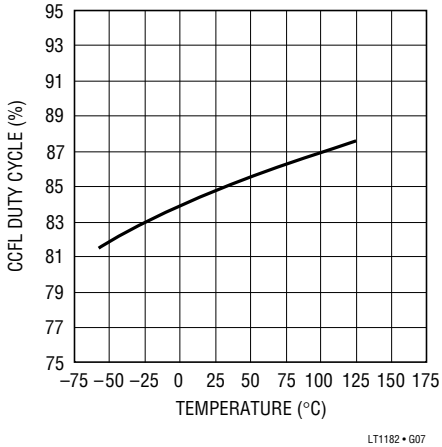
Shutdown Threshold Voltage vs Temperature



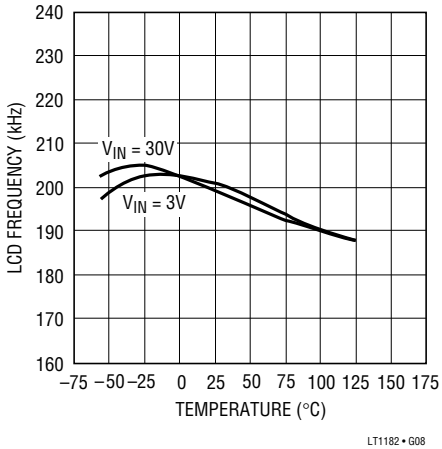
CCFL Frequency vs Temperature



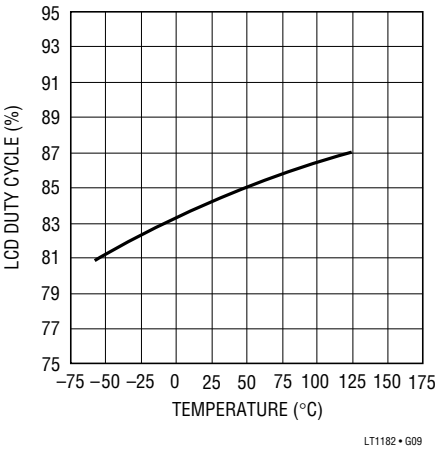
CCFL Duty Cycle vs Temperature



LCD Frequency vs Temperature

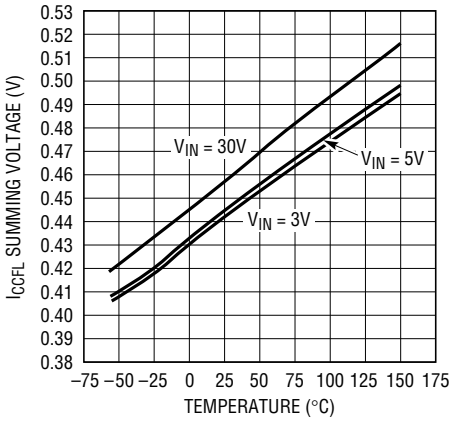


LCD Duty Cycle vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

I_{CCFL} Summing Voltage vs Temperature



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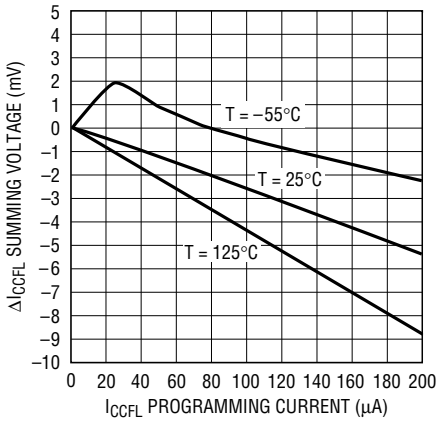
I_{CCFL} Summing Voltage Load Regulation



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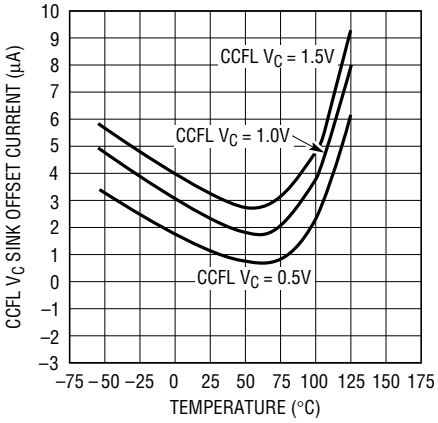
CCFL V_C Offset Sink Current vs Temperature



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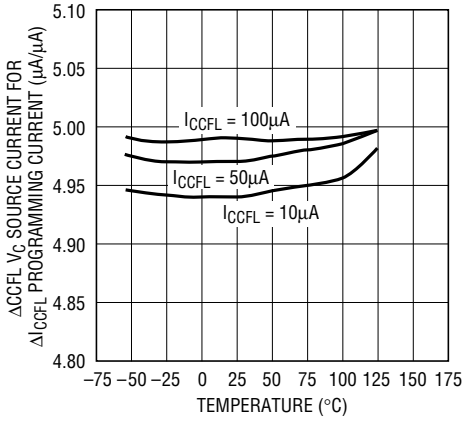
ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current vs Temperature



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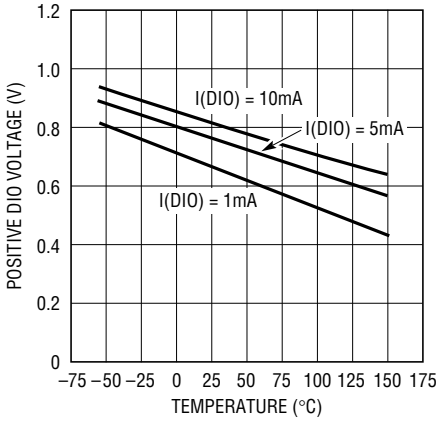
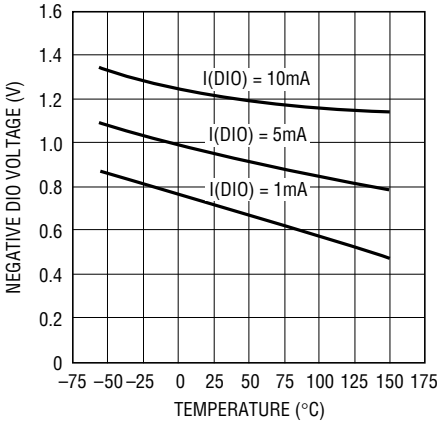
Positive DIO Voltage vs Temperature



LT1182 • G14

Negative DIO Voltage vs Temperature



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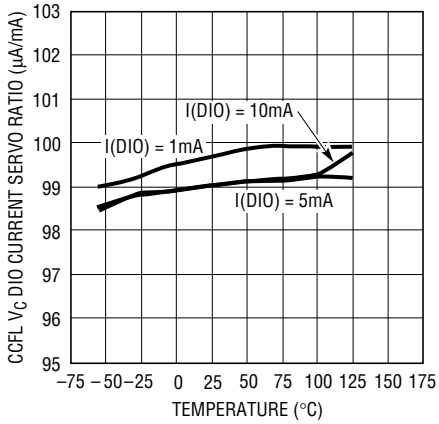
CCFL V_C to DIO Current Servo Ratio vs Temperature



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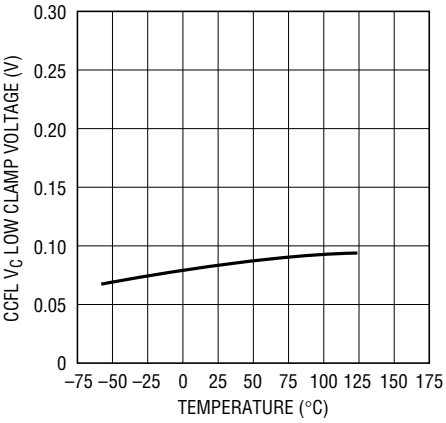
CCFL V_C Low Clamp Voltage vs Temperature



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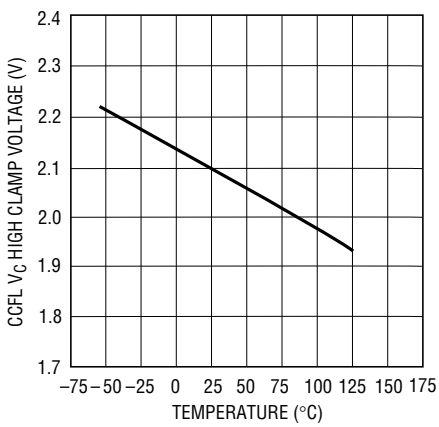
CCFL V_C High Clamp Voltage vs Temperature



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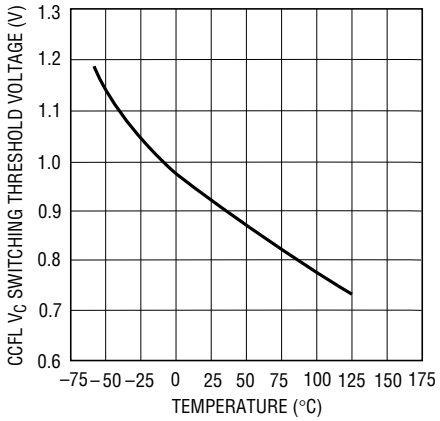
TYPICAL PERFORMANCE CHARACTERISTICS

CCFL V_C Switching Threshold Voltage vs Temperature



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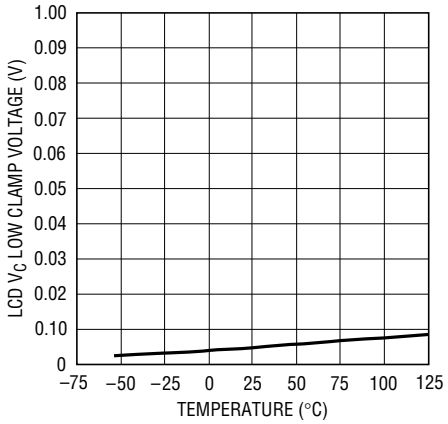
LCD V_C Low Clamp Voltage vs Temperature



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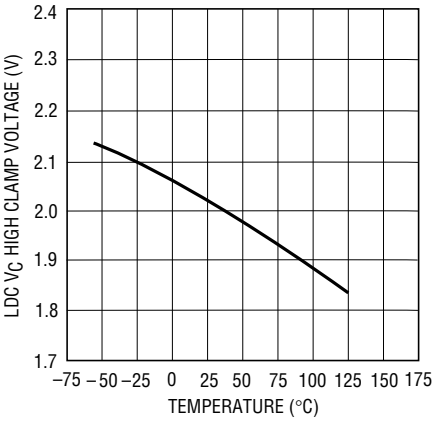
LCD V_C High Clamp Voltage vs Temperature



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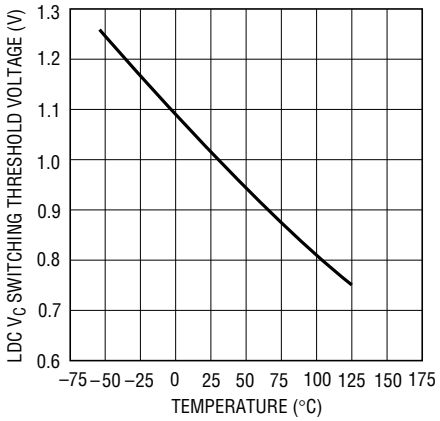
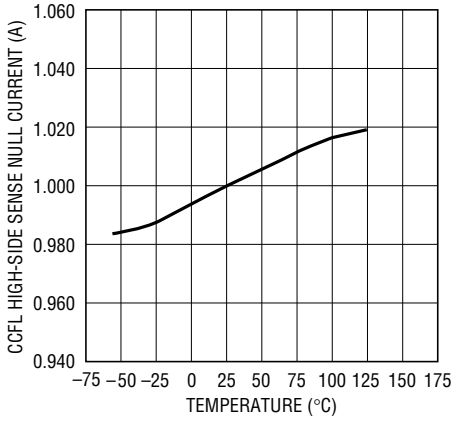
LCD V_C Switching Threshold Voltage vs Temperature



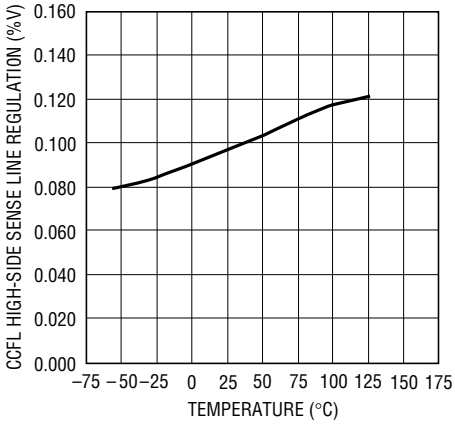
LT1182 • G22

CCFL High-Side Sense Null Current vs Temperature



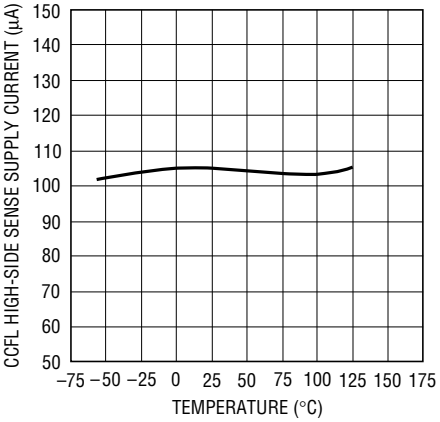
LT1182 • G23

CCFL High-Side Sense Null Current Line Regulation vs Temperature



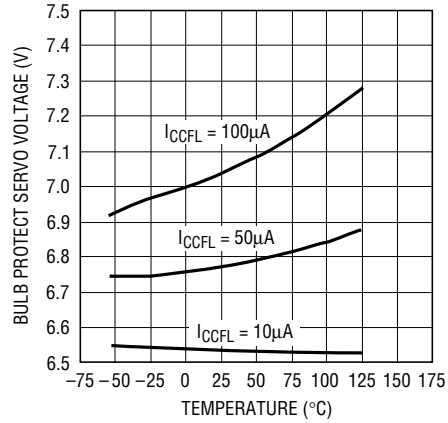
LT1182 • G24

CCFL High-Side Sense Supply Current vs Temperature



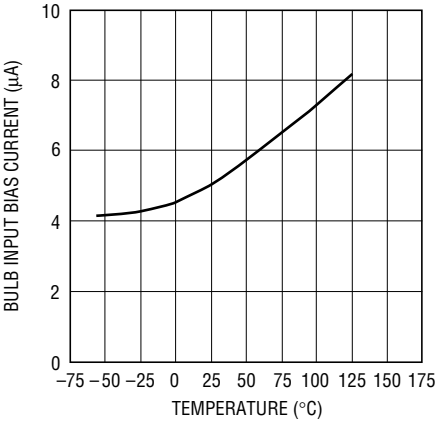
LT1182 • G25

Bulb Protect Servo Voltage vs Temperature



LT1182 • G26

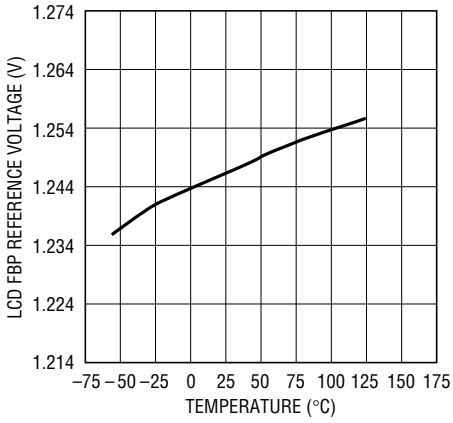
Bulb Input Bias Current vs Temperature



LT1182 • G27

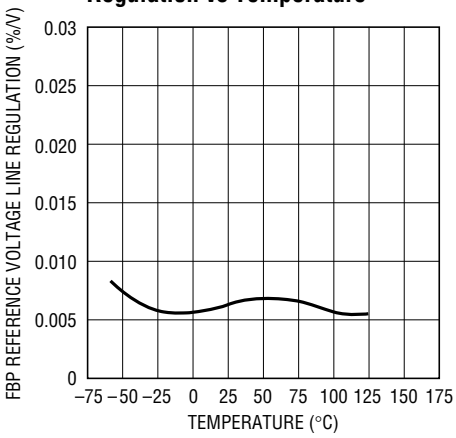
TYPICAL PERFORMANCE CHARACTERISTICS

LCD FBP Reference vs Temperature



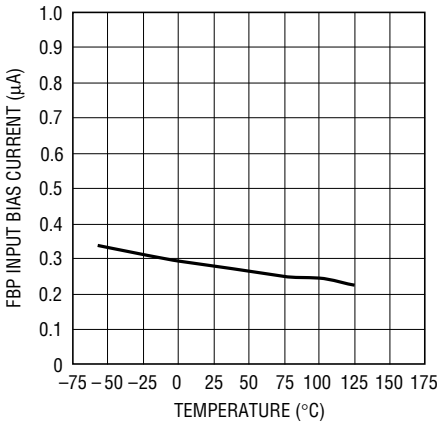
LT1182 • G28

FBP Reference Voltage Line Regulation vs Temperature



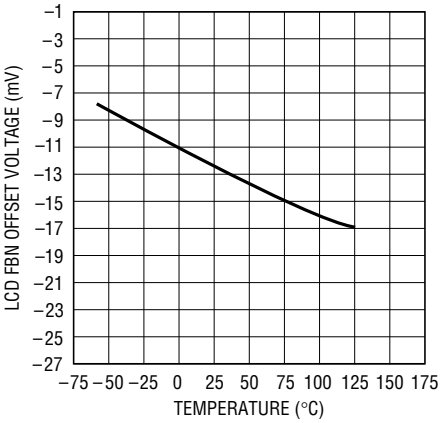
LT1182 • G29

FBP Input Bias Current vs Temperature

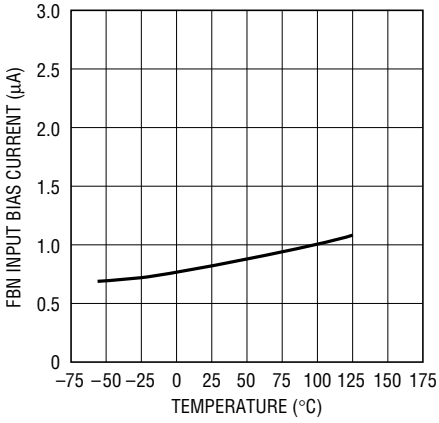


LT1182 • G30

LCD FBN Offset Voltage vs Temperature

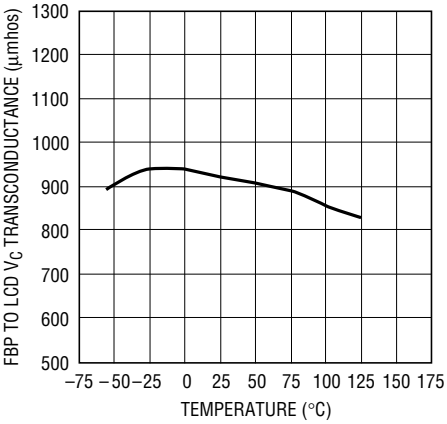


FBN Input Bias Current vs Temperature



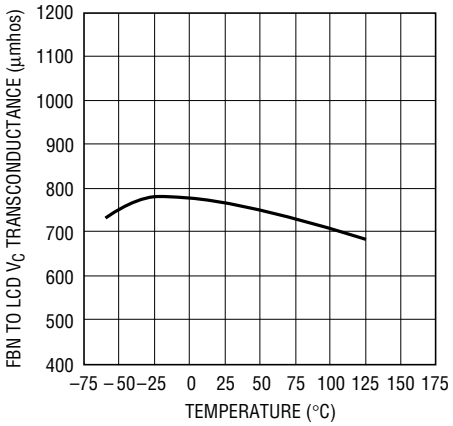
LT1182 • G32

FBP to LCD V_C Transconductance vs Temperature



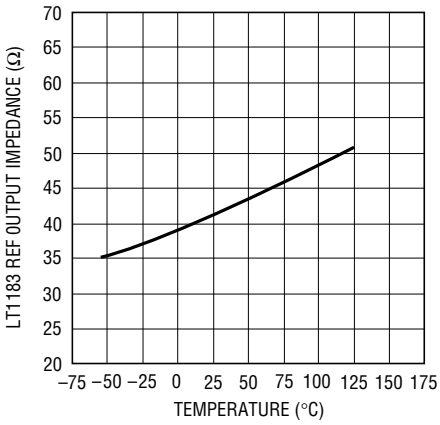
LT1182 • G33

FBN to LCD V_C Transconductance vs Temperature



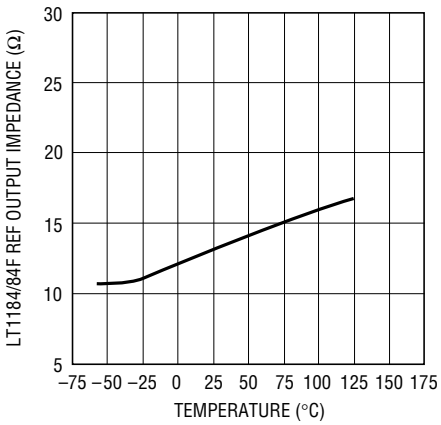
LT1182 • G34

LT1183 REF Output Impedance vs Temperature



LT1182 • G35

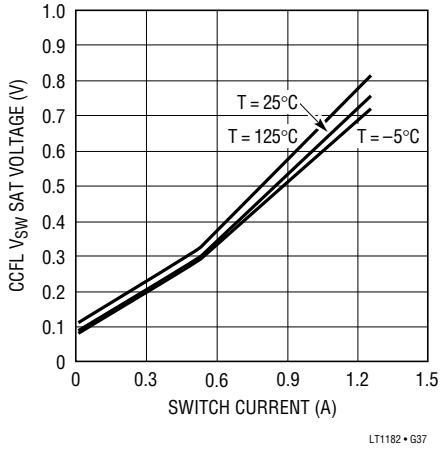
LT1184/84F REF Output Impedance vs Temperature



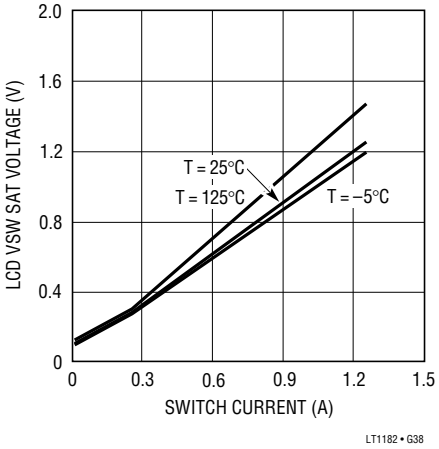
LT1182 • G36

TYPICAL PERFORMANCE CHARACTERISTICS

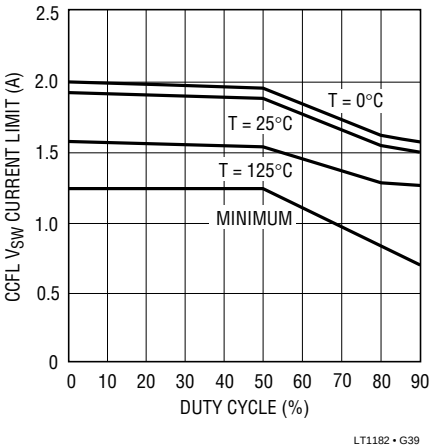
CCFL V_{SW} Sat Voltage vs Switch Current



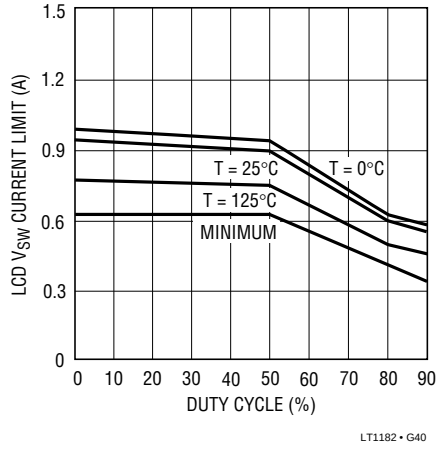
LCD V_{SW} Sat Voltage vs Switch Current



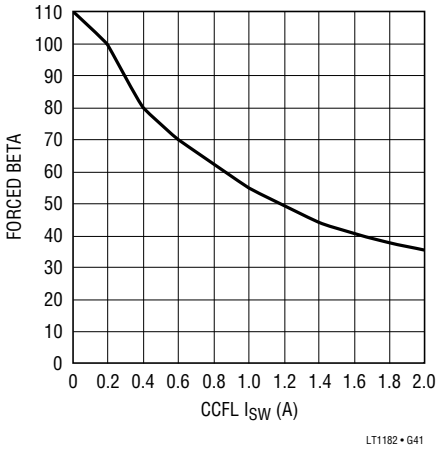
CCFL V_{SW} Current Limit vs Duty Cycle



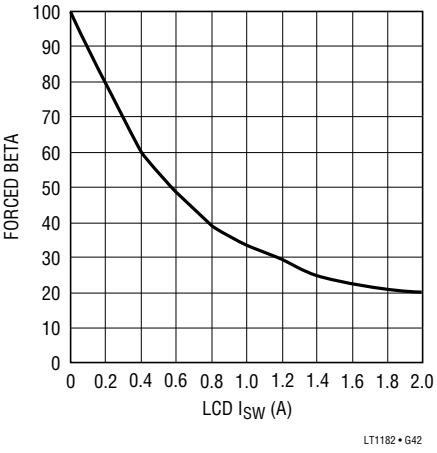
LCD V_{SW} Current Limit vs Duty Cycle



Forced Beta vs I_{SW} on CCFL V_{SW}



Forced Beta vs I_{SW} on LCD V_{SW}



PIN FUNCTIONS

LT1182/LT1183/LT1184/LT1184F

CCFL PGND (Pin 1): This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and permits internal, switch-current sensing. The regulators provide a separate analog ground and power ground(s) to isolate high current ground paths from low current signal paths. Linear Technology recommends the use of star-ground layout techniques.

I_{CCFL} (Pin 2): This pin is the input to the CCFL lamp current programming circuit. This pin internally regulates to 450mV (LT1182/LT1183) or 465mV (LT1184/LT1184F). The pin accepts a DC input current signal of 0μA to 100μA full scale. This input signal is converted to a 0μA to 500μA source current at the CCFL V_C pin. By shunt regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control. As input programming current increases, the regulated lamp current increases. For a typical 6mA lamp, the range of input programming current is about 0μA to 50μA.

DIO (Pin 3): This pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the two diodes connect to ground. In a grounded lamp configuration, DIO connects to the low voltage side of the lamp. Bidirectional lamp current flows in the DIO pin and thus the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin. This current nulls against the source current provided by the lamp-current programmer circuit. A single capacitor on the CCFL V_C pin provides both stable loop compensation and an averaging function to the half-wave-rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current. This scheme reduces the number of loop compensation components and permits faster loop transient response in comparison to previously published circuits. If a floating-lamp configuration is used, ground the DIO pin.

CCFL V_C (Pin 4): This pin is the output of the lamp current programmer circuit and the input of the current comparator for the CCFL regulator. Its uses include frequency compensation, lamp-current averaging for grounded lamp circuits, and current limiting. The voltage on the CCFL V_C pin determines the current trip level for switch turnoff. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current) with respect to analog ground (AGND). This pin has a high impedance output and permits external voltage clamping to adjust current limit. A single capacitor to ground provides stable loop compensation. This simplified loop compensation method permits the CCFL regulator to exhibit single-pole transient response behavior and virtually eliminates transformer output overshoot.

AGND (Pin 5): This pin is the low current analog ground. It is the negative sense terminal for the internal 1.24V reference and the I_{CCFL} summing voltage in the LT1182/LT1183/LT1184/LT1184F. It is also a sense terminal for the LCD dual input error amplifier in the LT1182/LT1183. Connect external feedback divider networks that terminate to ground and frequency compensation components that terminate to ground directly to this pin for best regulation and performance.

$\overline{\text{SHUTDOWN}}$ (Pin 6): Pulling this pin low causes complete regulator shutdown with quiescent current typically reduced to 35μA. The nominal threshold voltage for this pin is 0.85V. If the pin is not used, it can float high or be pulled to a logic high level (maximum of 6V). Carefully evaluate active operation when allowing the pin to float high. Capacitive coupling into the pin from switching transients could cause erratic operation.

CCFL V_{SW} (Pin 16): This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch provides a minimum of 1.25A. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

PIN FUNCTIONS

Bulb (Pin 15): This pin connects to the low side of a 7V threshold comparator between the BAT and Bulb pins. This circuit sets the maximum voltage level across the primary side of the Royer converter under all operating conditions and limits the maximum secondary output under start-up conditions or open lamp conditions. This eases transformer voltage rating requirements. Set the voltage limit to insure lamp start-up with worst-case, lamp start voltages and cold-temperature system operating conditions. The Bulb pin connects to the junction of an external divider network. The divider network connects from the center tap of the Royer transformer or the actual battery supply voltage to the top side of the current source "tail inductor". A capacitor across the top of the divider network filters switching ripple and sets a time constant that determines how quickly the clamp activates. When the comparator activates, sink current is generated to pull the CCFL V_C pin down. This action transfers the entire regulator loop from current mode operation into voltage mode operation.

BAT (Pin 14): This pin connects to the battery or battery charger voltage from which the CCFL Royer converter and LCD contrast converter operate. This voltage is typically higher than the V_{IN} supply voltage but can be equal or less than V_{IN}. However, the BAT voltage must be at least 2.1V greater than the internal 2.4V regulator or 4.5V minimum up to 30V maximum. This pin provides biasing for the lamp current programming block, is used with the Royer pin for floating lamp configurations, and connects to one input for the open lamp protection circuitry. For floating lamp configurations, this pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. The BAT and Royer pins monitor the primary side Royer converter current through an internal 0.1Ω top side current sense resistor. A 0A to 1A primary side, center tap converter current is translated to an input signal range of 0mV to 100mV for the current sense amplifier. This input range translates to a 0μA to 500μA sink current at the CCFL V_C pin that nulls against the source current provided by the programmer circuit. The BAT pin also connects to the top side of an internal clamp between the BAT and Bulb pins.

Royer (Pin 13): This pin connects to the center-tapped primary of the Royer converter and is used with the BAT pin in a floating lamp configuration where lamp current is controlled by sensing Royer primary side converter current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. If the CCFL regulator is not used in a floating lamp configuration, tie the Royer and BAT pins together. This pin is only available on the LT1182/LT1183/LT1184F.

V_{IN} (Pin 12): This pin is the supply pin for the LT1182/LT1183/LT1184/LT1184F. The ICs accept an input voltage range of 3V minimum to 30V maximum with little change in quiescent current (zero switch current). An internal, low dropout regulator provides a 2.4V supply for most of the internal circuitry. Supply current increases as switch current increases at a rate approximately 1/50 of switch current. This corresponds to a forced Beta of 50 for each switch. The ICs incorporate undervoltage lockout by sensing regulator dropout and lockout switching for input voltages below 2.5V. Hysteresis is not used to maximize the useful range of input voltage. The typical input voltage is a 3.3V or 5V logic supply.

LT1182/LT1183

LCD V_C (Pin 7): This pin is the output of the LCD contrast error amplifier and the input of the current comparator for the LCD contrast regulator. Its uses include frequency compensation and current limiting. The voltage on the LCD V_C pin determines the current trip level for switch turnoff. During normal operation, this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). The LCD V_C pin has a high impedance output and permits external voltage clamping to adjust current limit. A series R/C network to ground provides stable loop compensation.

LCD PGND (Pin 8): This pin is the emitter of an internal NPN power switch. LCD contrast switch current flows through this pin and permits internal, switch-current sensing. The regulators provide a separate analog ground and power ground(s) to isolate high current ground paths from low current signal paths. Linear Technology recommends star-ground layout techniques.

PIN FUNCTIONS

LCD V_{SW} (Pin 9): This pin is the collector of the internal NPN power switch for the LCD contrast regulator. The power switch provides a minimum of 625mA. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

LT1182

FBN (Pin 10): This pin is the noninverting terminal for the negative contrast control error amplifier. The inverting terminal is offset from ground by –12mV and defines the error amplifier output state under start-up conditions. The FBN pin acts as a summing junction for a resistor divider network. Input bias current for this pin is typically 1μA flowing out of the pin. If this pin is not used, force FBN to greater than 0.5V to deactivate the negative contrast control input stage. The proximity of FBN to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FBN to ground filters switching ripple.

FBP (Pin 11): This pin is the inverting terminal for the positive contrast control error amplifier. The noninverting terminal is tied to an internal 1.244V reference. Input bias current for this pin is typically 0.5μA flowing into the pin. If this pin is not used, ground FBP to deactivate the positive contrast control input stage. The proximity of FBP to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FBP to ground filters switching ripple.

LT1183

FB (Pin 10): This pin is the common connection between the noninverting terminal for the negative contrast error amplifier and the inverting terminal for the positive-contrast error amplifier. In comparison to the LT1182, the FBN and the FBP pins tie together and come out as one pin. This scheme permits one polarity of contrast to be regulated. The proximity of FB to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FB to ground filters switching ripple.

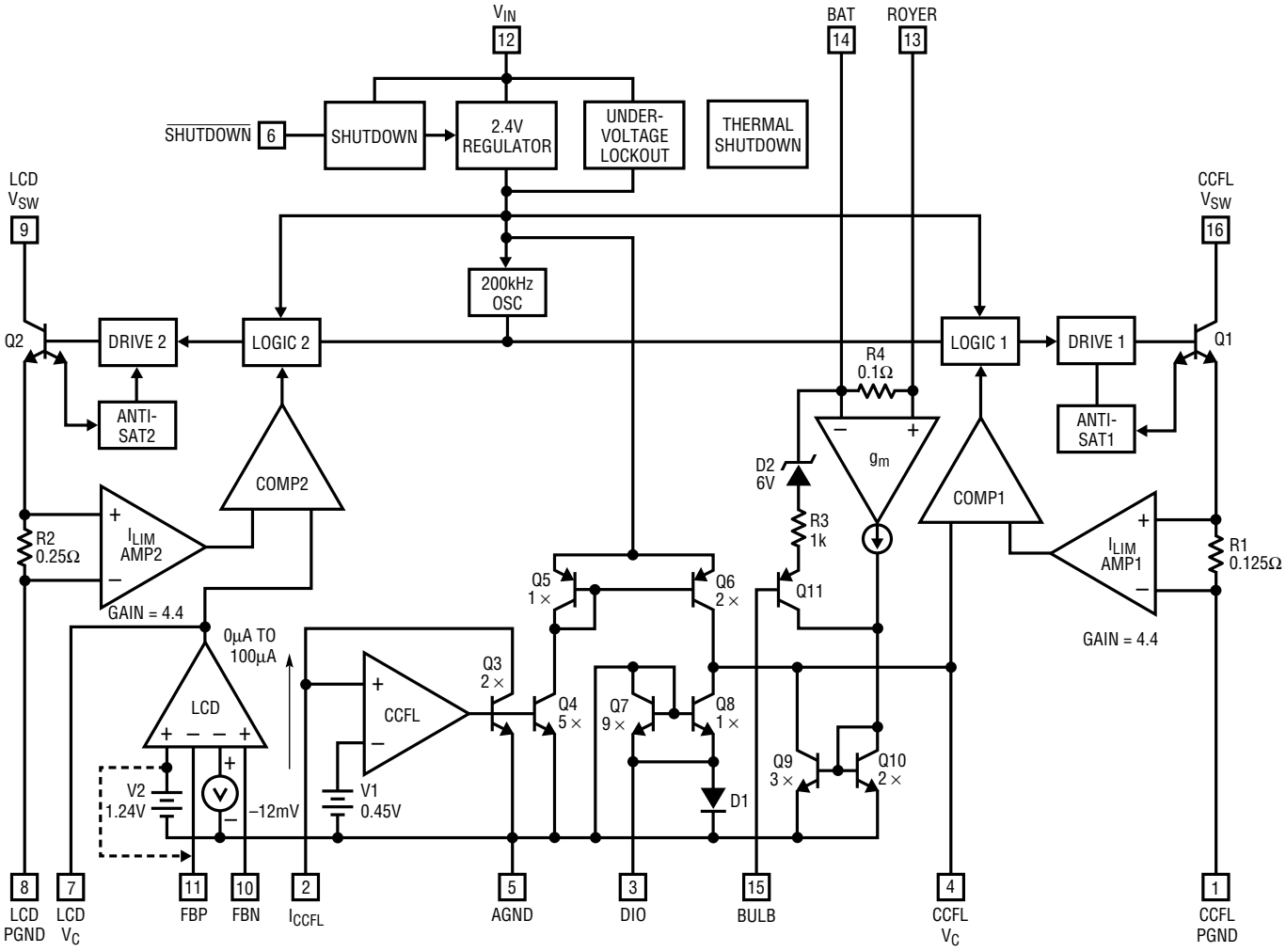
The FB pin requires attention to start-up conditions when generating negative contrast voltages. The pin has two stable operating points; regulating to 1.244V for positive contrast voltages or regulating to –12mV for negative contrast voltages. Under start-up conditions, the FB pin heads to a positive voltage. If negative contrast voltages are generated, tie a diode from the FB pin to ground. This ensures that the FB pin will clamp before reaching the positive reference voltage. Switching action then pulls the FB pin back to its normal servo voltage.

LT1183/LT1184/LT1184F

REF (Pin 11): This pin brings out the 1.244V reference. Its functions include the programming of negative contrast voltages with an external resistor divider network (LT1183 only) and the programming of lamp current for the I_{CCFL} pin. LTC does not recommend using the REF pin for both functions at once. The REF pin has a typical output impedance of 45Ω on the LT1183 and a typical output impedance of 15Ω on the LT1184/LT1184F. Reference load current should be limited to a few hundred microamperes, otherwise reference regulation will be degraded. REF is used to generate the maximum programming current for the I_{CCFL} pin by placing a resistor between the pins. PWM or DAC control subtracts from the maximum programming current. A small decoupling capacitor (0.1uF) is recommended to filter switching transients.

BLOCK DIAGRAM

LT1182/LT1183 CCFL/LCD Contrast Regulator Top Level Block Diagram

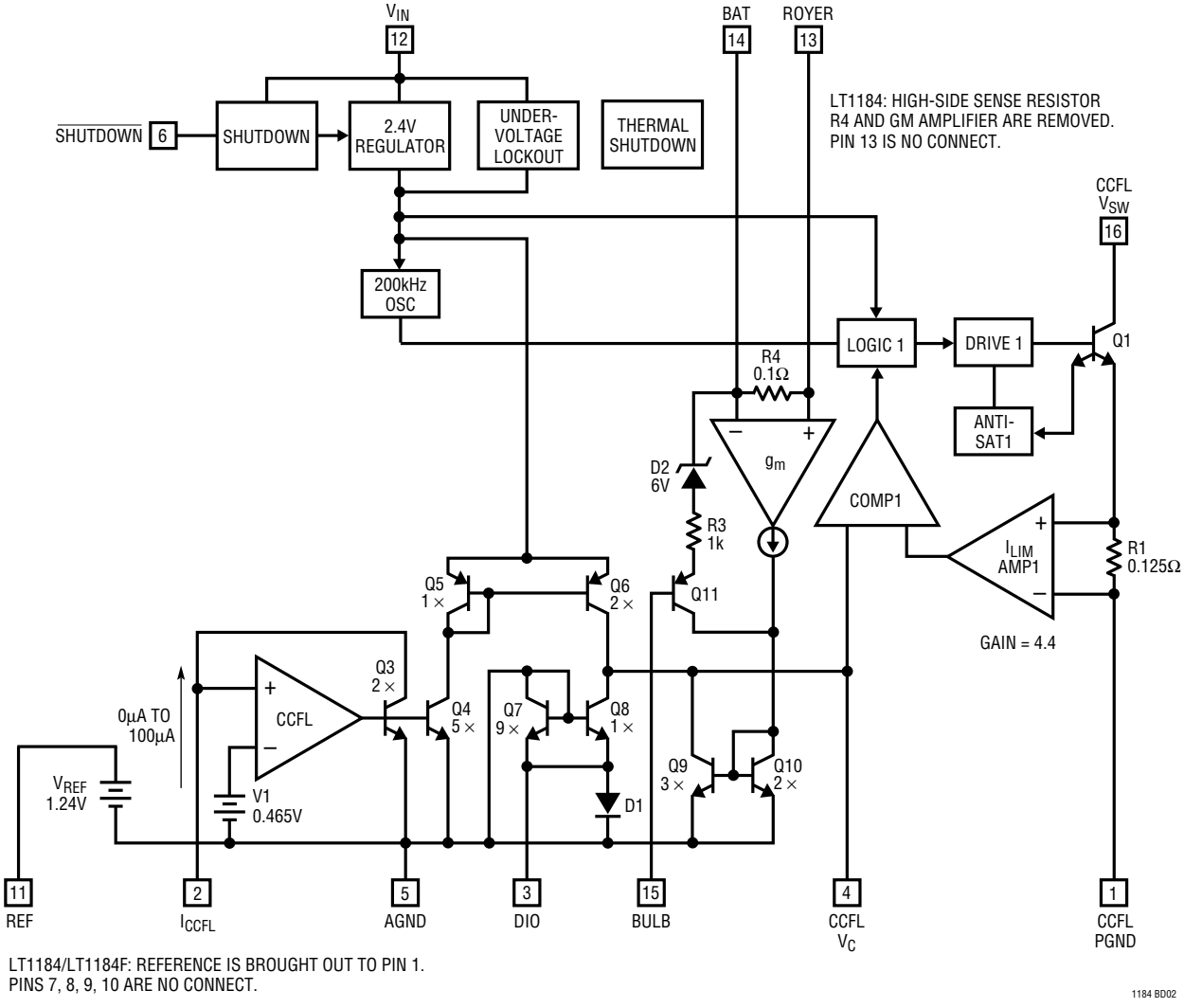


LT1183: FBP AND FBN ARE TIED TOGETHER TO CREATE FB AT PIN 10. THE REFERENCE IS BROUGHT OUT TO PIN 11.

1182 BD01

BLOCK DIAGRAM

LT1184/LT1184F CCFL Regulator Top Level Block Diagram



LT1184/LT1184F: REFERENCE IS BROUGHT OUT TO PIN 1.
PINS 7, 8, 9, 10 ARE NO CONNECT.

1184 BD02

APPLICATIONS INFORMATION

Introduction

Current generation portable computers and instruments use backlit Liquid Crystal Displays (LCDs). These displays also appear in applications extending to medical equipment, automobiles, gas pumps, and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency in backlighting the display. Providing the most light out for the least amount of input power is the most important goal. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. The lamps operate from DC, but migration effects damage the lamp and shorten its lifetime. Lamp drive should contain zero DC component. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This minimizes EMI and RF emissions. Such emissions can interfere with other devices and can also degrade overall operating efficiency. Sinusoidal CCFL drive maximizes current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or “pop-on”.

APPLICATIONS INFORMATION

Manufacturers offer a wide array of monochrome and color displays. LCD display types include passive matrix and active matrix. These displays differ in operating voltage polarity (positive and negative contrast voltage displays), operating voltage range, contrast adjust range, and power consumption. LCD contrast supplies must regulate, provide output adjustment over a significant range, operate over a wide input voltage range, and provide load currents from milliamps to tens of milliamps.

The small size and battery-powered operation associated with LCD equipped apparatus dictate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Displays found in newer color machines can have a contrast power supply battery drain as high as 20%.

Additionally, all components including PC board and hardware, usually must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

The CCFL switching regulator in the LT1182/LT1183/LT1184/LT1184F typically drives an inductor that acts as a switched mode current source for a current driven Royer class converter with efficiencies as high as 90%. The control loop forces the regulator to pulse-width modulate the inductor's average current to maintain constant current in the lamp. The constant current's value, and thus lamp intensity is programmable. This drive technique provides a wide range of intensity control. A unique lamp current programming block permits either grounded-lamp or floating-lamp configurations. Grounded-lamp circuits directly control one-half of actual lamp current. Floating-lamp circuits directly control the Royer's primary side converter current. Floating-lamp circuits provide differential drive to the lamp and reduce the loss from stray lamp-to-frame capacitance, extending illumination range.

The LCD contrast switching regulator in the LT1182/LT1183 is typically configured as a flyback converter and generates a bias supply for contrast control. Other topology choices for generating the bias supply include a boost converter or a boost/charge pump converter. The supply's variable output permits adjustment of contrast for the majority of available displays. Some newer types of displays require a fairly constant supply voltage and provide contrast adjustment through a digital control pin. A unique, dual polarity, error amplifier and the selection of a flyback converter topology allow either positive or negative LCD contrast voltages to be generated with minor circuit changes. The difference between the LT1182 and LT1183 is found in the pinout for the inputs of the LCD contrast error amplifier. The LT1182 brings out the error amplifier inputs individually for setting up positive and negative polarity contrast capability. This feature allows an output connector to determine the choice of contrast operating polarity by a ground connection. The LT1183 ties the error amplifier inputs together and brings out an internal reference. The reference may be used in generating negative contrast voltages or in programming lamp current.

Block Diagram Operation

The LT1182/LT1183/LT1184/LT1184F are fixed frequency, current mode switching regulators. Fixed frequency, current mode switchers control switch duty cycle directly by switch current rather than by output voltage. Referring to the block diagram for the LT1182/LT1183, the switch for each regulator turns ON at the start of each oscillator cycle. The switches turn OFF when switch current reaches a predetermined level. The operation of the CCFL regulator in the LT1184/LT1184F is identical to that in the LT1182/LT1183. The control of output lamp current is obtained by using the output of a unique programming block to set current trip level. The contrast voltage is controlled by the output of a dual-input-stage error amplifier, which sets current trip level. The current mode switching technique has several advantages. First, it provides excellent rejection of input voltage variations. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

The LT1182/LT1183/LT1184/LT1184F incorporate a low dropout internal regulator that provides a 2.4V supply for most of the internal circuitry. This low dropout design allows input voltage to vary from 3V to 30V with little

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change in quiescent current. An active low shutdown pin typically reduces total supply current to 35μA by shutting off the 2.4V regulator and locking out switching action for standby operation. The ICs incorporate undervoltage lockout by sensing regulator dropout and locking out switching below about 2.5V. The regulators also provide thermal shutdown protection that locks out switching in the presence of excessive junction temperatures.

A 200kHz oscillator is the basic clock for all internal timing. The oscillator turns on an output via its own logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in a power switch and adjusts base drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides rapid turn-off of the switch. The CCFL power switch is guaranteed to provide a minimum of 1.25A in the LT1182/LT1183/LT1184/LT1184F and the LCD power switch is guaranteed to provide a minimum of 0.625A in the LT1182/LT1183. The anti-sat circuitry provides a ratio of switch current to driver current of about 50:1.

Simplified Lamp Current Programming

A programming block in the LT1182/LT1183/LT1184/LT1184F controls lamp current, permitting either grounded-lamp or floating-lamp configurations. Grounded configurations control lamp current by directly controlling one-half of actual lamp current and converting it to a feedback signal to close a control loop. Floating configurations control lamp current by directly controlling the Royer's primary side converter current and generating a feedback signal to close a control loop.

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. This approach converted an RMS current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop frequency compensation. This compensation scheme meant that the loop had to be fairly slow and that output overshoot with startup or overload conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements.

The LT1182/LT1183/LT1184/LT1184F eliminate the error amplifier concept entirely and replace it with a lamp current programming block. This block provides an easy-to-use interface to program lamp current. The programmer circuit also reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor. The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and virtually eliminates overshoot under startup or overload conditions.

Lamp current is programmed at the input of the programmer block, the I_{CCFL} pin. This pin is the input of a shunt regulator and accepts a DC input current signal of 0μA to 100μA. This input signal is converted to a 0μA to 500uA source current at the CCFL V_C pin. The programmer circuit is simply a current-to-current converter with a gain of five. By regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control. The typical input current programming range for 0mA to 6mA lamp current is 0μA to 50μA.

The I_{CCFL} pin is sensitive to capacitive loading and will oscillate with capacitance greater than 10pF. For example, loading the I_{CCFL} pin with a 1× or 10× scope probe causes oscillation and erratic CCFL regulator operation because of the probe's respective input capacitance. A current meter in series with the I_{CCFL} pin will also produce oscillation due to its shunt capacitance. Use a decoupling resistor of several kilo-ohms between the I_{CCFL} pin and the control circuitry if excessive stray capacitance exists. This is basically free with potentiometer or PWM control as these control schemes use resistors. A current output DAC should use an isolating resistor as the DAC can have significant output capacitance that changes as a function of input code.

Grounded-Lamp Configuration

In a grounded-lamp configuration, the low voltage side of the lamp connects directly to the LT1182/LT1183/LT1184/LT1184F DIO pin. This pin is the common connection between the cathode and anode of two internal diodes. In previous grounded-lamp solutions, these diodes were discrete units and are now integrated onto the IC, saving cost and board space. Bi-directional lamp current flows in the DIO pin and thus, the diodes conduct alternately on half

APPLICATIONS INFORMATION

cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL pin and nulls against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current.

The transfer function between lamp current and input programming current must be empirically determined and is dependent on the particular lamp/display housing combination used. The lamp and display housing are a distributed loss structure due to parasitic lamp-to-frame capacitance. This means that the current flowing at the high voltage side of the lamp is higher than what is flowing at the DIO pin side of the lamp. The input programming current is set to control lamp current at the high voltage side of the lamp, even though the feedback signal is the lamp current at the bottom of the lamp. This insures that the lamp is not overdriven which can degrade the lamp's operating lifetime.

Floating-Lamp Configuration

In a floating-lamp configuration, the lamp is fully floating with no galvanic connection to ground. This allows the transformer to provide symmetric, differential drive to the lamp. Balanced drive eliminates the field imbalance associated with parasitic lamp-to-frame capacitance and reduces "thermometering" (uneven lamp intensity along the lamp length) at low lamp currents.

Carefully evaluate display designs in relation to the physical layout of the lamp, it leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current flow degrades electrical efficiency and losses up to 25% have been observed in practice. As an example, at a Royer operating frequency of 60kHz, 1pF of stray capacitance represents an impedance of 2.65MΩ. With an operating lamp voltage of 400V and an operating lamp current of 6mA, the parasitic current is 150μA. The efficiency loss is 2.5%. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp, and displays supplied in metal enclosures. Losses for a good display are under 5% whereas losses for a bad display range from 5% to 25%. Lossy displays are the primary reason to use a floating-lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss by one-half.

Maintaining closed-loop control of lamp current in a floating lamp configuration now necessitates deriving a feedback signal from the primary side of the Royer transformer. Previous solutions have used an external precision shunt and high side sense amplifier configuration. This approach has been integrated onto the LT1182/LT1183/LT1184F for simplicity of design and ease of use. An internal 0.1W resistor monitors the Royer converter current and connects between the input terminals of a high-side sense amplifier. A 0A to 1A Royer primary side, center tap current is translated to a 0μA to 500uA sink current at the CCFL V_C pin to null against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the error sink current. Therefore, input programming current is related to average Royer converter current. Floating-lamp circuits operate similarly to grounded-lamp circuits, except for the derivation of the feedback signal.

The transfer function between primary side converter current and input programming current must be empirically determined and is dependent upon a myriad of factors including lamp characteristics, display construction, transformer turns ratio, and the tuning of the Royer oscillator. Once again, lamp current will be slightly higher at one end of the lamp and input programming current should be set for this higher level to insure that the lamp is not overdriven.

The internal 0.1Ω high-side sense resistor on the LT1182/LT1183/LT1184F is rated for a maximum DC current of 1A. However, this resistor can be damaged by extremely high surge currents at start-up. The Royer converter typically uses a few microfarads of bypass capacitance at the center tap of the transformer. This capacitor charges up when the system is first powered by the battery pack or an AC wall adapter. The amount of current delivered at start-up can be

APPLICATIONS INFORMATION

very large if the total impedance in this path is small and the voltage source has high current capability. Linear Technology recommends the use of an aluminum electrolytic for the transformer center tap bypass capacitor with an ESR greater than or equal to 0.5Ω. This lowers the peak surge currents to an acceptable level. In general, the wire and trace inductance in this path also help reduce the di/dt of the surge current. This issue only exists with floating lamp circuits as grounded-lamp circuits do not make use of the high-side sense resistor.

Optimizing Optical Efficiency vs Electrical Efficiency

Evaluating the performance of an LCD backlight requires the measurement of both electrical and photometric efficiencies. The best optical efficiency operating point does not necessarily correspond to the best electrical efficiency. However, these two operating points are generally close. The desired goal is to maximize the amount of light out for the least amount of input power. It is possible to construct backlight circuits that operate with over 90% electrical efficiency, but produce significantly less light output than circuits that operate at 80% electrical efficiency.

The best electrical efficiency typically occur's just as the CCFL's transformer drive waveforms begin to exhibit artifacts of higher order harmonics reflected back from the Royer transformer secondary. Maximizing electrical efficiency equates to smaller values for the Royer primary side, resonating capacitor and larger values for the Royer secondary side ballast capacitor. The best optical efficiency occurs with nearly ideal sinusoidal drive to the lamp. Maximizing optical efficiency equates to larger values for the Royer primary side resonating capacitor and smaller values for the Royer secondary side ballast capacitor. The preferred operating point for the CCFL converter is somewhere in between the best electrical efficiency and the best optical efficiency. This operating point maximizes photometric output per watt of input power.

Making accurate and repeatable measurements of electrical and optical efficiency is difficult under the best circumstances. Requirements include high voltage measurements and equipment specified for this operation, specialized calibrated voltage and current probes, wideband RMS voltmeters, a photometer, and a calorimeter (for the backlight enthusiast). Linear Technology's Application Note 55 and Design Note 101 contain detailed information regarding equipment needs.

Input Supply Voltage Operating Range

The backlight/LCD contrast control circuits must operate over a wide range of input supply voltage and provide excellent line regulation for the lamp current and the contrast output voltage. This range includes the normal range of the battery pack itself as well as the AC wall adapter voltage, which is normally much higher than the maximum battery voltage. A typical input supply is 7V to 28V; a 4 to 1 supply range.

Operation of the CCFL control circuitry from the AC wall adapter generates the worst-case stress for the CCFL transformer. Evaluations of loop compensation for overshoot on startup transients and overload conditions are essential to avoid destructive arcing, overheating, and transformer failure. Open-lamp conditions force the Royer converter to operate open-loop. Component stress is again worst-case with maximum input voltage conditions. The LT1182/LT1183/LT1184/LT1184F open-lamp protection clamps the maximum transformer secondary voltage to safe levels and transfers the regulator loop from current mode operation into voltage mode operation. Other fault conditions include board shorts and component failures. These fault conditions can increase primary side currents to very high levels, especially at maximum input voltage conditions. Solutions to these fault conditions include electrical and thermal fuses in the supply voltage trace.

Improvements in battery technology are increasing battery lifetimes and decreasing battery voltages required by the portable systems. However, operation at reduced battery voltages requires higher, turns-ratio transformers for the CCFL to generate equivalent output drive capability. The penalty incurred with high ratio transformers is higher, circulating currents acting on the same primary side components. Loss terms increase and electrical efficiency often decreases.

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Size Constraints

Tighter length, width, and height constraints for CCFL and LCD contrast control circuitry are the result of LCD display enclosure sizes remaining fairly constant while display screen sizes have increased. Space requirements for connector hardware include the input power supply and control signal connector, the lamp connector, and the contrast output voltage connector.

Even though size requirements are shrinking, the high voltage AC required to drive the lamp has not decreased. In some cases, the use of longer bulbs for color, portable equipment has increased the high voltage requirement. Accommodating the high voltage on the circuit board dictates certain layout spacings and routings, involves providing creepages and clearances in the transformer design, and most importantly, involves routing a hole underneath the CCFL transformer. Routing this hole minimizes high voltage leakage paths and prevents moisture buildup that can result in destructive arcing. In addition to high voltage layout techniques, use appropriate layout techniques for isolating high current paths from low-current signal paths.

This leaves the remaining space for control circuitry at a premium. Minimum component count is required and minimum size for the components used is required. This squeeze on component size is often in direct conflict with the goals of maximizing battery life and efficiency. Compromise is often the only remaining choice.

LCD Contrast Circuits

The LCD contrast switching regulator on the LT1182/LT1183 operates in many standard switching configurations and is used as a classic DC/DC converter. The dual-input-stage error amplifier easily regulates either positive or negative contrast voltages. Topology choices for the converter include single inductor and transformer-based solutions. The switching regulator operates equally well either in continuous mode or discontinuous mode. Efficiencies for LCD contrast circuits range from 75% to 85% and depend on the total power drain of the particular display. Adjustment control of the LCD contrast voltage is provided by either potentiometer, PWM, or DAC control.

Applications Support

Linear Technology invests an enormous amount of time, resources, and technical expertise in understanding, designing and evaluating backlight/LCD contrast solutions for system designers. The design of an efficient and compact LCD backlight system is a study of compromise in a transduced electronic system. Every aspect of the design is interrelated and any design change requires complete re-evaluation for all other critical design parameters. Linear Technology has engineered one of the most complete test and evaluation setups for backlight designs and understands the issues and tradeoffs in achieving a compact, effficient and economical customer solution. Linear Technology welcomes the opportunity to discuss, design, evaluate, and optimize any backlight/LCD contrast system with a customer. For further information on backlight/LCD contrast designs, consult the references listed below.

References

1. Williams, Jim. August 1992. *Illumination Circuitry for Liquid Crystal Displays*. Linear Technology Corporation, Application Note 49.

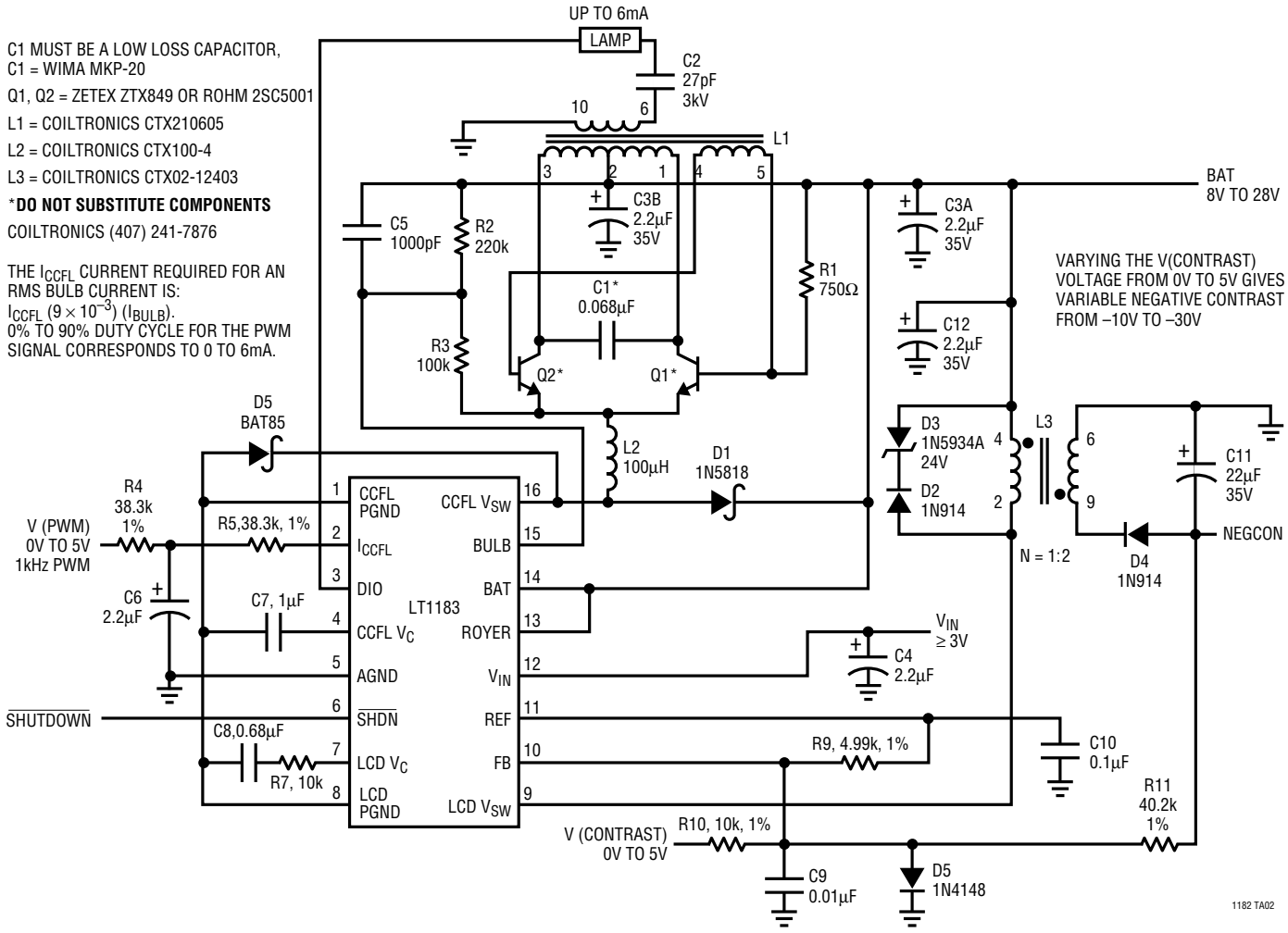
2. Williams, Jim. August 1993. *Techniques for 92% Efficient LCD Illumination*. Linear Technology Corporation, Application Note 55.

3. Bonte, Anthony. March 1995. *LT1182 Floating CCFL with Dual Polarity Contrast*. Linear Technology Corporation, Design Note 99.

4. Williams, Jim. April 1995. *A Precision Wideband Current Probe for LCD Backlight Meaasurement*. Linear Technology Corporation, Design Note 101.

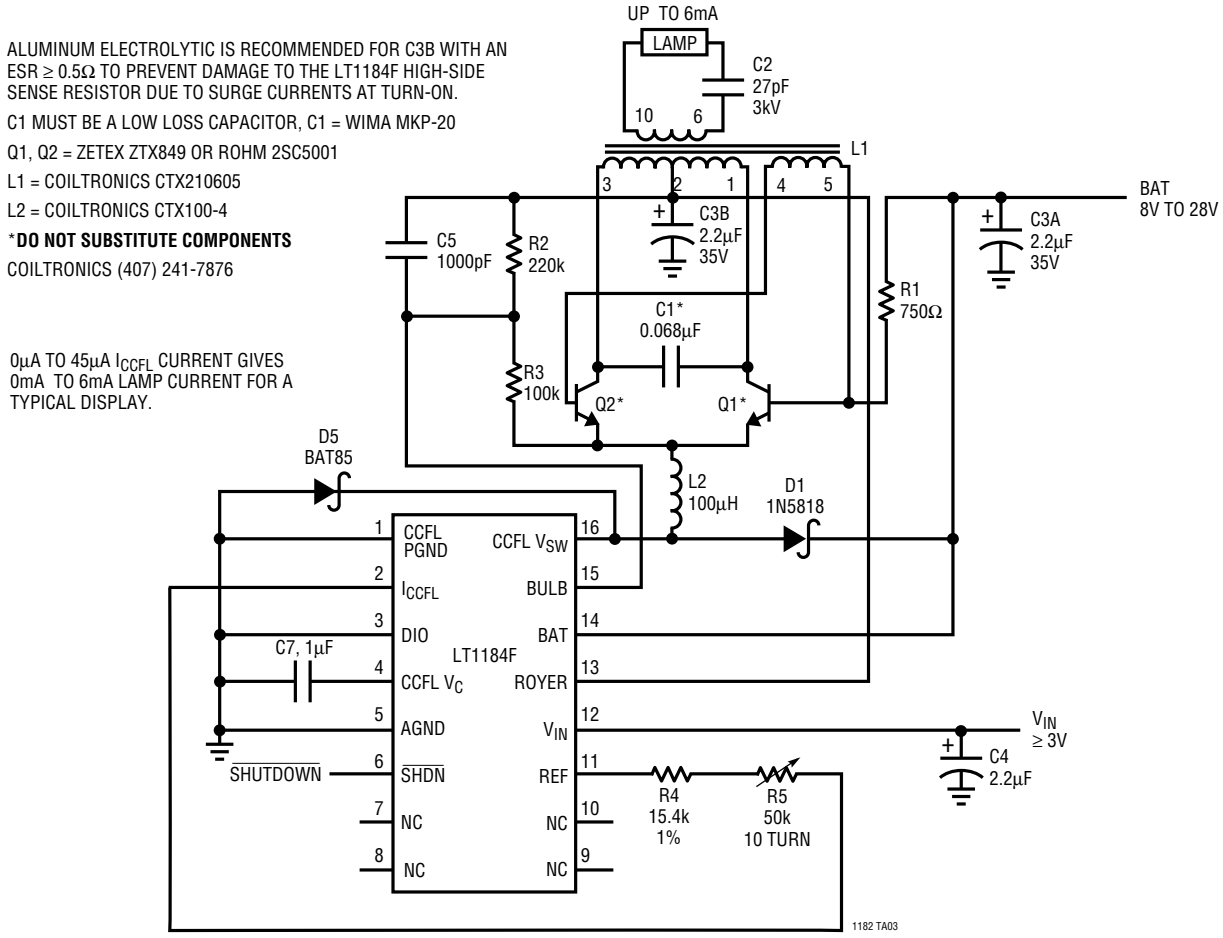
TYPICAL APPLICATIONS

90% Efficient Grounded CCFL Configuration with Negative Polarity LCD Contrast



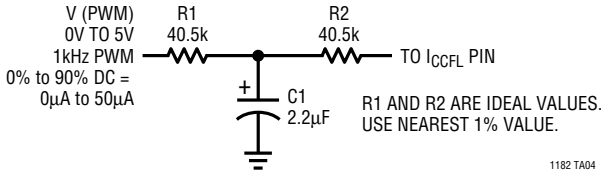
TYPICAL APPLICATIONS

LT1184F Floating CCFL with Potentiometer Control of Lamp Current

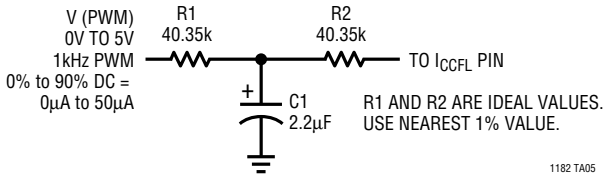


TYPICAL APPLICATIONS

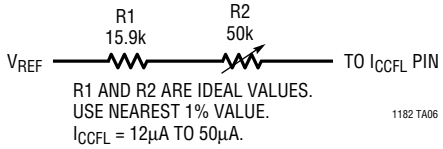
LT1182/LT1183 I_{CCFL} PWM Programming



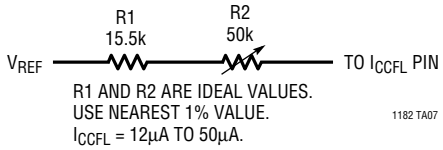
LT1184/LT1184F I_{CCFL} PWM Programming



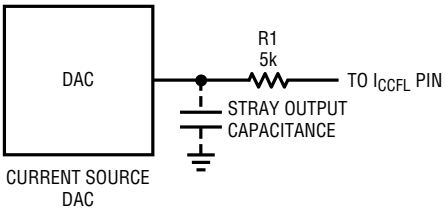
LT1183 I_{CCFL} Programming with Potentiometer Control



LT1184/LT1184F I_{CCFL} Programming with Potentiometer Control



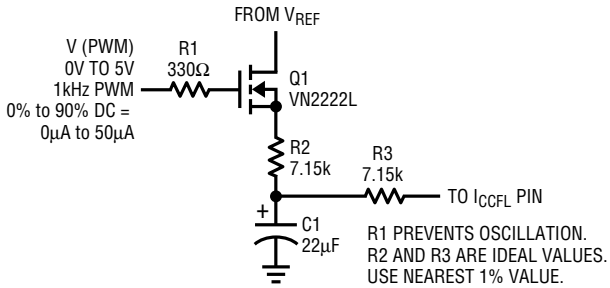
LT1182/LT1183/LT1184/LT1184F I_{CCFL} Programming with DAC Control



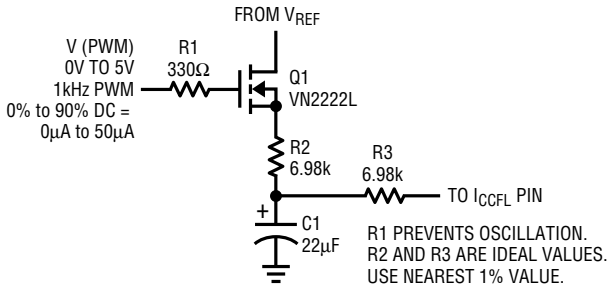
R1 DECOUPLES THE DAC OUTPUT CAPACITANCE FROM THE I_{CCFL} PIN.

1182 TA12

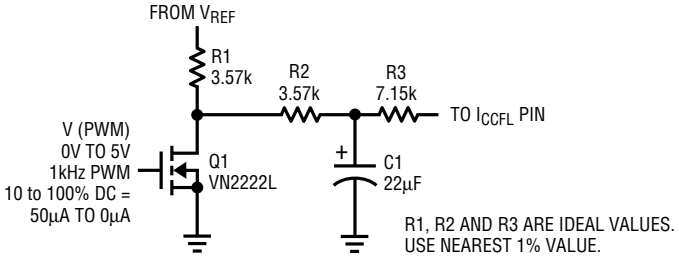
LT1183 I_{CCFL} PWM Programming with V_{REF}



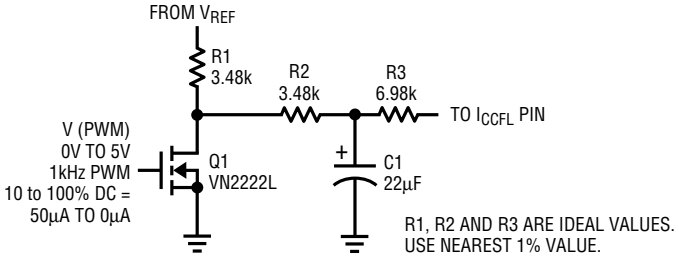
LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



LT1183 I_{CCFL} PWM Programming with V_{REF}

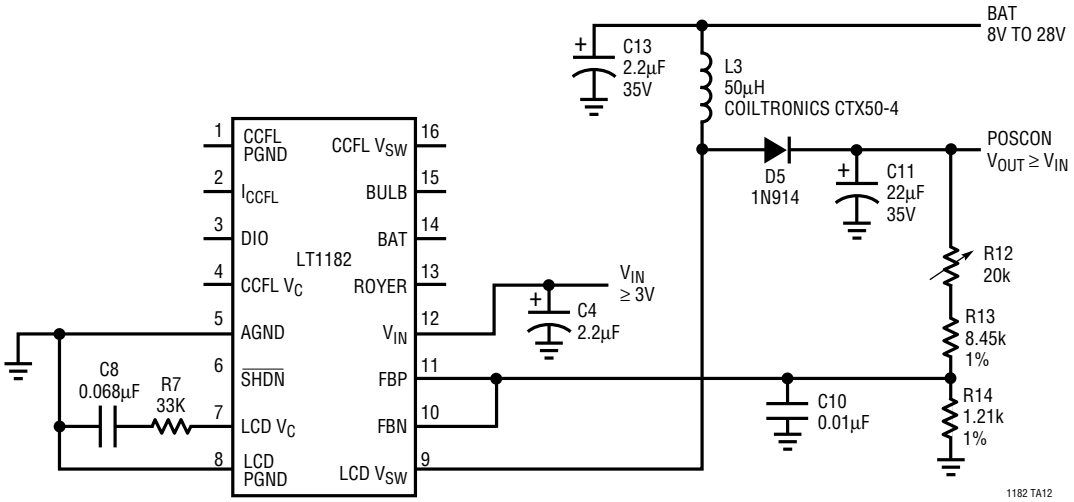


LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}

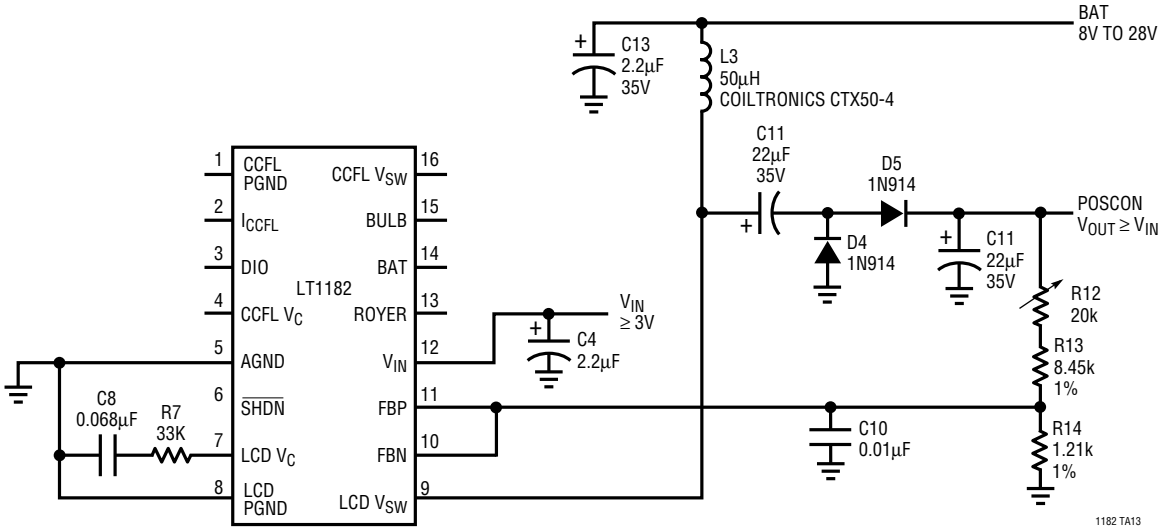


TYPICAL APPLICATIONS

LT1182 LCD Contrast Positive Boost Converter

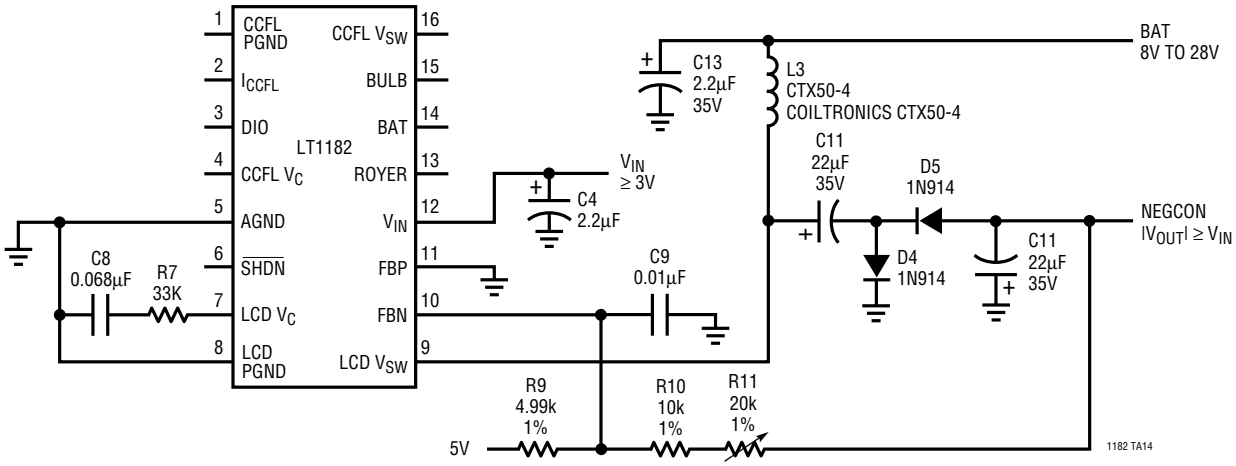


LT1182 LCD Contrast Positive Boost/Charge Pump Converter



TYPICAL APPLICATIONS

LT1182 LCD Contrast Positive to Negative/Charge Pump Converter



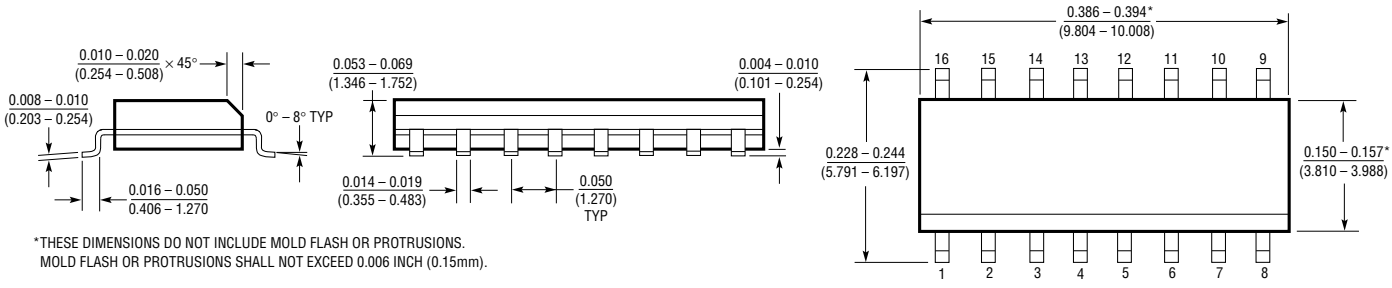
RELATED PARTS

PART NUMBER	FREQUENCY	SWITCH CURRENT	DESCRIPTION
LT1107	63kHz Hysteretic	1A	Micropower DC/DC Converter for LCD Contrast Control
LT1172	100kHz	1.25A	Current Mode Switching Regulator for CCFL or LCD Contrast Control
LT1173	24kHZ Hysteretic	1A	Micropower DC/DC Converter for LCD Contrast Control
LT1186	200kHz	1.25A	CCFL Switching Regulator with DAC for "Bits to Brightness Control"
LT1372	500kHz	1.5A	Current Mode Switching Regulator for CCFL or LCD Contrast Control

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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