# Programmable FemtoClock® NG LVPECL Oscillator Replacement

# ICS83PN625I

**DATA SHEET**

## General Description

The ICS83PN625I is a programmable LVPECL synthesizer that is "forward" footprint compatible with standard 5mm x 7mm oscillators. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. Forward footprint compatibility means that a board designed to accommodate the crystal oscillator interface and the optional control pins is also fully compatible with a canned oscillator footprint - the canned oscillator will drop onto the 10-VFQFN footprint for second sourcing purposes. This capability provides designers with programability and lead time advantages of silicon/crystal based solutions while maintaining compatibility with industry standard 5mm x 7mm oscillator footprints for ease of supply chain management. Oscillator-level performance is maintained with IDT's 4th Generation FemtoClock® NG PLL technology, which delivers sub 0.5ps rms phase jitter.

The ICS83PN625I defaults to 312.5MHz using a 25MHz crystal with 2 programming pins floating (pulled down/pulled up with internal pullup or pulldown resistors) but can also be set to 4 different frequency multiplier settings to support a wide variety of applications. The below table shows some of the more common application settings.

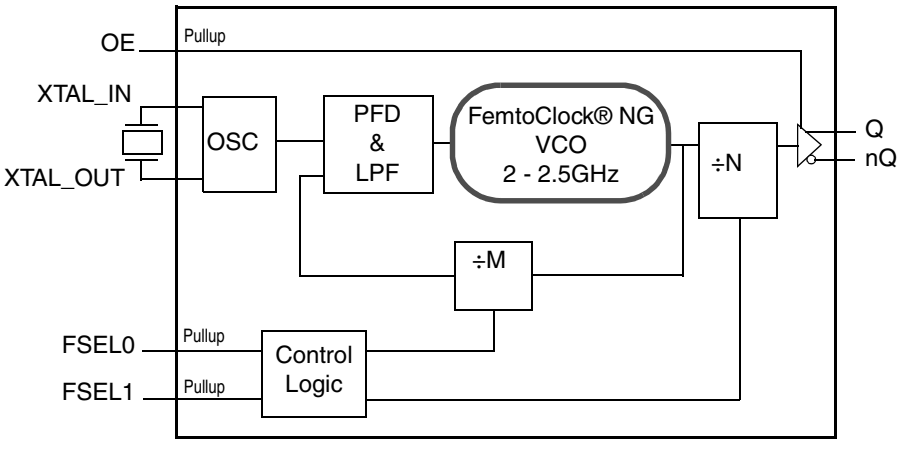
## Features

- Fourth Generation FemtoClock® Next Generation (NG) technology
- Footprint compatible with 5mm x 7mm differential oscillators
- One differential LVPECL output pair
- Crystal oscillator interface which can be overdriven by a single-ended reference clock
- Output frequency range: 125MHz – 625MHz
- Crystal/input frequency range: 25MHz, parallel resonant crystal
- VCO range: 2GHz – 2.5GHz
- Cycle-to-cycle jitter: 10ps (maximum), @ 3.3V±5%
- RMS phase jitter @ 156.25MHz, 12kHz – 20MHz: 0.348ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) package

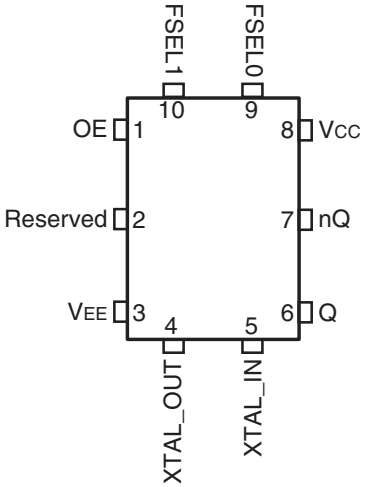
**Frequency Select Table**

| FSEL[1:0] | XTAL (MHz) | Output Frequency (MHz) | Common Application(s) |
|---|---|---|---|
| 00 | 25 | 156.25 | 10 Gigabit Ethernet XAUI |
| 01 | 25 | 625 | 10 Gigabit Ethernet, XAUI |
| 10 | 25 | 250 | Ethernet, Infiniband |
| 11 (default) | 25 | 312.5 | 10 Gigabit Ethernet XAUI, Rocket IO |

## Block Diagram




## Pin Assignment




**ICS83PN625I**

**10-Lead VFQFN**
**5mm x 7mm x 1mm package body**
**K Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | OE | | Pullup | Output enable. External pullup required for normal operation. LVCMOS/LVTTL interface levels. |
| 2 | Reserved | Reserve | | Reserved pin. Do not connect |
| 3 | $V_{EE}$ | Power | | Negative supply pin. |
| 4, 5 | XTAL_OUT XTAL_IN | Input | | Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output. This oscillator interface can also be driven by a single-ended reference clock. |
| 6, 7 | Q, nQ | Output | | Differential output pair. LVPECL interface levels. |
| 8 | $V_{CC}$ | Power | | Power supply pin. |
| 9 | FSEL0 | Input | Pullup | Output frequency select pin. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1. |
| 10 | FSEL1 | Input | Pullup | Output frequency select pin. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |

## Function Table

### Table 3. Divider Function Table

| FSEL[1:0] | M Value | N Value |
|---|---|---|
| 0 0 | 100 | ÷16 |
| 0 1 | 100 | ÷4 |
| 1 0 | 80 | ÷8 |
| 1 1 (default) | 100 | ÷8 |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 3.63V |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | <br>0V to 2V<br>-0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 39.2°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 131 | mA |

**Table 4B. Power Supply DC Characteristics,** $V_{CC}$ = 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | | 124 | mA |

**Table 4C. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 3.3V ± 5% or 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{CC}$ = 3.465V | 2 | | $V_{CC}$ + 0.3 | V |
| | | | $V_{CC}$ = 2.625V | 1.7 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{CC}$ = 3.465V | -0.3 | | 0.8 | V |
| | | | $V_{CC}$ = 2.625V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input<br>High Current | FSEL[1:0] | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input<br>Low Current | FSEL[1:0] | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4D. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V ± 5% or 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ – 1.3 | | $V_{CC}$ – 0.8 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CC}$ – 2.0 | | $V_{CC}$ – 1.6 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CC}$ – 2V.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 20 | | 25 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

# AC Electrical Characteristics

**Table 6A. AC Characteristics,** $V_{cc}$ = 3.3V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | 156.25 | | 625 | MHz |
| $t_{jit}$(cc) | Cycle-to-Cycle Jitter; NOTE 1 | | | | 10 | ps |
| $t_{jit}$(Ø) | RMS Phase Jitter (Random); NOTE 2 | 156.25MHz, Integration Range: 12kHz – 20MHz | | 0.348 | 0.5 | ps |
| | | 250MHz, Integration Range: 12kHz – 20MHz | | 0.305 | 0.5 | ps |
| | | 312.5MHz, Integration Range: 12kHz – 20MHz | | 0.338 | 0.5 | ps |
| | | 625MHz, Integration Range: 12kHz – 20MHz | | 0.343 | 0.5 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 100 | | 350 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz, 12pF resonant crystal.
NOTE: Characterized using a crystal.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Please refer to the Phase Noise plots.

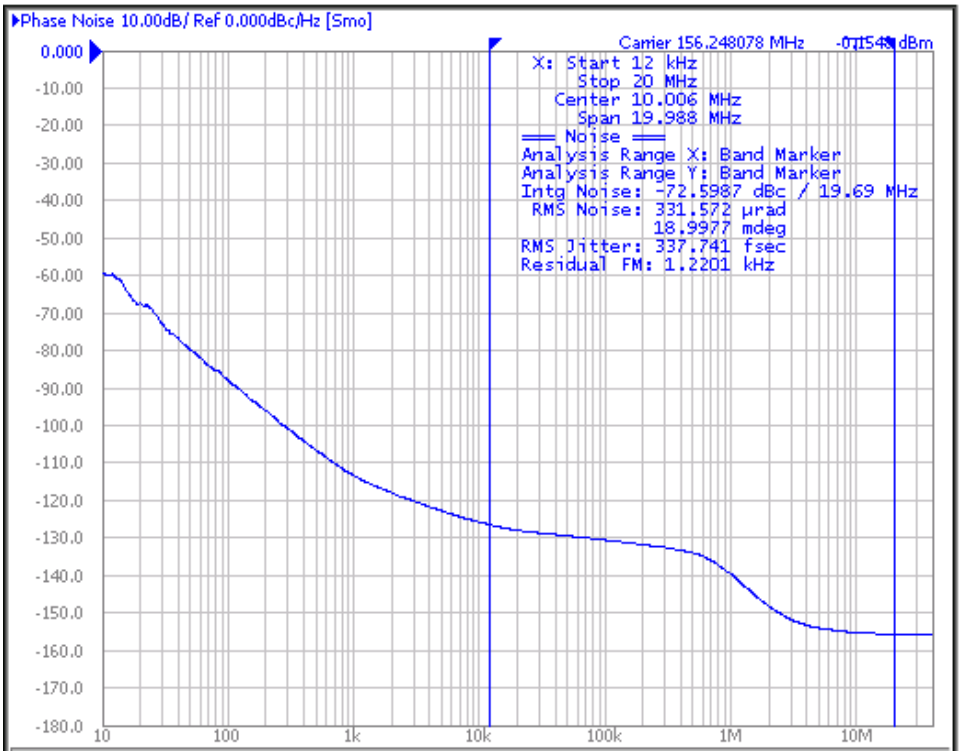
**Table 6B. AC Characteristics,** $V_{cc}$ = 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | 156.25 | | 625 | MHz |
| $t_{jit}$(cc) | Cycle-to-Cycle Jitter; NOTE 1 | | | | 12 | ps |
| $t_{jit}$(Ø) | RMS Phase Jitter (Random); NOTE 2 | 156.25MHz, Integration Range: 12kHz – 20MHz | | 0.359 | 0.5 | ps |
| | | 250MHz, Integration Range: 12kHz – 20MHz | | 0.315 | 0.5 | ps |
| | | 312.5MHz, Integration Range: 12kHz – 20MHz | | 0.349 | 0.5 | ps |
| | | 625MHz, Integration Range: 12kHz – 20MHz | | 0.351 | 0.5 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 100 | | 350 | ps |
| odc | Output Duty Cycle | | 46 | | 54 | % |

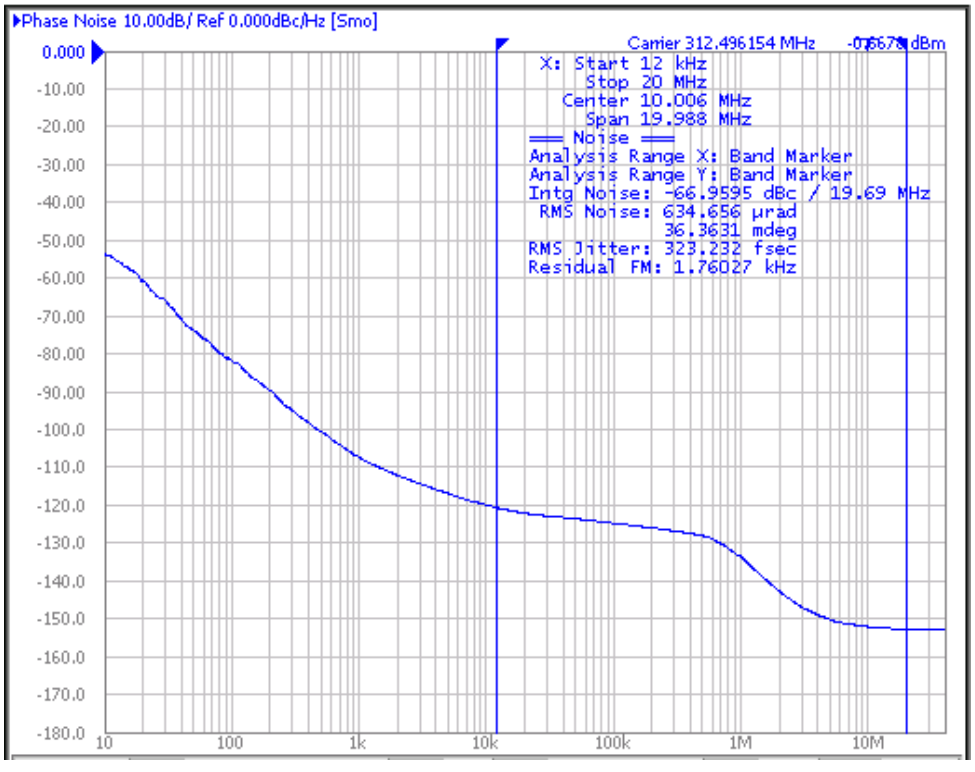
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz, 12pF resonant crystal.
NOTE: Characterized using a crystal.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Please refer to the Phase Noise plots.

## Typical Phase Noise at 156.25MHz (3.3V)

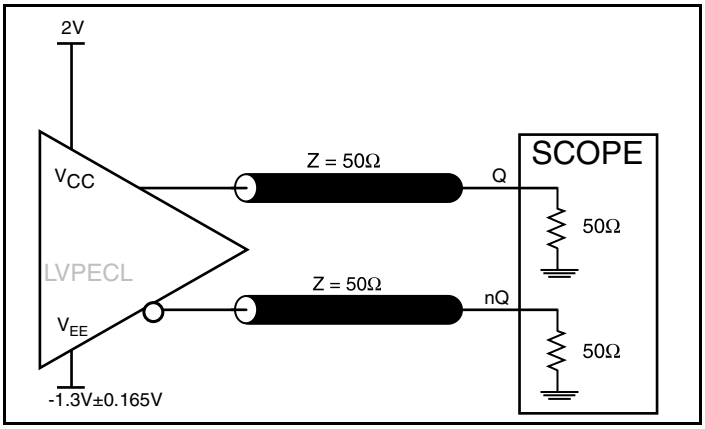



## Typical Phase Noise at 312.5MHz (3.3V)

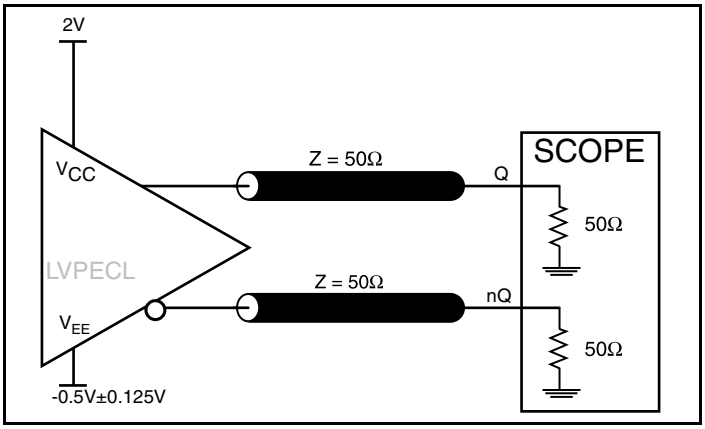


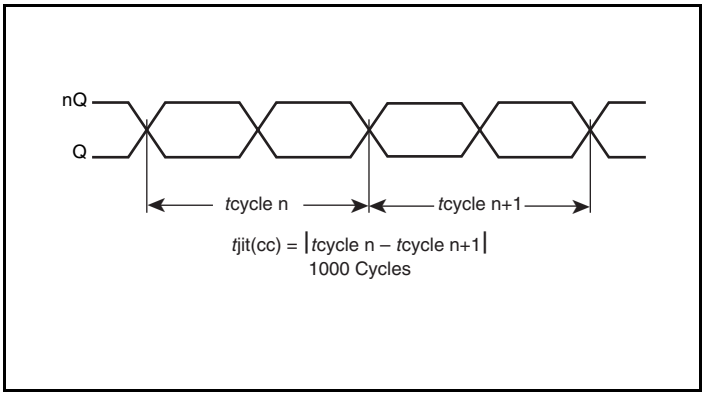
# Parameter Measurement Information



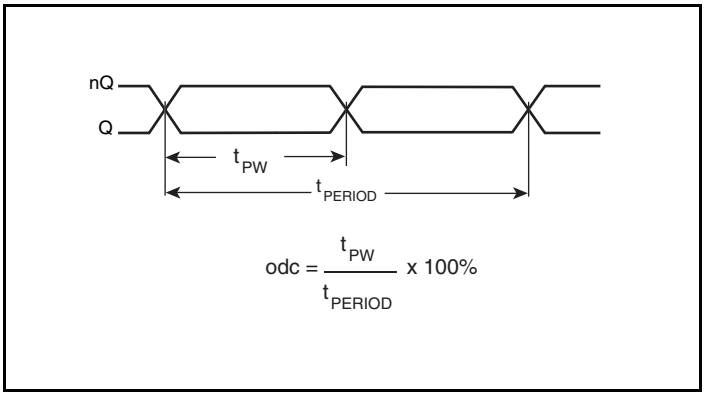

**3.3V LVPECL Output Load AC Test Circuit**



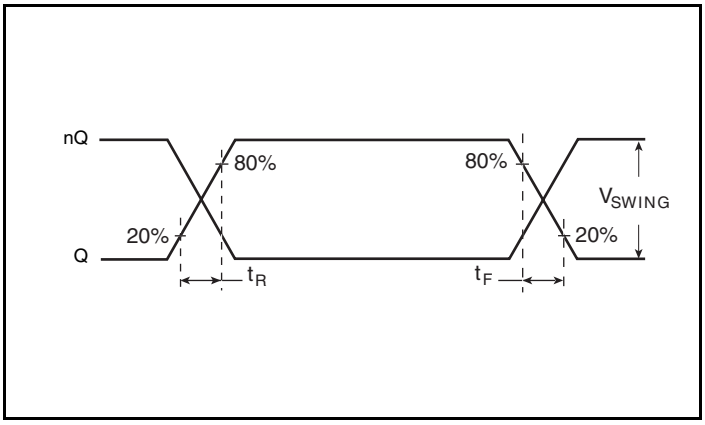

**2.5V LVPECL Output Load AC Test Circuit**



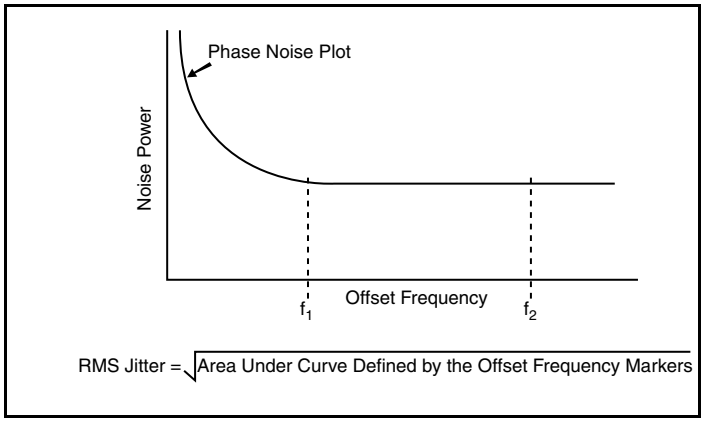

**Cycle-to-Cycle Jitter**




**Output Duty Cycle/Pulse Width/Period**




**Output Rise/Fall Time**




**RMS Phase Jitter**

# Application Information

## Recommendations for Unused Input Pins

## Inputs:

### LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

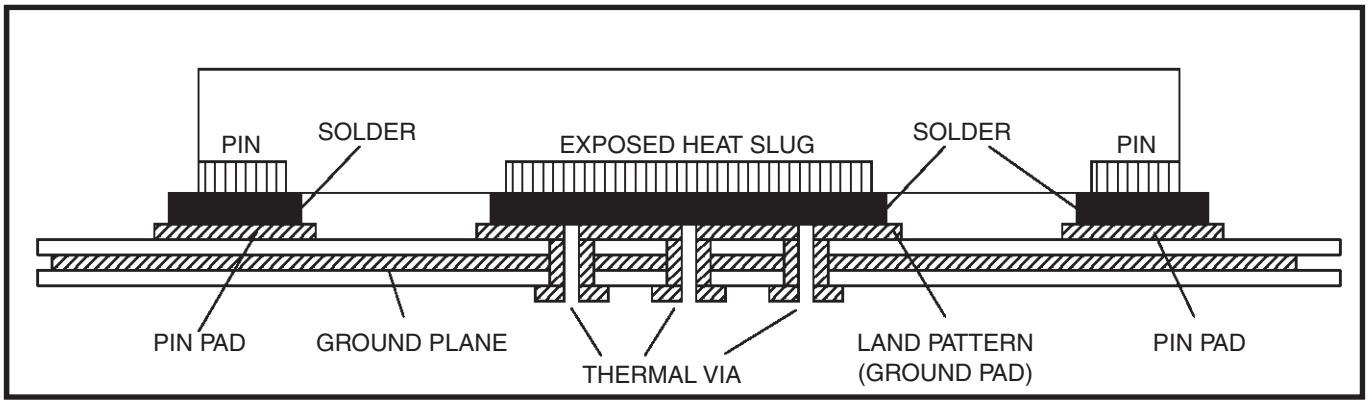



**Figure 1. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Crystal Input Interface

The ICS83PN625I has been characterized with 12pF parallel resonant crystals. The capacitor values shown in *Figure 2A* below were determined using a 25MHz, 12pF parallel resonant crystal and were chosen to minimize the ppm error. Other parallel resonant crystal's values can be used. For example, a crystal with a $C_L$ = 18pF can be used, but would require the tuning capacitors to be adjusted.

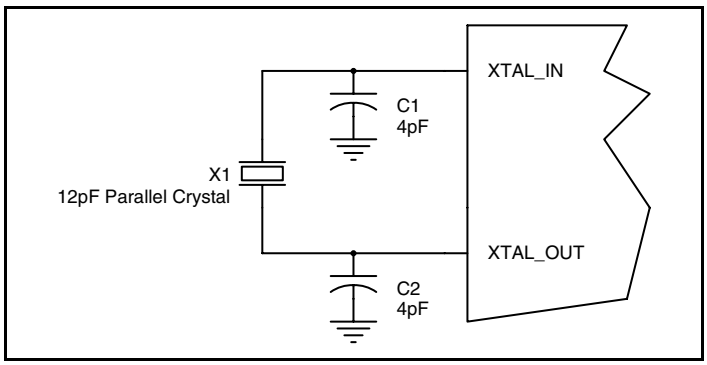



**Figure 2A. Crystal Input Interface, using 12pF crystal**

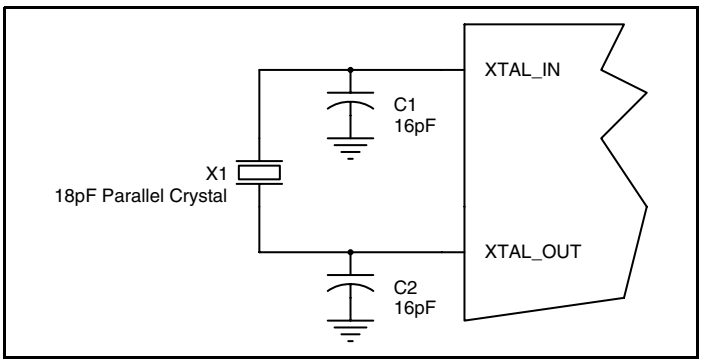



**Figure 2B. Crystal Input Interface, using 18pF crystal**

## Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

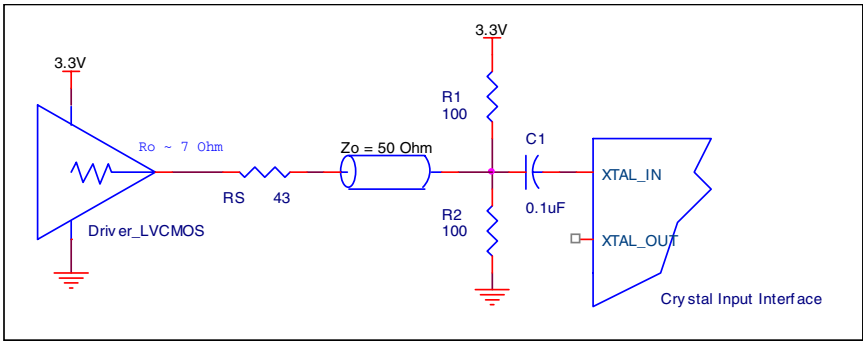



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

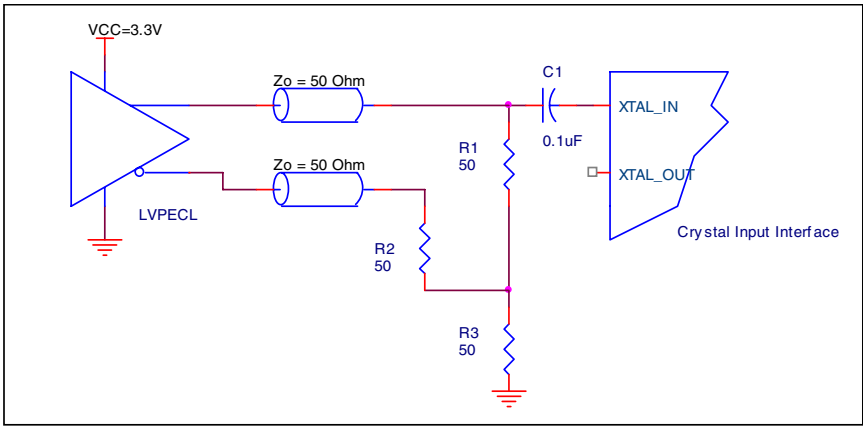



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

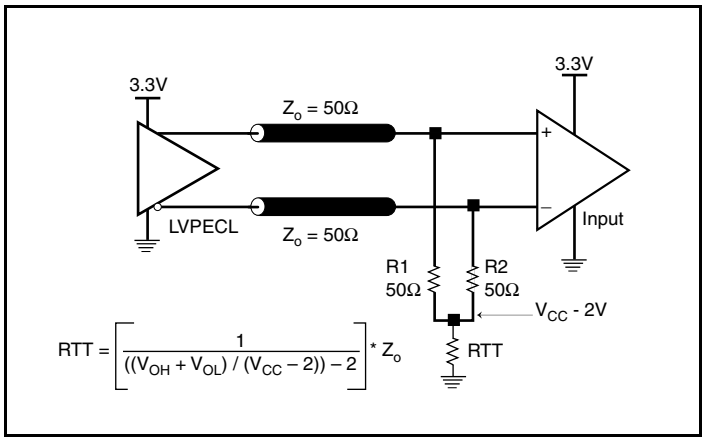



**Figure 4A. 3.3V LVPECL Output Termination**

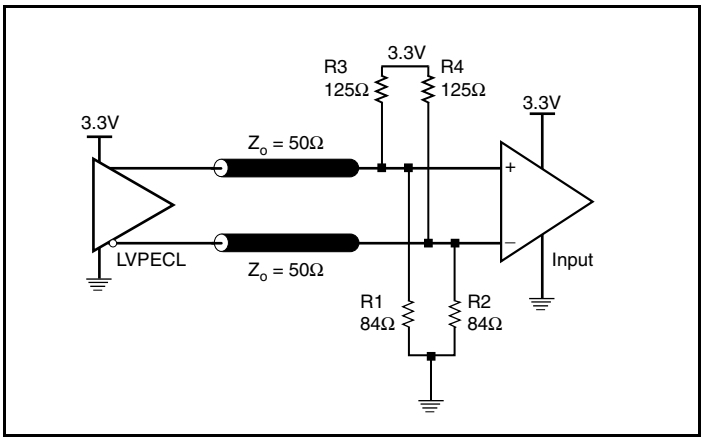



**Figure 4B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 5A* and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ – 2V. For $V_{CC}$ = 2.5V, the $V_{CC}$ – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

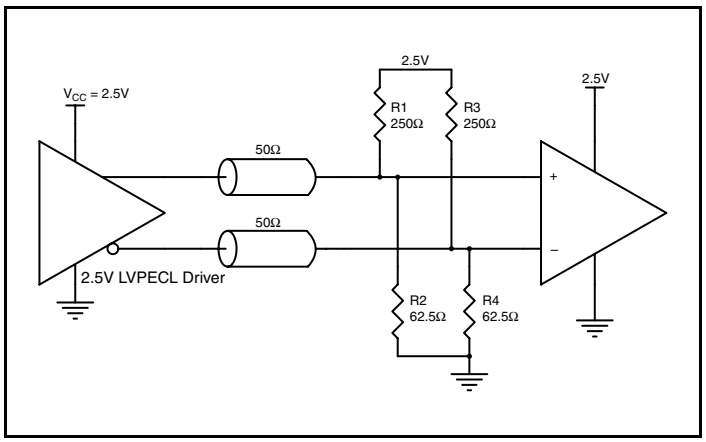



**Figure 5A. 2.5V LVPECL Driver Termination Example**

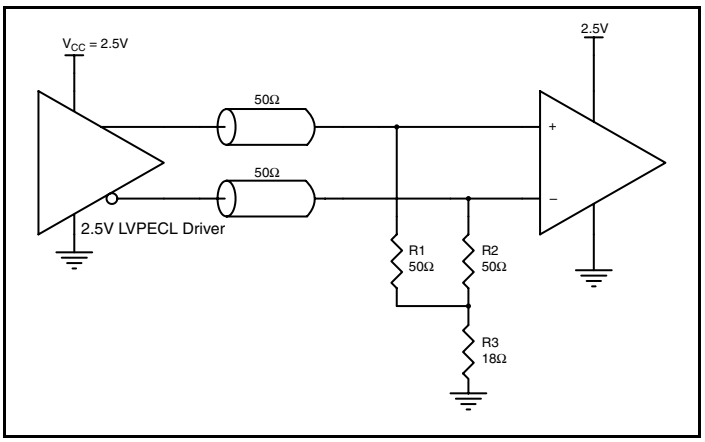



**Figure 5B. 2.5V LVPECL Driver Termination Example**

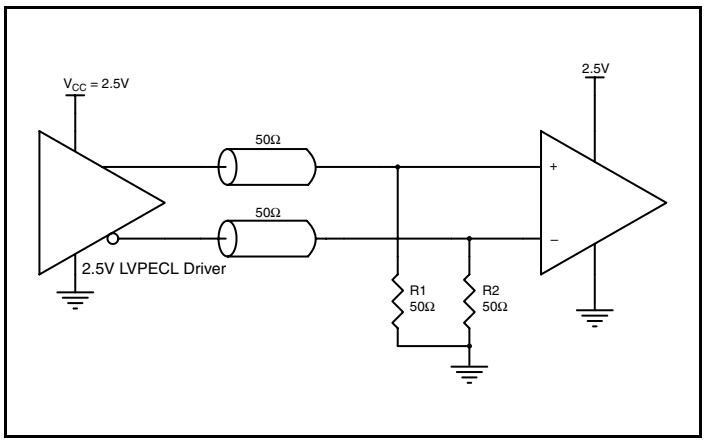



**Figure 5C. 2.5V LVPECL Driver Termination Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS83PN625I.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS83PN625I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 131mA = **453.915mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**

**Total Power**$_{\_MAX}$ (3.3V, with all outputs switching) = 453.915mW + 32mW = **485.915mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.486W * 39.2°C/W = 104.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 10 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ vs. Air Flow | |
|---|---|
| Meters per Second | **0** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.2°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

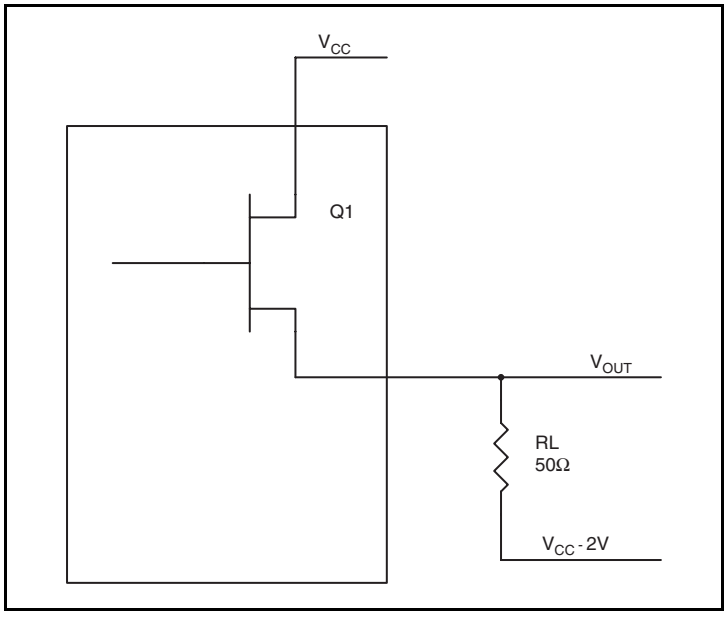



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **$V_{CC\_MAX}$ – 0.8V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.8V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **$V_{CC\_MAX}$ – 1.6V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50Ω] * 0.8V =$ **19.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50Ω] * 1.6V =$ **12.82mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 10 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | |
|---|---|
| Meters per Second | **0** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.2°C/W |

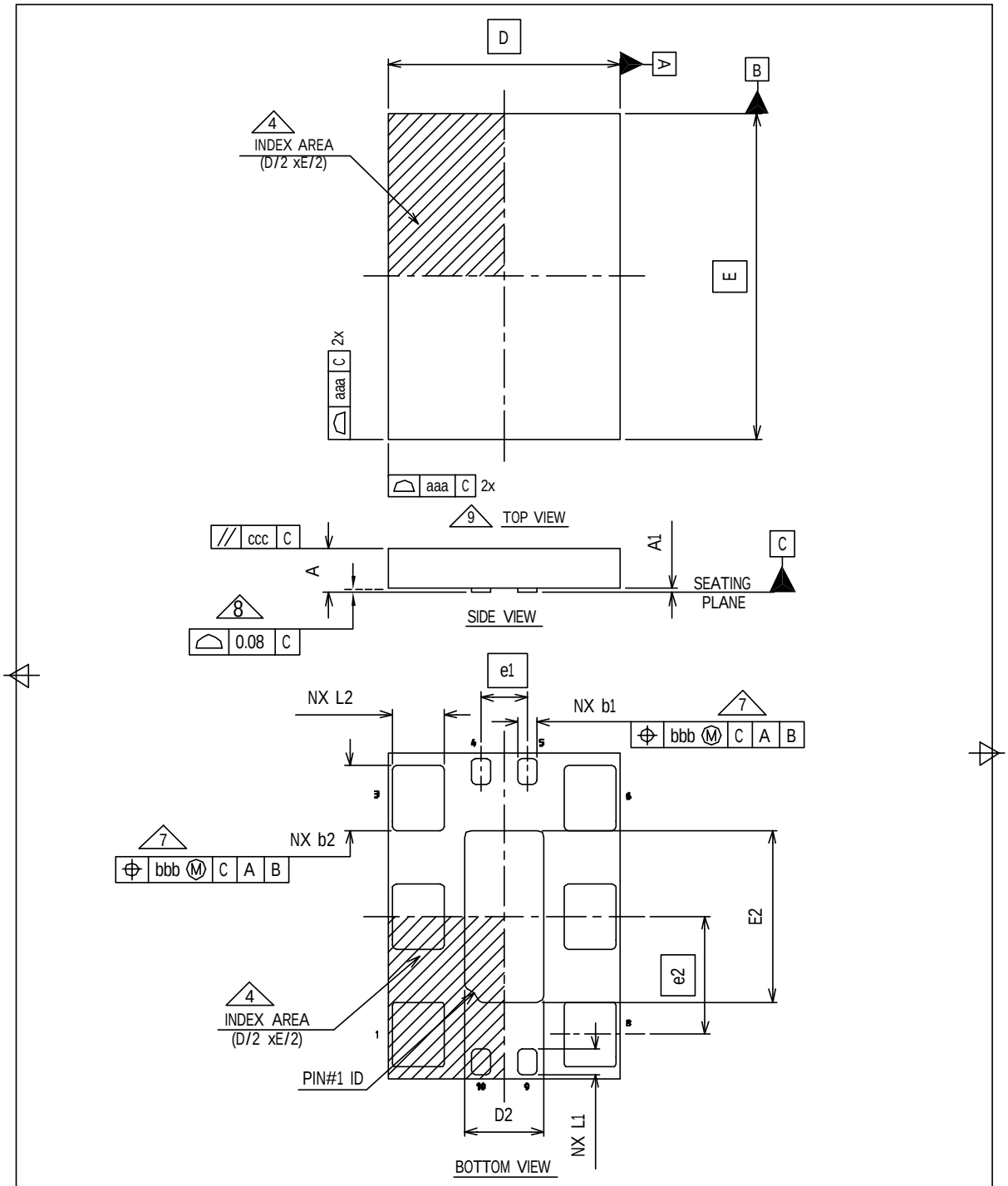
## Transistor Count

The transistor count for ICS83PN625I is: 25,212

# Package Outline

## Package Outline - K Suffix for 10-Lead VFQFN




FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

| | | | | |
|---|---|---|---|---|
| DRAFT 1 | ORIGINATOR | ZAHRUL | | DWG. NO : PKGML00305 |
| | | | | MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch |
| | ENGINEERING MANAGER | | | |
| | TOOLING MANAGER | ARAVEN | | |
| | TECH. SALES MANAGER | KANDA | | |
| | DATE | 2007-APR-18 | | Page 1 Of 4 |

# Package Outline, continued

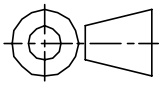
## Package Outline - K Suffix for 10-Lead VFQFN

| COMMON DIMENSION | | | | | | |
|---|---|---|---|---|---|---|
| | TOLERANCE OF FORM AND POSITION | | | | | |
| aaa | 0.15 | | | | | |
| bbb | 0.10 | | | | | |
| ccc | 0.10 | | | | | |

| COMMON DIMENSION | | | |
|---|---|---|---|
| SYMBOL | V : Very thin | | |
| | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| NOTES | 1, 2 | 1, 2 | 1, 2 |

| Summary Table | | | | |
|---|---|---|---|---|
| Lead Pitch (e1 & e2) | Lead Count | Body Size | Very Very Thin Variation | Pin #1 ID |
| 1.00/2.54 | 10 | 5.00X7.00 | VNJR-1 | R0.30 |

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

| | | | | |
|---|---|---|---|---|
| DRAFT 1 | ORIGINATOR | ZAHRUL |  | DWG. NO : PKGML00305 |
| | | | | MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch |
| | ENGINEERING MANAGER | | | |
| | TOOLING MANAGER | ARAVEN | | |
| | TECH. SALES MANAGER | KANDA | | |
| | DATE | 2007-APR-18 | | PAGE: 2 of 4 |

# Package Outline, continued

## Package Outline - K Suffix for 10-Lead VFQFN

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.

2. All dimensions are in millimeters, angles are in degrees(°).

3. N is the total number of terminals.

4. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

5. ND and NE refer to the number of terminals on each D and E side respectively.

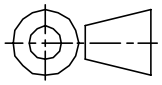
6. NJR refers to NON JEDEC REGISTERED

7. Dimension b applies to metallized terminal and is measured between 0.10mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

8. Coplanarity applies to the terminals and all other bottom surface metallization.

9. Drawing shown are for illustration only.

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

| | | | | |
|---|---|---|---|---|
| DRAFT<br>1 | ORIGINATOR | ZAHRUL |  | DWG. NO : PKGML00305 |
| | | | | MLP QUAD<br>PACKAGE OUTLINE<br>5.00x7.00 MLPQ 10LD<br>1.00/2.54 Pitch |
| | ENGINEERING MANAGER | | | |
| | TOOLING MANAGER | ARAVEN | | |
| | TECH. SALES MANAGER | KANDA | | |
| | DATE | 2007-APR-18 | | PAGE: 3 of 4 |

# Package Outline, continued

## Package Outline - K Suffix for 10-Lead VFQFN

| Variation / Symbol | | VNJR-1 | | | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D BSC | | 5.00 | | | | | | | | | |
| E BSC | | 7.00 | | | | | | | | | |
| b1 | MIN | 0.35 | | | | | | | | | |
| | NOM | 0.40 | | | | | | | | | |
| | MAX | 0.45 | | | | | | | | | |
| b2 | MIN | 1.35 | | | | | | | | | |
| | NOM | 1.40 | | | | | | | | | |
| | MAX | 1.45 | | | | | | | | | |
| D2 | MIN | 1.55 | | | | | | | | | |
| | NOM | 1.70 | | | | | | | | | |
| | MAX | 1.80 | | | | | | | | | |
| E2 | MIN | 3.55 | | | | | | | | | |
| | NOM | 3.70 | | | | | | | | | |
| | MAX | 3.80 | | | | | | | | | |
| L1 | MIN | 0.45 | | | | | | | | | |
| | NOM | 0.55 | | | | | | | | | |
| | MAX | 0.65 | | | | | | | | | |
| L2 | MIN | 1.00 | | | | | | | | | |
| | NOM | 1.10 | | | | | | | | | |
| | MAX | 1.20 | | | | | | | | | |
| N | | 10 | | | | | | | | | |
| ND | | 2 | | | | | | | | | |
| NE | | 3 | | | | | | | | | |
| NOTES | | - | | | | | | | | | |
| PAD DESIGN | | - | | | | | | | | | |

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

| | | | | |
|---|---|---|---|---|
| DRAFT | ORIGINATOR | ZAHRUL | | DWG. NO : PKGML00305 |
| | | | | MLP QUAD<br>PACKAGE OUTLINE<br>5.00x7.00 MLPQ 10LD<br>1.00/2.54 Pitch |
| 1 | ENGINEERING MANAGER | | | |
| | TOOLING MANAGER | ARAVEN | | |
| | TECH. SALES MANAGER | KANDA | | |
| | DATE | 2007-APR-18 | | PAGE: 4 of 4 |

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 83PN625DKILF | ICS3PN625DIL | “Lead-Free” 10 Lead VFQFN | Tray | -40°C to 85°C |
| 83PN625DKILFT | ICS3PN625DIL | “Lead-Free” 10Lead VFQFN | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | | 3, 15-18 | Supply Voltage, $V_{CC.}$ Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03. Updated 10-Lead VFQFN package information. | 6/02/11 |
| | | | | |

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support**
netcom@idt.com
+480-763-2056