High Voltage Capacitor Charger Controller with Regulation

FEATURES

- **Charges Any Size Capacitor**
- **Low Noise Output in Voltage Regulation Mode**
- **Stable Operation Under a No-Load Condition**
- **Integrated 2A MOSFET Gate Driver with Rail-to-Rail Operation for $V_{CC} \leq 8V$**
- **Selectable 5.6V or 10.5V Internal Gate Drive Voltage Clamp**
- **User-Selectable Over/Undervoltage Detect**
- Easily Adjustable Output Voltage
- Primary or Secondary Side Output Voltage Sense
- Wide Input V_{CC} Voltage Range (5V to 24V)
- Available in 20-Pin QFN 4mm × 5mm and 20-Lead TSSOP Packages

APPLICATIONS

- High Voltage Regulated Supply
- High Voltage Capacitor Charger
- Professional Photoflash Systems
- Emergency Strobe
- Security/Inventory Control Systems
- Detonators

DESCRIPTION

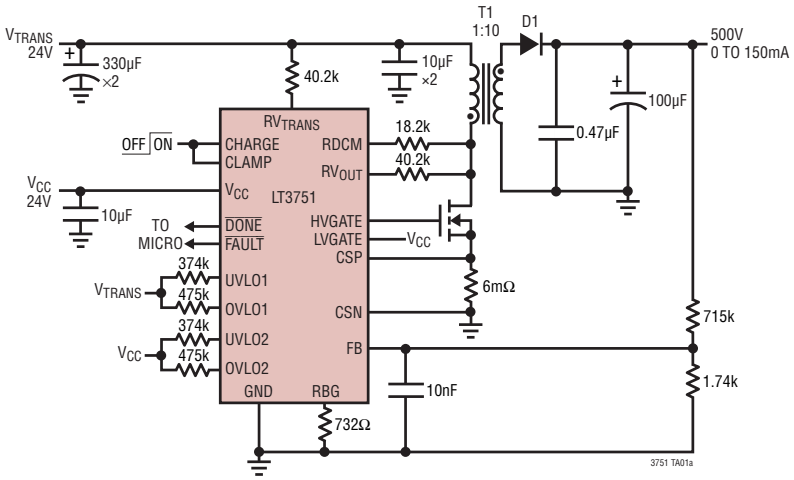
The LT®3751 is a high input voltage capable flyback controller designed to rapidly charge a large capacitor to a user-adjustable high target voltage set by the transformer turns ratio and three external resistors. Optionally, a feedback pin can be used to provide a low noise high voltage regulated output.

The LT3751 has an integrated rail-to-rail MOSFET gate driver that allows for efficient operation down to 4.75V. A low 106mV differential current sense threshold voltage accurately limits the peak switch current. Added protection is provided via user-selectable overvoltage and undervoltage lockouts for both V_{CC} and V_{TRANS}. A typical application can charge a 1000µF capacitor to 500V in less than one second.

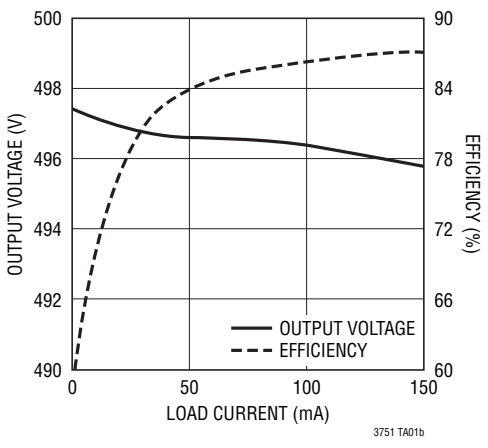
The CHARGE pin is used to initiate a new charge cycle and provides ON/OFF control. The $\overline{DONE}$ pin indicates when the capacitor has reached its programmed value and the part has stopped charging. The $\overline{FAULT}$ pin indicates when the LT3751 has shut down due to either V_{CC} or V_{TRANS} voltage exceeding the user-programmed supply tolerances.

TYPICAL APPLICATION

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



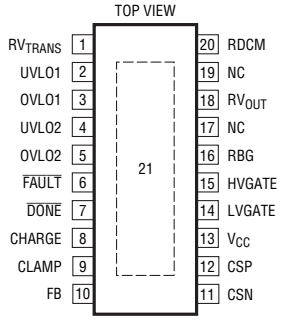
Load Regulation and Efficiency



ABSOLUTE MAXIMUM RATINGS (Note 1)

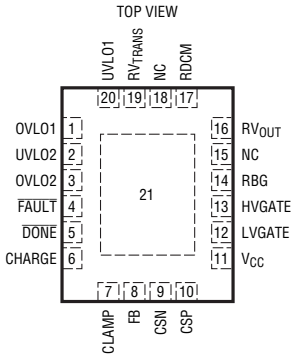
V_{CC}, CHARGE, CLAMP 24V
$\overline{DONE}$, $\overline{FAULT}$ 24V
LVGATE (Note 8) 24V
V_{CC} – LVGATE 8V
HVGATE ..... Note 9
RBG, CSP, CSN 2V
FB 5V
Current into $\overline{DONE}$ Pin ..... ±1mA
Current into $\overline{FAULT}$ Pin ..... ±1mA
Current into RV_{TRANS} Pin ..... ±1mA
Current into RV_{OUT} Pin ..... ±10mA
Current into RDCM Pin ..... ±10mA
Current into UVLO1 Pin ..... ±1mA
Current into UVLO2 Pin ..... ±1mA
Current into OVLO1 Pin ..... ±1mA
Current into OVLO2 Pin ..... ±1mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) .. –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
20-PIN (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE TIED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3751EFE#PBF	LT3751EFE#TRPBF	LT3751FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3751IFE#PBF	LT3751IFE#TRPBF	LT3751FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3751EUFD#PBF	LT3751EUFD#TRPBF	3751	20-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3751IUFD#PBF	LT3751IUFD#TRPBF	3751	20-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3751EFE	LT3751EFE#TR	LT3751FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3751IFE	LT3751IFE#TR	LT3751FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3751EUFD	LT3751EUFD#TR	3751	20-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3751IUFD	LT3751IUFD#TR	3751	20-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = CHARGE = 5V, CLAMP = 0V, unless otherwise noted. Individual 25kΩ resistors tied from 5V V_{TRANS} supply to RV_{TRANS}, RV_{OUT}, RDCM, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Voltage		●	4.75		24	V
RV_{TRANS} Voltage	(Note 3)	●	4.75		65	V
V_{CC} Quiescent Current	Not Switching, CHARGE = 5V Not Switching, CHARGE = 0.3V			5.5 0	8 1	mA µA
RV_{TRANS}, R_{DCM} Quiescent Current	(Note 4) Not Switching, CHARGE = 5V Not Switching, CHARGE = 0.3V	●	35	40 0	45 1	 µA µA
RV_{OUT} Quiescent Current	(Note 4) Not Switching, CHARGE = 5V Not Switching, CHARGE = 0.3V	●	42	47 0	52 1	 µA µA
UVLO1, UVLO2, OVLO1, OVLO2 Clamp Voltage	Measured at 1mA into Pin, CHARGE = 0V			55		V
RV_{TRANS}, RV_{OUT}, R_{DCM} Clamp Voltage	Measured at 1mA into Pin, CHARGE = 0V			60		V
CHARGE Pin Current	CHARGE = 24V CHARGE = 5V CHARGE = 0V			425 60	 1	µA µA µA
CHARGE Minimum Enable Voltage		●	1.5			V
CHARGE Maximum Disable Voltage	$I_{VCC} \leq 1\mu A$	●			0.3	V
Minimum CHARGE Pin Low Time				20		µs
One-Shot Clock Period		●	32	38	44	µs
V_{OUT} Comparator Trip Voltage	Measured at RBG Pin	●	0.955	0.98	1.005	V
V_{OUT} Comparator Overdrive	2µs Pulse Width, RV_{TRANS}, RV_{OUT} = 25kΩ R_{BG} = 0.83kΩ			20	40	mV
DCM Comparator Trip Voltage	Measured as $V_{DRAIN} - V_{TRANS}$, R_{DCM} = 25kΩ, V_{CC} = 4.75V (Note 5)		350	600	900	mV
Current Limit Comparator Trip Voltage	FB Pin = 0V FB Pin = 1.3V	● ●	100 7	106 11	112 15	mV mV
FB Pin Bias Current	Current Sourced from FB Pin, Measured at FB Pin Voltage			64	300	nA
FB Pin Voltage	(Note 6)	●	1.19	1.22	1.25	V
FB Pin Charge Mode Threshold			1.12	1.16	1.2	V
FB Pin Charge Mode Hysteresis	(Note 7)			55		mV
FB Pin Overvoltage Mode Threshold			1.29	1.34	1.38	V
FB Pin Overvoltage Hysteresis				60		mV
$\overline{DONE}$ Output Signal High	100kΩ to 5V			5		V
$\overline{DONE}$ Output Signal Low	100kΩ to 5V			40	200	mV
$\overline{DONE}$ Leakage Current	$\overline{DONE}$ = 5V			5	200	nA
$\overline{FAULT}$ Output Signal High	100kΩ to 5V			5		V
$\overline{FAULT}$ Output Signal Low	100kΩ to 5V			40	200	mV
$\overline{FAULT}$ Leakage Current	$\overline{FAULT}$ = 5V			5	200	nA
UVLO1 Pin Current	UVLO1 Pin Voltage = 1.24V	●	48.5	50	51.5	µA
UVLO2 Pin Current	UVLO2 Pin Voltage = 1.24V	●	48.5	50	51.5	µA
OVLO1 Pin Current	OVLO1 Pin Voltage = 1.24V	●	48.5	50	51.5	µA
OVLO2 Pin Current	OVLO2 Pin Voltage = 1.24V	●	48.5	50	51.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = CHARGE = 5V, CLAMP = 0V, unless otherwise noted. Individual 25kΩ resistors tied from 5V V_{TRANS} supply to RV_{TRANS}, RV_{OUT}, RDCM, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UVLO1 Threshold	Measured from Pin to GND	●	1.195	1.225	1.255	V
UVLO2 Threshold	Measured from Pin to GND	●	1.195	1.225	1.255	V
OVLO1 Threshold	Measured from Pin to GND	●	1.195	1.225	1.255	V
OVLO2 Threshold	Measured from Pin to GND	●	1.195	1.225	1.255	V
Gate Minimum High Time				0.7		µs
Gate Peak Pull-Up Current	V_{CC} = 5V, LVGATE Active V_{CC} = 12V, LVGATE Inactive			2.0 1.5		A A
Gate Peak Pull-Down Current	V_{CC} = 5V, LVGATE Active V_{CC} = 12V, LVGATE Inactive			1.2 1.5		A A
Gate Rise Time	10% → 90%, C_{GATE} = 3.3nF (Note 8) V_{CC} = 5V, LVGATE Active V_{CC} = 12V, LVGATE Inactive			 40 55		 ns ns
Gate Fall Time	90% → 10%, C_{GATE} = 3.3nF (Note 8) V_{CC} = 5V, LVGATE Active V_{CC} = 12V, LVGATE Inactive			 30 30		 ns ns
Gate High Voltage	(Note 8): V_{CC} = 5V, LVGATE Active V_{CC} = 12V, LVGATE Inactive V_{CC} = 12V, LVGATE Inactive, CLAMP Pin = 5V V_{CC} = 24V, LVGATE Inactive		 4.98 10 5 10	 5 10.5 5.6 10.5	 11.5 6.5 11.5	 V V V V
Gate Turn-Off Propagation Delay	C_{GATE} = 3.3nF 25mV Overdrive Applied to CSP Pin			180		ns
Gate Voltage Overshoot				500		mV
CLAMP Pin Threshold				1.6		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3751E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT3751I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: A 60V internal clamp is connected to RV_{TRANS}, RDCM, RV_{OUT}, UVLO1, UVLO2, OVLO1 and OVLO2. Resistors should be used such that the pin currents do not exceed the Absolute Maximum Ratings.

Note 4: Currents will increase as pin voltages are taken higher than the internal clamp voltage.

Note 5: Refer to Block Diagram for V_{TRANS} and V_{DRAIN} definitions.

Note 6: Low noise regulation of the output voltage requires a resistive voltage divider from output voltage to FB pin. FB pin should not be grounded in this configuration. Refer to the Typical Application diagram for proper FB pin configuration.

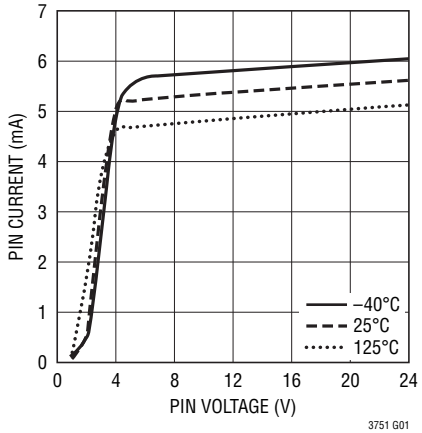
Note 7: The feedback pin has built-in hysteresis that defines the boundary between charge-only mode and low noise regulation mode.

Note 8: LVGATE should be used in parallel with HVGATE when V_{CC} is less than or equal to 8V (LVGATE active). When not in use, LVGATE should be tied to V_{CC} (LVGATE inactive).

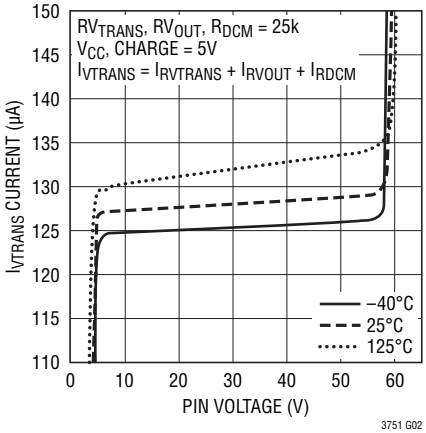
Note 9: Do not apply a positive or negative voltage or current source to HVGATE, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

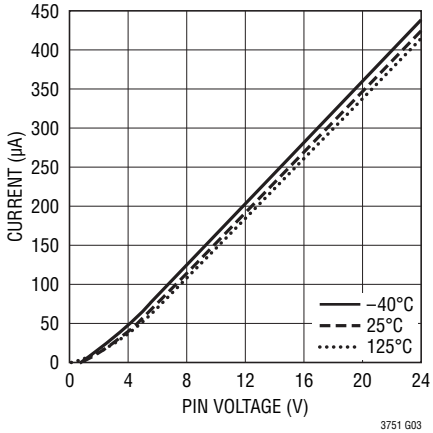
V_{CC} Pin Current



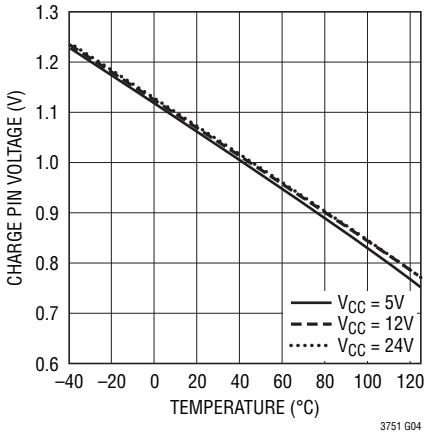
V_{TRANS} Supply Current



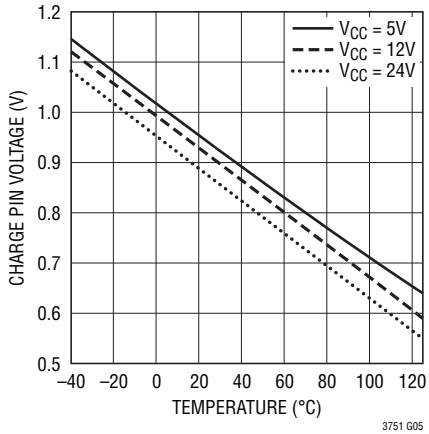
CHARGE Pin Current



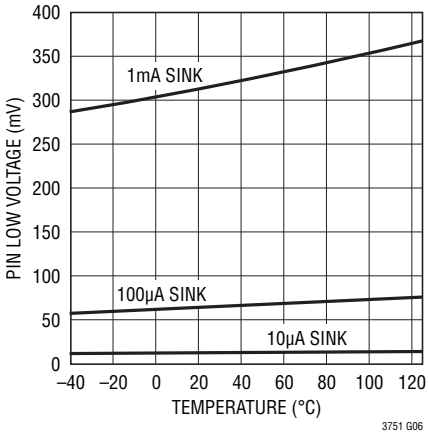
CHARGE Pin Minimum Enable Voltage



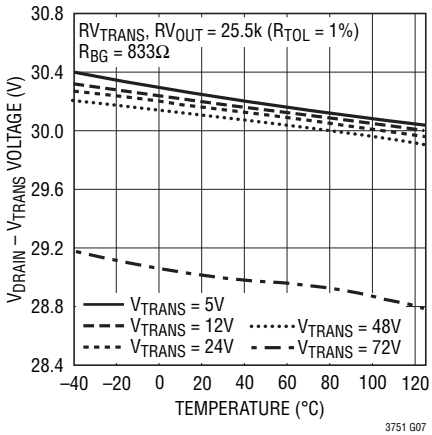
CHARGE Pin Maximum Disable Voltage



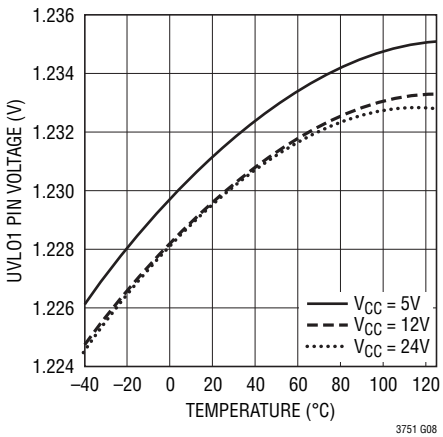
$\overline{DONE}$, $\overline{FAULT}$ Pin Voltage Low



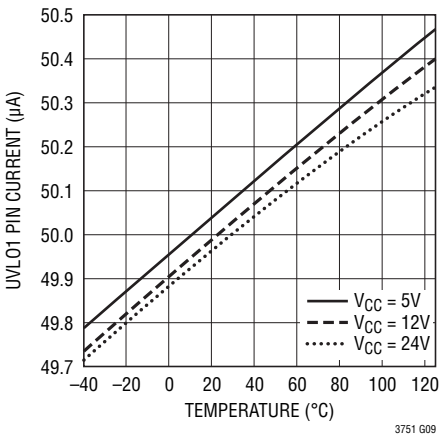
V_{OUT} Comparator Trip Voltage



UVLO1 Trip Voltage

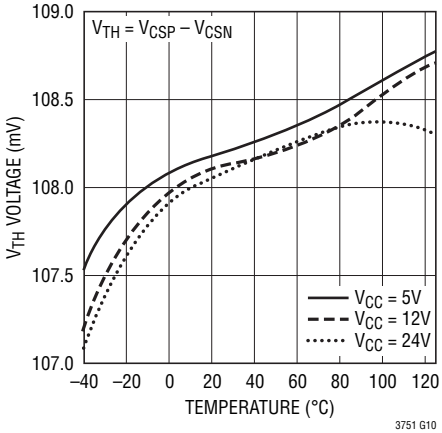


UVLO1 Trip Current

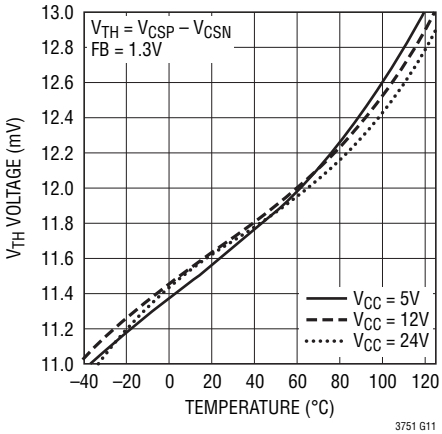


TYPICAL PERFORMANCE CHARACTERISTICS

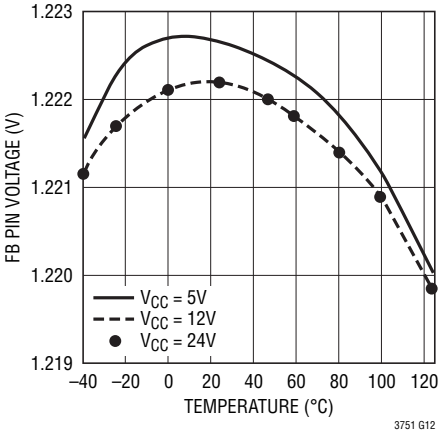
Current Comparator Trip Voltage (Charge Mode)



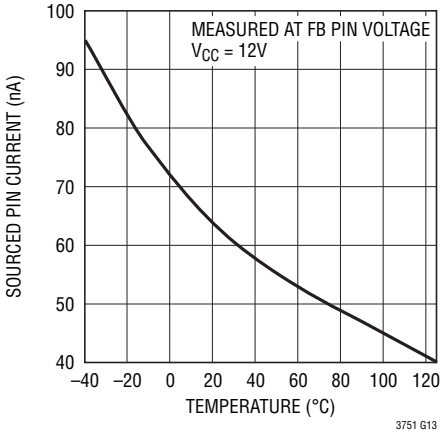
Current Comparator Minimum Trip Voltage (Regulation Mode)



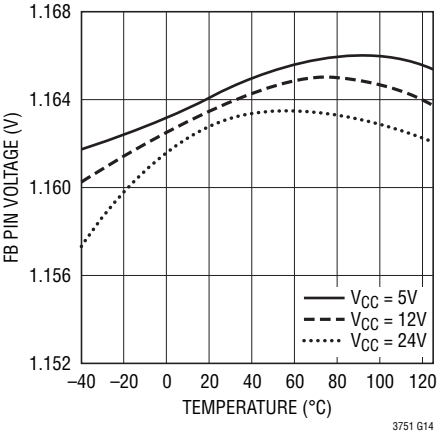
FB Pin Voltage



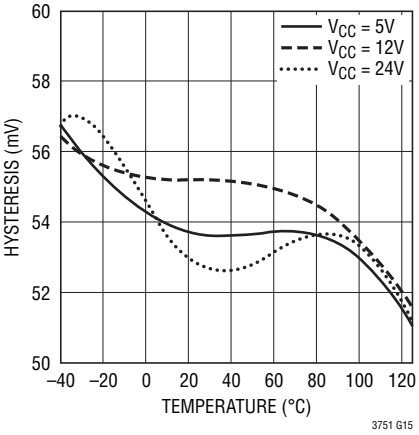
FB Pin Bias Current



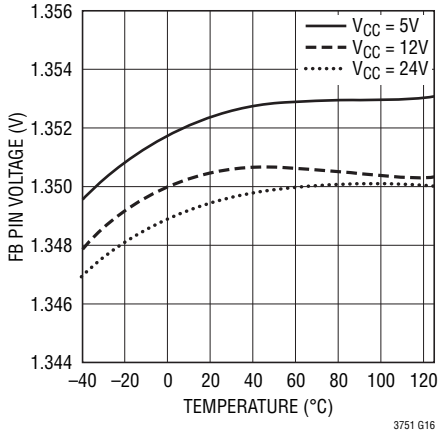
FB Pin Regulation Mode Threshold



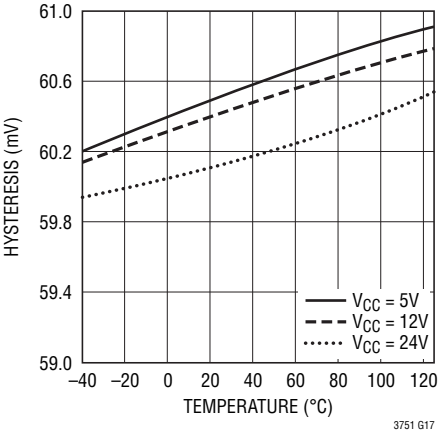
FB Pin Regulation Mode Hysteresis



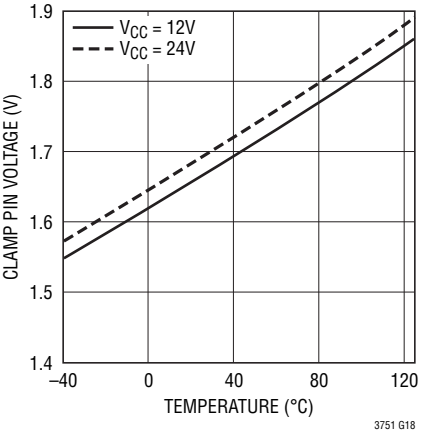
FB Pin Overvoltage Mode Threshold Voltage



FB Pin Overvoltage Mode Hysteresis

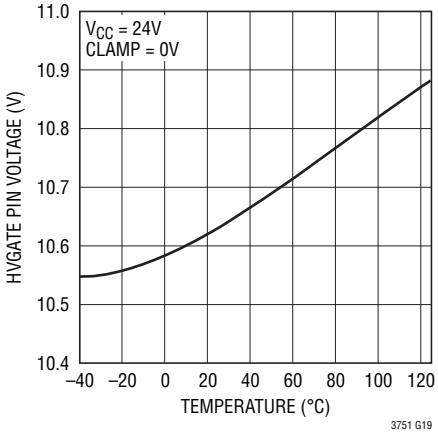


CLAMP Pin Threshold

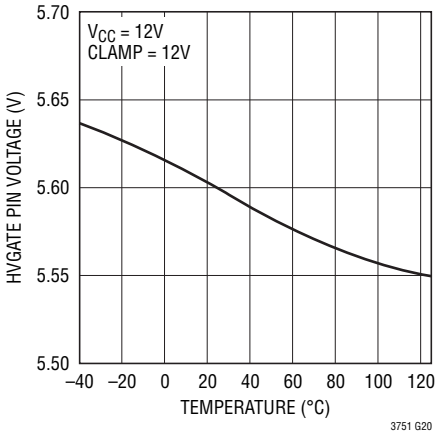


TYPICAL PERFORMANCE CHARACTERISTICS

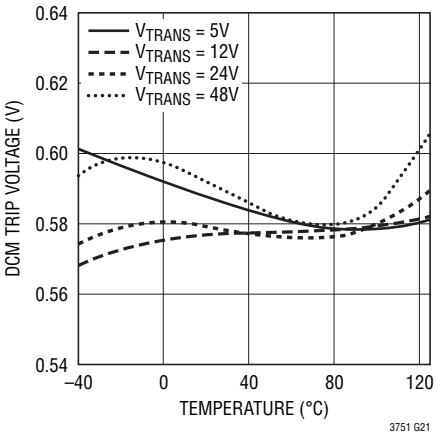
HVGATE Pin Clamp Voltage



HVGATE Pin Clamp Voltage



DCM Trip Voltage ($V_{DRAIN} – V_{TRANS}$), RV_{TRANS} = RDCM = 25kΩ



PIN FUNCTIONS (TSSOP/QFN)

RV_{TRANS} (Pin 1/Pin 19): Transformer Supply Sense Pin. Connect a resistor between the RV_{TRANS} pin and the V_{TRANS} supply. Refer to Table 2 for proper sizing of the RV_{TRANS} resistor. The minimum operation voltage for V_{TRANS} is 4.75V.

UVLO1 (Pin 2/Pin 20): V_{TRANS} Undervoltage Lockout Pin. Senses when V_{TRANS} drops below:

$$V_{UVLO1} = 1.225 + 50\mu A \bullet R_{UVLO1}$$

and trips the $\overline{FAULT}$ latch low, disabling switching. After V_{TRANS} rises above V_{UVLO1}, toggling the CHARGE pin reactivates switching.

OVLO1 (Pin 3/Pin 1): V_{TRANS} Overvoltage Lockout Pin. Senses when V_{TRANS} rises above:

$$V_{OVLO1} = 1.225 + 50\mu A \bullet R_{OVLO1}$$

and trips the $\overline{FAULT}$ latch low, disabling switching. After V_{TRANS} drops below V_{OVLO1}, toggling the CHARGE pin reactivates switching.

UVLO2 (Pin 4/Pin 2): V_{CC} Undervoltage Lockout Pin. Senses when V_{CC} drops below:

$$V_{UVLO2} = 1.225 + 50\mu A \bullet R_{UVLO2}$$

and trips the $\overline{FAULT}$ latch low, disabling switching. After V_{CC} rises above V_{UVLO2}, toggling the CHARGE pin reactivates switching.

OVLO2 (Pin 5/Pin 3): V_{CC} Overvoltage Lockout Pin. Senses when V_{CC} rises above:

$$V_{OVLO2} = 1.225 + 50\mu A \bullet R_{OVLO2}$$

and trips the $\overline{FAULT}$ latch low, disabling switching. After V_{CC} drops below V_{OVLO2}, toggling the CHARGE pin reactivates switching.

$\overline{FAULT}$ (Pin 6/Pin 4): Open Collector Indication Pin. When either V_{TRANS} or V_{CC} exceeds the user-selected voltage range, or an internal UVLO condition occurs, a transistor turns on. The part will stop switching. This pin needs a proper pull-up resistor or current source.

PIN FUNCTIONS

$\overline{\text{DONE}}$ (Pin 7/ Pin 5): Open Collector Indication Pin. When the target output voltage (charge mode) is reached or the $\overline{\text{FAULT}}$ pin goes low, a transistor turns on. This pin needs a proper pull-up resistor or current source.

CHARGE (Pin 8/Pin 6): Charge Pin. Initiates a new charge cycle (charge mode) or enables the part (regulation mode) when driven higher than 1.5V. Bring this pin below 0.3V to discontinue charging and put the part into shutdown. Turn-on ramp rates should be between 10ns to 10ms. CHARGE pin should not be directly ramped with V_{CC} or LT3751 may not properly initialize.

CLAMP (Pin 9/Pin 7): Internal Clamp Voltage Selection Pin. Tie this pin to V_{CC} to activate the internal 5.6V gate driver clamp. Tie this pin to ground to activate the internal 10.5V gate driver clamp.

FB (Pin 10/Pin 8): Feedback Regulation Pin. Use this pin to achieve low noise voltage regulation. FB is internally regulated to 1.22V when a resistive divider is tied from this pin to the output. FB pin should not float. Tie FB pin to either a resistor divider or ground.

CSN (Pin 11/Pin 9): Negative Current Sense Pin. Senses external NMOS source current. Connect to local R_{SENSE} ground connection for proper Kelvin sensing. The current limit is set by $106mV/R_{SENSE}$.

CSP (Pin 12/Pin 10): Positive Current Sense Pin. Senses NMOS source current. Connect the NMOS source terminal and the current sense resistor to this pin. The current limit is fixed at $106mV/R_{SENSE}$ in charge mode. The current limit can be reduced to a minimum $11mV/R_{SENSE}$ in regulation mode.

V_{CC} (Pin 13/Pin 11): Input Supply Pin. Must be locally bypassed with high grade (X5R or better) ceramic capacitor. The minimum operating voltage for V_{CC} is 4.75V.

LVGATE (Pin 14/Pin 12): Low Voltage Gate Pin. Connect the NMOS gate terminal to this pin when operating V_{CC} below 8V. The internal gate driver will drive the voltage to the V_{CC} rail. When operating V_{CC} higher than 8V, tie this pin directly to V_{CC}.

HVGATE (Pin 15/Pin 13): High Voltage Gate Pin. Connect NMOS gate terminal to this pin for all V_{CC} operating voltages. Internal gate driver will drive the voltage to within V_{CC} – 2V during each switch cycle.

RBG (Pin 16/Pin 14): Bias Generation Pin. Generates a bias current set by $0.98V/R_{BG}$. Select R_{BG} to achieve desired resistance for R_{DCM}, RV_{OUT}, and RV_{TRANS}.

NC (Pins 17, 19/Pins 15, 18): No Connection.

RV_{OUT} (Pin 18/Pin 16): Output Voltage Sense Pin. Develops a current proportional to the output capacitor voltage. Connect a resistor between this pin and the drain of NMOS such that:

$$V_{OUT} = 0.98 \bullet N \bullet \left(\frac{RV_{OUT}}{R_{BG}} \right) - V_{DIODE}$$

when RV_{OUT} is set equal to RV_{TRANS}, otherwise:

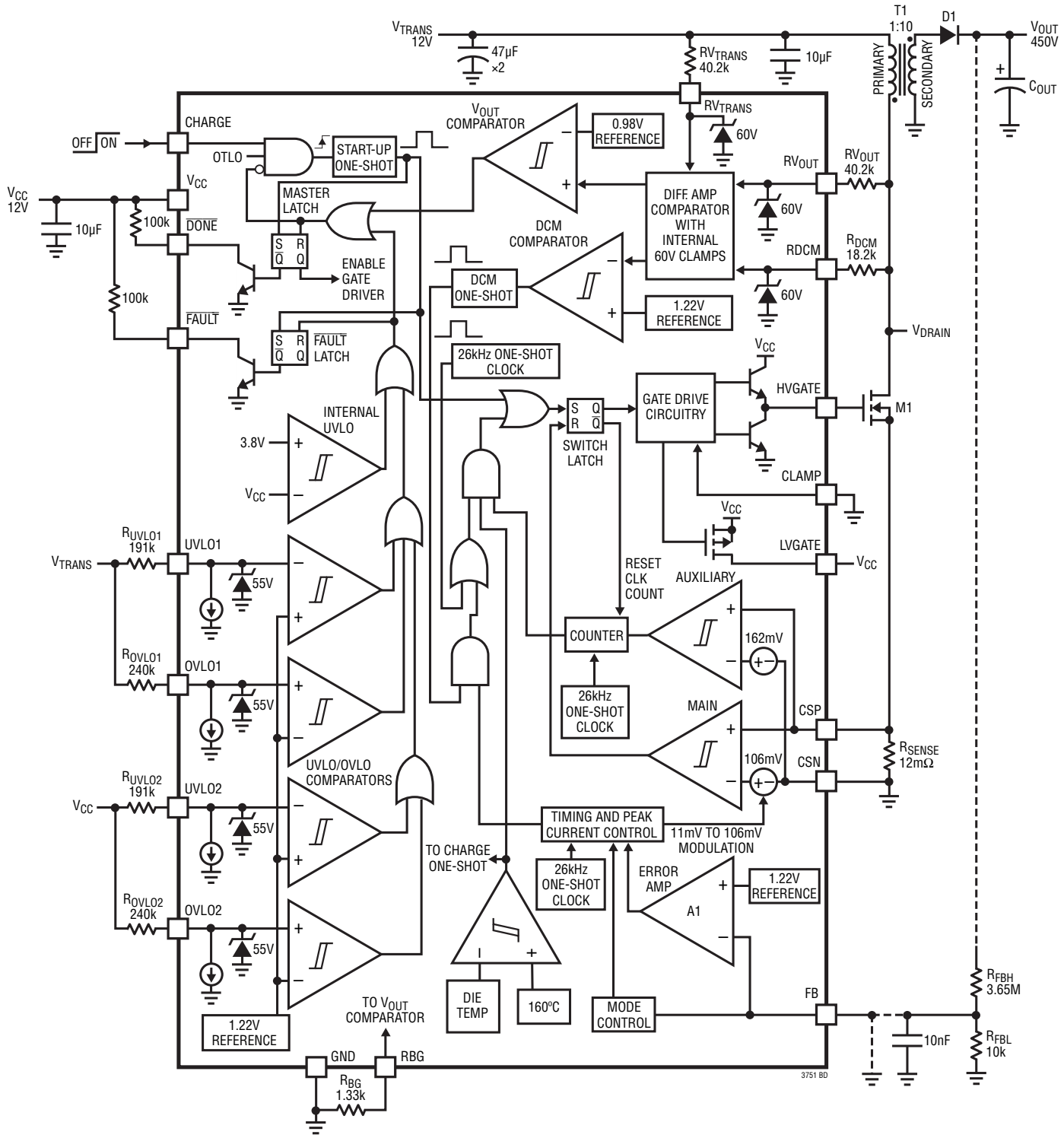
$$V_{OUT} = N \bullet \left[0.98 \bullet \frac{RV_{OUT}}{R_{BG}} + V_{TRANS} \left(\frac{RV_{OUT}}{RV_{TRANS}} - 1 \right) \right] - V_{DIODE}$$

where V_{DIODE} = forward voltage drop of diode D1 (refer to the Block Diagram).

RDCM (Pin 20/Pin 17): Discontinuous Mode Sense Pin. Senses when the external NMOS drain is equal to $20\mu A \bullet R_{DCM} + V_{TRANS}$ and initiates the next switch cycle. Place a resistor equal to 0.45 times the resistor on the RV_{TRANS} pin between this pin and V_{DRAIN}.

GND (Pin 21/Pin 21): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM



OPERATION

The LT3751 can be used as either a fast, efficient high voltage capacitor charger controller or as a high voltage, low noise voltage regulator. The FB pin voltage determines one of the three primary modes: charge mode, low noise regulation, or no-load operation (see Figure 1).

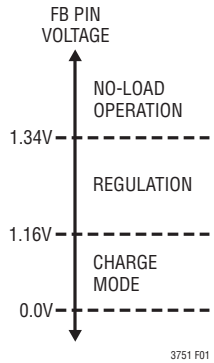


Figure 1. FB Pin Modes

CHARGE MODE

When the FB pin voltage is below 1.16V, the LT3751 acts as a rapid capacitor charger. The charging operation has four basic states for charge mode steady-state operation (see Figure 2).

1. Start-Up

The first switching cycle is initiated approximately 2µs after the CHARGE pin is raised high. During this phase, the start-up one-shot enables the master latch turning on the external NMOS and beginning the first switching cycle. After start-up, the master latch will remain in the switching-enable state until the target output voltage is reached or a fault condition occurs.

The LT3751 utilizes circuitry to protect against transformer primary current entering a runaway condition and remains in start-up mode until the DCM comparator has enough headroom. Refer to the Start-Up Protection section for more detail.

2. Primary-Side Charging

When the NMOS switch latch is set, and depending on the use of LVGATE, the gate driver rapidly charges the gate pin to V_{CC} – 2V in high voltage applications or directly to V_{CC} in low voltage applications (refer to the Application

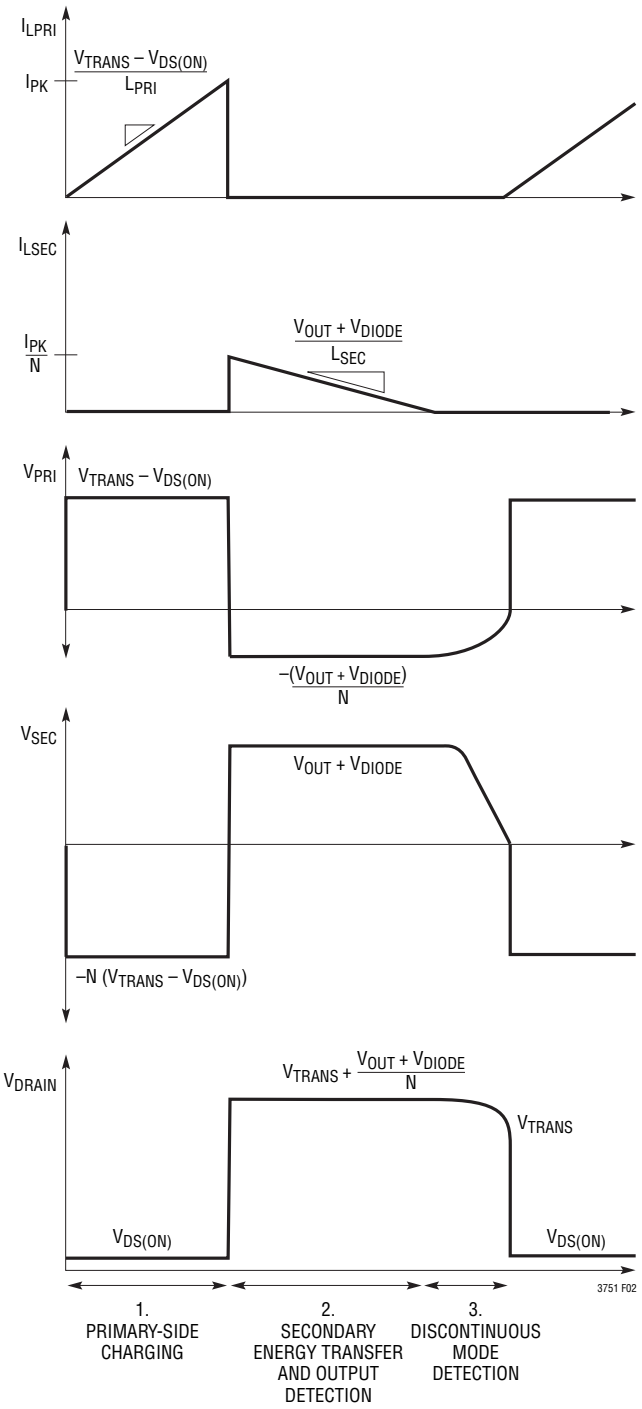


Figure 2. Idealized Charging Waveforms

OPERATION

Information section for proper use of LVGATE). With the gate driver output high, the external NMOS turns on, forcing $V_{TRANS} – V_{DS(ON)}$ across the primary winding. Consequently, current in the primary coil rises linearly at a rate $(V_{TRANS} – V_{DS(ON)})/L_{PRI}$. The input voltage is mirrored on the secondary winding $–N • (V_{TRANS} – V_{DS(ON)})$ which reverse-biases the diode and prevents current flow in the secondary winding. Thus, energy is stored in the core of the transformer.

3. Secondary Energy Transfer

When current limit is reached, the current limit comparator resets the NMOS switch latch and the device enters the third phase of operation, secondary energy transfer. The energy stored in the transformer core forward-biases the diode and current flows into the output capacitor. During this time, the output voltage (neglecting the diode drop) is reflected back to the primary coil. If the target output voltage is reached, the V_{OUT} comparator resets the master latch and the $\overline{DONE}$ pin goes low. Otherwise, the device enters the next phase of operation.

4. Discontinuous Mode Detection

During secondary energy transfer to the output capacitor, $(V_{OUT} + V_{DIODE})/N$ will appear across the primary winding. A transformer with no energy cannot support a DC voltage, so the voltage across the primary will decay to zero. In other words, the drain of the NMOS will ring down from $V_{TRANS} + (V_{OUT} + V_{DIODE})/N$ to V_{TRANS}. When the drain voltage falls to $V_{TRANS} + 20\mu A • R_{DCM}$, the DCM comparator sets the NMOS switch latch and a new switch cycle begins. Steps 2-4 continue until the target output voltage is reached.

Start-Up Protection

The LT3751 at start-up, when the output voltage is very low (or shorted), usually does not have enough V_{DRAIN} node voltage to trip the DCM comparator. The part in start-up mode uses the internal 26kHz clock and an auxiliary current comparator. Figure 3 shows a simplified block diagram of the start-up circuitry.

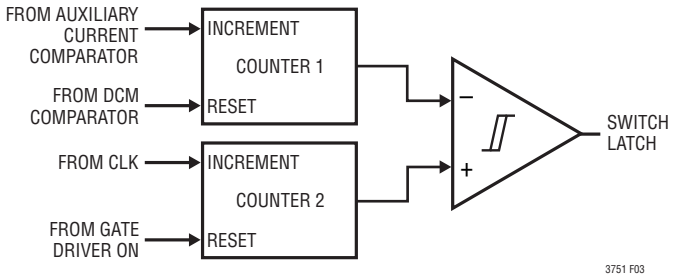


Figure 3. Start-Up Protection Circuitry

Toggling the CHARGE pin always generates a start-up one-shot to turn on the external switch, initiating the charging process. After the start-up one-shot, the LT3751 waits for either the DCM comparator to generate a one-shot or the output of the start-up protection circuitry going high, which ever comes first. If the switch drain node, V_{DRAIN}, is below the DCM comparator threshold (see Entering Normal Boundary Mode), the DCM comparator will never fire and the start-up circuitry is dominant.

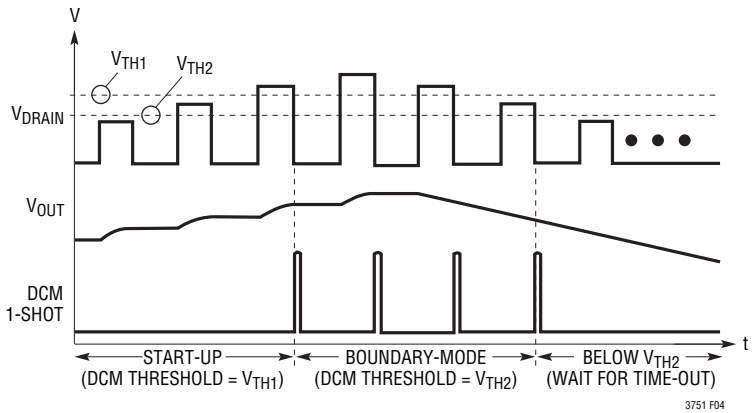


Figure 4. DCM Comparator Thresholds

OPERATION

At very low output voltages, the boundary-mode switching cycle period increases significantly such that the energy stored in the transformer core is not depleted before the next clock cycle. In this situation, the clock may initiate another switching cycle before the secondary winding current reaches zero and cause the LT3751 to enter continuous-mode conduction. Normally, this is not a problem; however, if the secondary energy transfer time is much longer than the CLK period, significant primary current overshoot can occur. This is due to the non-zero starting point of the primary current when the switch turns on and the finite speed of the current comparator.

The LT3751 startup circuitry adds an auxiliary current comparator with a trip level 50% higher than the nominal trip level. Every time the auxiliary current comparator trips, the required clock count between switching cycles is incremented by one. This allows more time for secondary energy transfer.

Counter 1 in Figure 3 is set to its maximum count when the first DCM comparator one-shot is generated. If no DCM one-shot is initiated in normal boundary-mode operation during a maximum count of approximately 500µs, the LT3751 re-enters start-up mode and the count is returned to zero.

Note that Counter 1 is initialized to zero at start-up. Thus, the output of the startup circuitry will go high after one clock cycle. Counter 2 is reset when the gate driver goes high. This repeats until either the auxiliary current comparator increments the required clock count or until V_{DRAIN} is high enough to sustain normal operation described in steps 2 through 4 in the previous section.

Entering Normal Boundary Mode

The LT3751 has two DCM comparator thresholds that are dependent on what mode the part is in, either start-up mode or normal boundary-mode, and the state of the mode latch. For boundary-mode switching, the LT3751 requires the DCM sense voltage (V_{DRAIN}) to exceed V_{TRANS} by the ΔDCM comparator threshold, ΔV_{DRAIN}:

$$\Delta V_{DRAIN} = (40\mu A + I_{OFFSET}) \bullet R_{DCM} - 40\mu A \bullet RV_{TRANS}$$

where I_{OFFSET} is mode dependent. The DCM one-shot signal is negative edge triggered by the switch node, V_{DRAIN}, and indicates that the energy in the secondary winding has depleted. For this to happen, V_{DRAIN} must exceed $V_{TRANS} + \Delta V_{DRAIN}$ prior to its negative edge; otherwise, the DCM comparator will not generate a one-shot to initiate the next switching cycle. The part would remain stuck in this state indefinitely; however, the LT3751 uses the start-up protection circuitry to jumpstart switching if the DCM comparator does not generate a one-shot after a maximum time-out of 500µs.

Figure 4 shows a typical V_{DRAIN} node waveform with a test circuit voltage clamp applied to the output. V_{TH1} is the start-up threshold and is set internally by forcing I_{OFFSET} to 40µA. Once the first DCM one-shot is initiated, the mode latch is set to boundary-mode. The mode latch then sets the clock count to maximum (500µs) and lowers the DCM comparator threshold to V_{TH2} (I_{OFFSET} = 20µA). This provides needed hysteresis between start-up mode and boundary-mode operation.

LOW NOISE REGULATION

Low noise voltage regulation can be achieved by adding a resistive divider from the output node to the LT3751 FB pin. At start-up (FB pin below 1.16V), the LT3751 enters the charge mode to rapidly charge the output capacitor. Once the FB pin is within the threshold range of 1.16V to 1.34V, the part enters into low noise regulation. The switching methodology in regulation mimics that used in the capacitor charging mode, but with the addition of peak current and duty cycle control techniques. Figure 5 shows the steady state operation for both regulation techniques. Figure 6 shows how both techniques are combined to provide stable, low noise operation over a wide load and supply range.

During heavy load conditions, the LT3751 sets the peak primary current to its maximum value, 106mV/R_{SENSE} and sets the maximum duty cycle to approximately 95%. This allows for maximum power delivery. At very light loads, the opposite occurs, and the LT3751 reduces the peak primary current to approximately one tenth its maximum value while modulating the duty cycle below 10%. The LT3751 controls moderate loads with a combination of peak current mode control and duty cycle control.

OPERATION

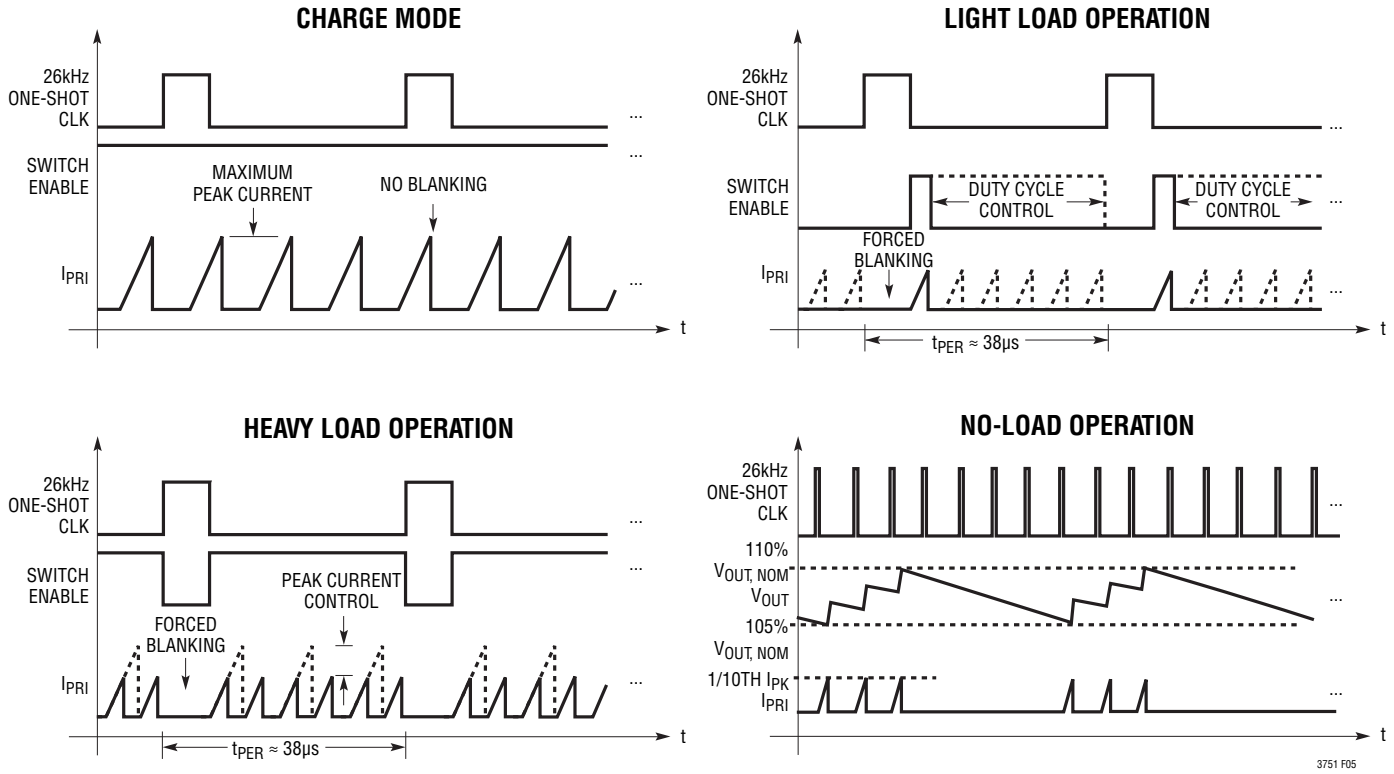


Figure 5. Modes of Operation (Steady State)

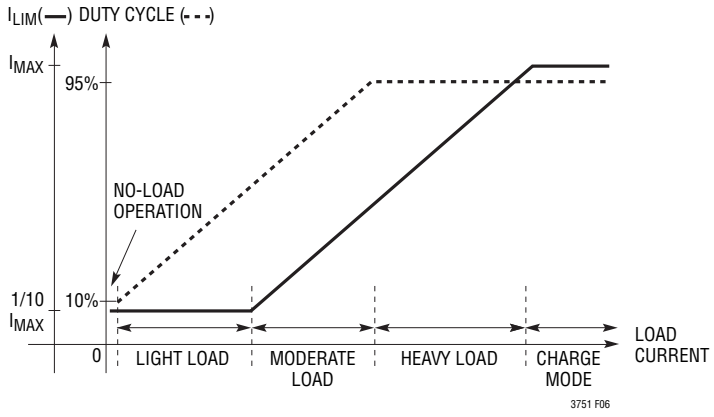


Figure 6. Regulation Technique

OPERATION

Periodic Refresh

When the LT3751 enters regulation, the internal circuitry deactivates switching when the internal one-shot clock is high. The clock operates at a 1/20th duty cycle with a minimum blank time of 1.5µs. This reset pulse is timed to drastically reduce switching frequency content within the audio spectrum and is active during all loading conditions. Each reset pulse guarantees at least one energy cycle. A minimum load is required to prevent the LT3751 from entering no-load operation.

Heavy Load Operation

The LT3751 enters peak current mode control at higher output load conditions. The control loop maximizes the number of switch cycles between each reset pulse. Since the control scheme operates in boundary mode, the resonant boundary-mode period changes with varying peak primary current:

$$Period = I_{PK} \bullet L_{PRI} \bullet \left[\frac{1}{V_{TRANS}} + \frac{N}{V_{OUT}} \right]$$

and the power output is proportional to the peak primary current:

$$P_{OUT} = \frac{1/2 \bullet I_{PK}}{\left[\frac{1}{V_{TRANS}} + \frac{N}{V_{OUT}} \right]}$$

Noise becomes an issue at very low load currents. The LT3751 remedies this problem by setting the lower peak current limit to one tenth the maximum level and begins to employ duty-cycle control.

Light Load Operation

The LT3751 uses duty cycle control to drastically reduce audible noise in both the transformer (mechanical) and the ceramic capacitors (piezoelectric effects). Internal control circuitry forces a one-shot condition at a periodic rate greater than 20kHz and out of the audio spectrum. The regulation loop then determines the number of pulses that are required to maintain the correct output voltage. Figure 5 shows the use of duty-cycle control.

No-Load Operation

The LT3751 can remain in low noise regulation at very low loading conditions. Below a certain load current threshold (Light Load Operation), the output voltage would continue to increase and a runaway condition could occur. This is due to the periodic one-shot forced by the periodic refresh circuitry. By design, the LT3751 has built-in overvoltage protection associated with the FB pin.

When the FB pin voltage exceeds 1.34V (±20mV), the LT3751 enters no-load operation. No-load operation does not reset with the one-shot clock. Instead, the pulse train is completely load-dependent. These bursts are asynchronous and can contain long periods of inactivity. This allows regulation at a no-load condition but with the increase of audible noise and voltage ripple. Note that when operating with no-load, the output voltage will increase 10% above the nominal output voltage.

APPLICATIONS INFORMATION

The LT3751 charger controller can be optimized for either capacitor charging only or low noise regulation applications. Several equations are provided to aid in the design process.

Safety Warning

Large capacitors charged to high voltage can deliver a lethal amount of energy if handled improperly. It is particularly important to observe appropriate safety measures when designing the LT3751 into applications. First, create a discharge circuit that allows the designer to safely discharge the output capacitor. Second, adequately space high voltage nodes from adjacent traces to satisfy printed circuit board voltage breakdown requirements.

Selecting Operating Mode

Tie the FB pin to GND to operate the LT3751 as a capacitor charger. In this mode, the LT3751 charges the output at peak primary current in boundary mode operation. This constitutes maximum power delivery and yields the fastest charge times. Power delivery is halted once the output reaches the desired output voltage set by the RV_{OUT} and RBG pins.

Tie a resistor divider from the FB pin to V_{OUT} and GND to operate the LT3751 as a low noise voltage regulator (refer to Low Noise regulation section for proper design procedures). The LT3751 operates as a voltage regulator using both peak current and duty cycle modulation to vary output current during different loading conditions.

Selecting Component Parameters

Most designs start with the initial selection of V_{TRANS}, V_{OUT}, C_{OUT}, and either charge time, t_{CHARGE}, (capacitor charger) or $P_{OUT,MAX}$ (regulator). These design inputs are then used to select the transformer ratio, N, the peak primary current, I_{PK}, and the primary inductance, L_{PRI}. Figure 7 can be used as a rough guide for maximum power output for a given V_{TRANS} and I_{PK}.

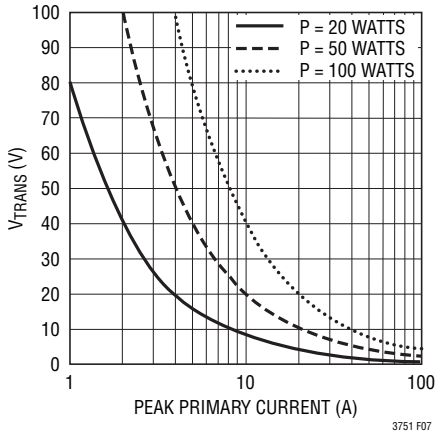


Figure 7. Maximum Power Output

Selecting Transformer Turns Ratio

The transformer ratio, N, should be selected based on the input and output voltages. Smaller N values equate to faster charge times and larger available output power. Note that drastically reducing N below the V_{OUT}/V_{TRANS} ratio will increase the flyback voltage on the drain of the NMOS and increase the current through the output diode. The ratio, N, should not be drastically increased either, due to the increased capacitance, $N^2 \bullet C_{SEC}$, reflected to the primary. A good choice is to select N equal to V_{OUT}/V_{TRANS}.

$$N \leq \frac{V_{OUT}}{V_{TRANS}}$$

Choosing Capacitor Charger I_{PK}

When operating the LT3751 as capacitor charger, choose I_{PK} based on the required capacitor charge time, t_{CHARGE}, and the initial design inputs.

$$I_{PK} = \frac{\left(2 \bullet N \bullet V_{TRANS} + V_{OUT}\right) \bullet C_{OUT} \bullet V_{OUT}}{\text{Efficiency} \bullet V_{TRANS} \bullet \left(t_{CHARGE} - t_d\right)}$$

The converter efficiency varies over the output voltage range. The I_{PK} equation is based on the average efficiency over the entire charging period. Several factors can cause the charge time to increase. Efficiency is the most dominant factor and is mainly affected by the transformer winding resistance, core losses, leakage inductance, and transistor R_{DS}. Most applications have overall efficiencies above 70%.

APPLICATIONS INFORMATION

The total propagation delay, t_d, is the second most dominant factor that affects efficiency and is the summation of gate driver on-off propagation delays and the discharge time associated with the secondary winding capacitance. There are two effective methods to reduce the total propagation delay. First, reduce the total capacitance on the secondary winding, most notably the diode capacitance. Second, reduce the total required NMOS gate charge. Figure 8 shows the effect of large secondary capacitance.

The energy stored in the secondary winding capacitance is $\frac{1}{2} \bullet C_{SEC} \bullet V_{OUT}^2$. This energy is reflected to the primary when the diode stops forward conduction. If the reflected capacitance is greater than the total NMOS drain capacitance, the drain of the NMOS power switch goes negative and its intrinsic body diode conducts. It takes some time for this energy to be dissipated and thus adds to the total propagation delay.

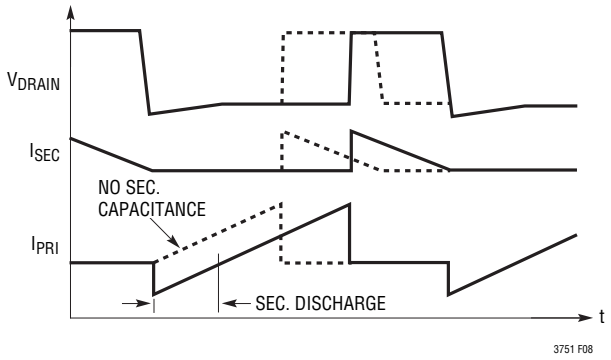


Figure 8. Effect of Secondary Winding Capacitance

Choosing Regulator Maximum I_{PK}

The I_{PK} parameter in regulation mode is calculated based on the desired maximum output power instead of charge time like that in a capacitor charger application.

$$I_{PK} = 2 \bullet \frac{P_{OUT(AVG)}}{Efficiency} \bullet \left(\frac{1}{V_{TRANS}} + \frac{N}{V_{OUT}} \right)$$

Note that the LT3751 regulation scheme varies the peak current based on the output load current. The maximum I_{PK} is only reached during charge mode or during heavy load conditions where output power is maximized.

Transformer Design

The transformer's primary inductance, L_{PRI}, is determined by the desired V_{OUT} and previously calculated N and I_{PK} parameters. Use the following equation to select L_{PRI}:

$$L_{PRI} = \frac{3\mu s \bullet V_{OUT}}{I_{PK} \bullet N}$$

The previous equation guarantees that the V_{OUT} comparator has enough time to sense the flyback waveform and trip the $\overline{DONE}$ pin latch. Operating V_{OUT} significantly higher than that used to calculate L_{PRI} could result in a runaway condition and overcharge the output capacitor.

The L_{PRI} equation is adequate for most regulator applications. Note that if both I_{PK} and N are increased significantly for a given V_{TRANS} and V_{OUT}, the maximum I_{PK} will not be reached within the refresh clock period. This will result in a lower than expected maximum output power. To prevent this from occurring, maintain the condition in the following equation.

$$L_{PRI} < \frac{38\mu s}{I_{PK} \bullet \left[\frac{1}{V_{TRANS}} + \frac{N}{V_{OUT}} \right]}$$

The upper constraint on L_{PRI} can be reduced by increasing V_{TRANS} and starting the design process over. The best regulation occurs when operating the boundary-mode frequency above 100kHz (refer to Operation section for boundary-mode definition).

Figure 9 defines the maximum boundary-mode switching frequency when operating at a desired output power level and is normalized to L_{PRI}/P_{OUT} (μH/Watt). The relationship of output power, boundary-mode frequency, I_{PK}, and primary inductance can be used as a guide throughout the design process.

APPLICATIONS INFORMATION

Table 1. Recommended Transformers

MANUFACTURER	PART NUMBER	SIZE L × W × H (mm)	MAXIMUM I_{PRI} (A)	L_{PRI} (µH)	TURNS RATIO (PRI:SEC)
Coilcraft www.coilcraft.com	DA2033-AL DA2034-AL GA3459-BL GA3460-BL HA4060-AL HA3994-AL	17.4 × 24.1 × 10.2 20.6 × 30 × 11.3 32.65 × 26.75 × 14 32.65 × 26.75 × 14 34.29 × 26.75 × 14 34.29 × 28.75 × 14	5 10 20 50 2 5	10 10 5 2.5 300 7.5	1:10 1:10 1:10 1:10 1:3 2:1:3:3*
Würth Elektronik/Midcom www.we-online.com	750032051 750032052 750310349 750310355	28.7 × 22 × 11.4 28.7 × 22 × 11.4 36.5 × 42 × 23 36.5 × 42 × 23	5 10 20 50	10 10 5 2.5	1:10 1:10 1:10 1:10
Sumida www.sumida.com	C8117 C8119 PS07-299 PS07-300	23 × 18.6 × 10.8 32.2 × 27 × 14 32.5 × 26.5 × 13.5 32.5 × 26.5 × 13.5	5 10 20 50	10 10 5 2.5	1:10 1:10 1:10 1:10
TDK www.tdk.com	DCT15EFD-U44S003 DCT20EFD-U32S003 DCT25EFD-U27S005	22.5 × 16.5 × 8.5 30 × 22 × 12 27.5 × 33 × 15.5	5 10 20	10 10 5	1:10 1:10 1:10

*Transformer has three secondaries where the ratio is designated as PRI:SEC1:SEC2:SEC3

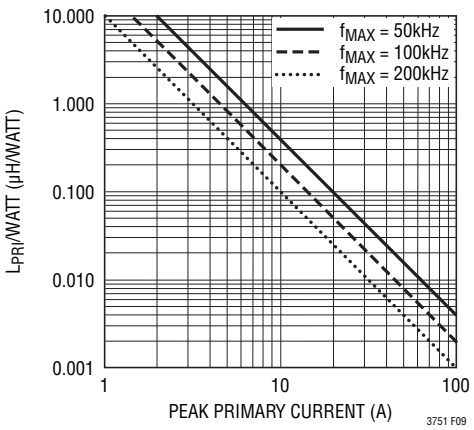


Figure 9. Maximum Switching Frequency

RV_{TRANS}, RV_{OUT} and R_{DCM} Selection

RV_{TRANS} sets the common-mode reference voltage for both the DCM comparator and V_{OUT} comparator. Select RV_{TRANS} from Table 2 based on the transformer supply voltage range, V_{TRANS}, and the maximum trip voltage, ΔV_{DRAIN} (V_{DRAIN}-V_{TRANS}).

The RV_{TRANS} pin is connected to an internal 40µA current source. Pin current increases as the pin voltage is taken higher than the internal 60V Zener clamp. The LT3751 can operate from V_{TRANS} greater than the 60V internal Zener clamps by limiting the RV_{TRANS} pin current to 250µA. Operating V_{TRANS} above 200V requires the use of resistor dividers. Two applications are presented that operate

Table 2. Suggested RV_{TRANS}, RV_{OUT}, and R_{DCM} Values

V_{TRANS} Range (V)	ΔV_{DRAIN} RANGE (V)	RV_{TRANS} (kΩ)	RV_{OUT} (kΩ)	R_{DCM} (kΩ)
4.75 to 55	0 to 5	5.11	5.11	2.32
4.75 to 60	2.5 to 50	25.5	25.5	11.5
	5 to 80	40.2	40.2	18.2
8 to 80	8 to 160	80.6	80.6	36.5
80 to 200	2mA • RV_{OUT}	$\frac{V_{TRANS}-55V}{0.25}$	$\frac{V_{TRANS}-55V}{0.25}$	0.86 • RV_{TRANS}
>200	Resistor Divider Dependent	Use Resistor Divider	Use Resistor Divider	Use Resistor Divider

APPLICATIONS INFORMATION

with V_{TRANS} between 100V and 400V (refer to Typical Applications section). Consult applications engineering for applications with V_{TRANS} operating above 400V.

RV_{OUT} is required for capacitor charger applications but may be removed for regulator applications. Note that the V_{OUT} comparator can be used as secondary protection for regulator applications. If the V_{OUT} comparator is used for protection, design $V_{OUT,TRIP}$ 15% to 20% higher than the regulation voltage. Tie the RV_{OUT} pin to ground when RV_{OUT} resistor is removed.

R_{DCM} needs to be properly sized in relation to RV_{TRANS}. Improper selection of R_{DCM} can lead to undesired switching operation at low output voltages. Use Table 2 to size R_{DCM}.

Parasitic capacitance on RV_{TRANS}, RV_{OUT}, and R_{DCM} should be minimized. Capacitances on these nodes slow down the response times of the V_{OUT} and DCM comparators. Keep the distance between the resistor and pin short. It is recommended to remove all ground and power planes underneath these pins and their respective components (refer to the recommended board layout at the end of this section).

R_{BG} Selection

R_{BG} sets the trip current ($0.98/R_{BG}$) and is directly related to the selection of RV_{OUT}. The best accuracy is achieved with a trip current between 100µA and 2mA. Choosing RV_{OUT} from Table 2 meets this criterion. Use the following equation to size R_{BG} ($V_{TRANS} \leq 80V$):

$$R_{BG} = 0.98 \bullet N \bullet \left(\frac{RV_{OUT}}{V_{OUT,TRIP} + V_{DIODE}} \right)$$

Tie R_{BG} pin to ground when not using the V_{OUT} comparator. Consult applications engineering for calculating R_{BG} when operating V_{TRANS} above 80V.

NMOS Switch Selection

Choose an external NMOS power switch with minimal gate charge and on-resistance that satisfies current limit and voltage break-down requirements. The gate is nominally driven to V_{CC} – 2V during each charge cycle. Ensure that this does not exceed the maximum gate to source voltage rating of the NMOS but enhances the channel enough to minimize the on-resistance.

Similarly, the maximum drain-source voltage rating of the NMOS must exceed $V_{TRANS} + V_{OUT}/N$ or the magnitude of the leakage inductance spike, whichever is greater. The maximum instantaneous drain current rating must exceed selected current limit. Because the switching period decreases with output voltage, the average current though the NMOS is greatest when the output is nearly charged and is given by:

$$I_{AVG,M} = \frac{I_{PK} \bullet V_{OUT(PK)}}{2(V_{OUT(PK)} + N \bullet V_{TRANS})}$$

See Table 3 for recommended external NMOS transistors.

Table 3. Recommended NMOS Transistors

MANUFACTURER	PART NUMBER	I_D (A)	$V_{DS(MAX)}$ (V)	$R_{DS(ON)}$ (mΩ)	$Q_{G(TOT)}$ (nC)	PACKAGE
Fairchild Semiconductor www.fairchildsemi.com	FDS2582	4.1	150	66	11	SO-8
	FQB19N20L	21	200	140	27	D^2PAK
	FQP34N20L	31	200	75	55	TO-220
	FQD12N20L	12	200	280	16	DPAK
	FQB4N80	3.9	800	3600	19	D^2PAK
On Semiconductor www.onsemi.com	MTD6N15T4G	6	150	300	15	DPAK
	NTD12N10T4G	12	100	165	14	DPAK
	NTB30N20T4G	30	200	81	75	D^2PAK
	NTB52N10T4G	52	100	30	72	D^2PAK
Vishay www.vishay.com	Si7820DN	2.6	200	240	12.1	1212-8
	Si7818DN	3.4	150	135	20	1212-8
	SUP33N20-60P	33	200	60	53	TO-220

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Table 4. Recommended Output Diodes

MANUFACTURER	PART NUMBER	$I_{F(AV)}$ (A)	V_{RRM} (V)	T_{RR} (ns)	PACKAGE
Central Semiconductor www.centralsemi.com	CMR1U-10M CMSH2-60M CMSH5-40	1 2 5	1000 60 40	100	SMA SMA SMC
Fairchild Semiconductor www.fairchildsemi.com	ES3J ES1G ES1J	3 1 1	600 400 600	35 35 35	SMC SMA SMA
On Semiconductor www.onsemi.com	MURS360 MURA260 MURA160	3 2 1	600 600 600	75 75 75	SMC SMA SMA
Vishay www.vishay.com	USB260 US1G US1M GURB5H60	2 1 1 5	600 400 1000 600	30 50 75 30	SMB SMA SMA D^2PAK

Gate Driver Operation

The LT3751 gate driver has an internal, selectable 10.5V or 5.6V clamp with up to 2A current capability (using LVGATE). For 10.5V operation, tie CLAMP pin to ground, and for 5.6V operation, tie the CLAMP pin to the V_{CC} pin. Choose a clamp voltage that does not exceed the NMOS manufacturer's maximum V_{GS} ratings. The 5.6V clamp can also be used to reduce LT3751 power dissipation and increase efficiency when using logic-level FETs. The typical gate driver overshoot voltage is 0.5V above the clamp voltage.

The LT3751's gate driver also incorporates a PMOS pull-up device via the LVGATE pin. The PMOS pull-up driver should only be used for V_{CC} applications of 8V or below. Operating LVGATE with V_{CC} above 8V will cause permanent damage to the part. LVGATE is active when tied to HVGATE and allows rail-to-rail gate driver operation. This is especially useful for low V_{CC} applications, allowing better NMOS drive capability. It also provides the fastest rise times, given the larger 2A current capability verses 1.5A when using only HVGATE.

Output Diode Selection

The output diode(s) are selected based on the maximum repetitive reverse voltage (V_{RRM}) and the average forward current ($I_{F(AV)}$). The output diode's V_{RRM} should exceed $V_{OUT} + N \bullet V_{TRANS}$. The output diode's $I_{F(AV)}$ should exceed $I_{PK}/2N$, the average short-circuit current. The average diode current is also a function of the output voltage.

$$I_{AVG} = \frac{I_{PK} \bullet V_{TRANS}}{2 \bullet (V_{OUT} + N \bullet V_{TRANS})}$$

The highest average diode current occurs at low output voltages and decreases as the output voltage increases. Reverse recovery time, reverse bias leakage and junction capacitance should also be considered. All affect the overall charging efficiency. Excessive diode reverse recovery times can cause appreciable discharging of the output capacitor, thereby increasing charge time. Choose a diode with a reverse recovery time of less than 100ns. Diode leakage current under high reverse bias bleeds the output capacitor of charge and increases charge time. Choose a diode that has minimal reverse bias leakage current. Diode junction capacitance is reflected back to the primary, and energy is lost during the NMOS intrinsic diode conduction. Choose a diode with minimal junction capacitance. Table 4 recommends several output diodes for various output voltages that have adequate reverse recovery times.

Setting Current Limit

Placing a sense resistor from the positive sense pin, CSP, to the negative sense pin, CSN, sets the maximum peak switch current. The maximum current limit is nominally $106mV/R_{SENSE}$. The power rating of the current sense resistor must exceed:

$$P_{RSENSE} \geq \frac{I^2_{PK} \bullet R_{SENSE}}{3} \left(\frac{V_{OUT(PK)}}{V_{OUT(PK)} + N \bullet V_{TRANS}} \right)$$

Additionally, there is approximately a 180ns propagation delay from the time that peak current limit is

APPLICATIONS INFORMATION

detected to when the gate transitions to the low state. This delay increases the peak current limit by (V_{TRANS}) (180ns)/L_{PRI}.

Sense resistor inductance (L_{RSENSE}) is another source of current limit error. L_{RSENSE} creates an input offset voltage (V_{OS}) to the current comparator and causes the current comparator to trip early. V_{OS} can be calculated as:

$$V_{OS} = V_{TRANS} \bullet \left(\frac{L_{RSENSE}}{L_{PRIMARY}} \right)$$

The change in current limit becomes V_{OS}/R_{SENSE}. The error is more significant for applications using large di/dt ratios in the transformer primary. It is recommended to use very low inductance (< 2nH) sense resistors. Several resistors can be placed in parallel to help reduce the inductance.

Care should also be taken in placement of the sense lines. The negative return line, CSN, must be a dedicated trace to the low side resistor terminal. Haphazardly routing the CSN connection to the ground plane can cause inaccurate current limit and can also cause an undesirable discontinuous charging profile.

$\overline{DONE}$ and $\overline{FAULT}$ Pin Design

Both the $\overline{DONE}$ and $\overline{FAULT}$ pins require proper pull-up resistors or current sources. Limit pin current to 1mA into either of these pins. 100kΩ pull-up resistors are recommended for most applications. Both the $\overline{DONE}$ and $\overline{FAULT}$ pins are latched in the low output state. Resetting either latch requires the CHARGE pin to be toggled. A fault condition will also cause the $\overline{DONE}$ pin to go low. A third, non-latching condition occurs during startup when the CHARGE pin is driven high. During this start-up condition, both the $\overline{DONE}$ and $\overline{FAULT}$ pins will go low for several micro seconds. This indicates the internal rails are still ramping to their proper levels. External RC filters may be added to both indication pins to remove start-up indication. Time constants for the RC filter should be between 5µs to 20µs.

Under/Overvoltage Lockout

The LT3751 provides user-programmable under and overvoltage lockouts for both V_{CC} and V_{TRANS}. Use the equations in the Pin Functions section for proper selection of resistor values. When under/overvoltage lockout comparators are tripped, the master latch is disabled, power delivery is halted, and the $\overline{FAULT}$ pin goes low.

Adequate supply bulk capacitors should be used to reduce power supply voltage ripple that could cause false tripping during normal switching operation. Additional filtering may be required due to the high input impedance of the under/overvoltage lockout pins to prevent false tripping. Individual capacitors ranging from 100pF to 1nF may be placed between each of the UVLO1, UVLO2, OVLO1 and OVLO2 pins and ground. Disable the undervoltage lockouts by directly connecting the UVLO1 and UVLO2 pins to VCC. Disable the overvoltage lockouts by directly connecting the OVLO1 and OVLO2 pins to ground.

The LT3751 provides internal Zener clamping diodes to protect itself in shutdown when V_{TRANS} is operated above 55V. Supply voltages should only be applied to UVLO1, UVLO2, OVLO1 and OVLO2 with series resistance such that the Absolute Maximum pin currents are not exceeded. Pin current can be calculated using:

$$I_{PIN} = \frac{V_{APPLIED} - 55V}{R_{SERIES}}$$

Note that in shutdown, RV_{TRANS}, RV_{OUT}, R_{DCM}, UVLO1, UVLO2, OVLO1 and OVLO2 currents increase significantly when operating V_{TRANS} above the Zener clamp voltages and are inversely proportional to the external series pin resistances.

NMOS Snubber Design

The transformer leakage inductance causes a parasitic voltage spike on the drain of the power NMOS switch during the turn-off transition. Transformer leakage inductance effects become more apparent at high peak primary currents. The worst-case magnitude of the voltage spike is determined by the energy stored in the leakage inductance and the total capacitance on the V_{DRAIN} node.

$$V_{D,LEAK} = \sqrt{\frac{L_{LEAK} \bullet I^2_{PK}}{C_{VDRAIN}}}$$

Two problems can arise from large $V_{D,LEAK}$. First, the magnitude of the spike may require an NMOS with an

APPLICATIONS INFORMATION

unnecessarily high $V_{(BR)DSS}$ which equates to a larger $R_{DS(ON)}$. Secondly, the V_{DRAIN} node will ring—possibly below ground—causing false tripping of the DCM comparator or damage to the NMOS switch (see Figure 11). Both issues can be remedied using a snubber. If leakage inductance causes issues, it is recommended to use a RC snubber in parallel with the primary winding, as shown in Figure 10. Size C_{SNUB} and R_{SNUB} based on the desired leakage spike voltage, known leakage inductance, and an RC time constant less than 1µs. Otherwise, the leakage voltage spike can cause false tripping of the V_{OUT} comparator and stop charging prematurely.

Figure 11 shows the effect of the RC snubber resulting in a lower voltage spike and faster settling time.

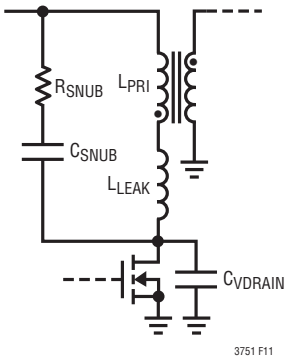

Figure 10. RC Snubber Circuit

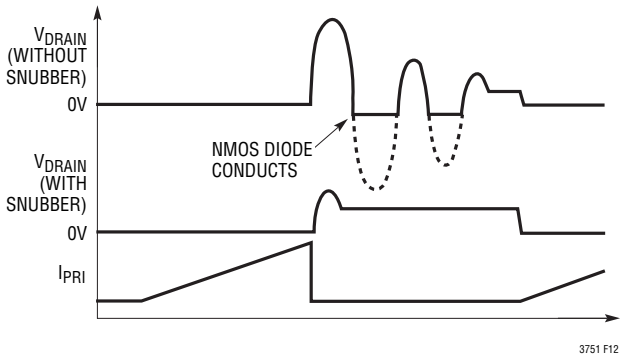

Figure 11. Effects of RC Snubber

LOW NOISE REGULATION

The LT3751 has the option to provide a low noise regulated output voltage when using a resistive voltage divider from the output node to the FB pin. Refer to the Selecting Component Parameters section to design the transformer, NMOS power switch, output diode, and sense resistor. Use the following equations to select the feedback resistor values based on the power dissipation and desired output voltage:

$$R_{FBH} = \frac{(V_{OUT} - 1.22)^2}{P_D} \text{ ; Top Feedback Resistor}$$

$$R_{FBL} = \left(\frac{1.22}{V_{OUT} - 1.22}\right) \bullet R_{FBH} \text{ ; Bottom Feedback Resistor}$$

R_{FBH}, depending on output voltage and type used, may require several smaller values placed in series. This will reduce the risk of arcing and damage to the feedback resistors. Consult the manufacturer's rated voltage specification for safe operation of the feedback resistors.

The LT3751 has a minimum periodic refresh frequency limit of 23kHz. This drastically reduces switching frequency components in the audio spectrum. The LT3751 can operate with no-load, but the regulation scheme switches to no-load operation and audible noise and output voltage ripple increase. This can be avoided by operating with a minimum load current.

Minimum Load Current

Periodic refresh circuitry requires an average minimum load current to avoid entering no-load operation. Usually, the feedback resistors should be adequate to provide this minimum load current.

$$I_{LOAD(MIN)} \geq \frac{L_{PRI} \bullet I^2_{PK} \bullet 23kHz}{100 \bullet V_{OUT}}$$

I_{PK} is the peak primary current at maximum power delivery. The LT3751 will enter no-load operation if the minimum load current is not met. No-load operation will prevent the application from entering a runaway condition; however, the output voltage will increase 10% over the nominal regulated voltage.

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Large Signal Stability

Large signal stability can be an issue when audible noise is a concern. Figure 12 shows that the problem originates from the one-shot clock and the output voltage ripple. The load must be constrained such that the output voltage ripple does not exceed the regulation range of the error amplifier within one clock period (approximately 6mV referred to the FB pin).

The output capacitance should be increased if oscillations occur or audible noise is present. Use Figure 13 to determine the maximum load for a given output capacitance to maintain low audible noise operation. A small capacitor can also be added from the FB pin to ground to lower the ripple injected into FB pin.

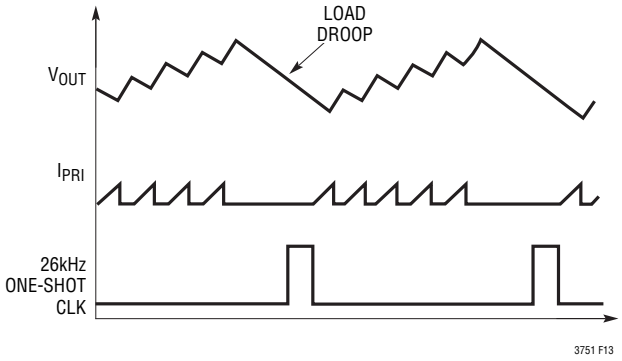


Figure 12. Voltage Ripple Stability Constraint

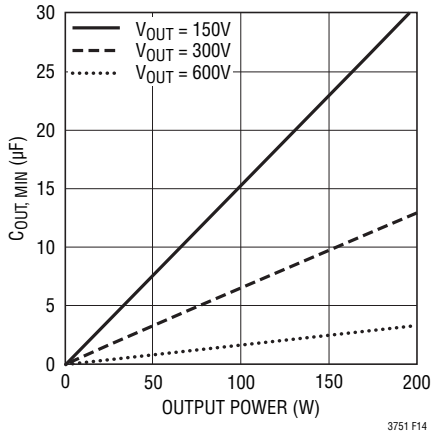


Figure 13. $C_{OUT(MIN)}$ vs Output Power

Small Signal Stability

The LT3751's error amplifier is internally compensated to increase its operating range but requires the converter's output node to be the dominant pole. Small signal stability constraints become more prevalent during heavy loading conditions where the dominant output pole moves to higher frequency and closer to the internal feedback poles and zeros. The feedback loop requires the output pole frequency to remain below 200Hz to guarantee small signal stability. This allows smaller R_{LOAD} values than the large signal constraint. Thus, small signal issues should not arise if the large signal constraint is met.

Board Layout

The high voltage operation of the LT3751 demands careful attention to the board layout, observing the following points:

1. Minimize the area of the high voltage end of the secondary winding.
2. Provide sufficient spacing for all high voltage nodes (NMOS drain, V_{OUT} and secondary winding of the transformer) in order to meet the breakdown voltage requirements.
3. Keep the electrical path formed by C_{VTRANS}, the primary of T1, and the drain of the NMOS as short as possible. Increasing the length of this path effectively increases the leakage inductance of T1, potentially resulting in an overvoltage condition on the drain of the NMOS.
4. Reduce the total node capacitance on the RV_{OUT} and R_{DCM} pins by removing any ground or power planes underneath the R_{DCM} and R_{VOUT} pads and traces. Parasitic capacitance can cause unwanted behavior on these pins.
5. Thermal vias should be added underneath the Exposed Pad, Pin 21, to enhance the LT3751's thermal performance. These vias should go directly to a large area of ground plane.
6. Isolated applications require galvanic separation of the output-side ground and primary-side ground. Adequate spacing between both ground planes is needed to meet voltage safety requirements.

APPLICATIONS INFORMATION

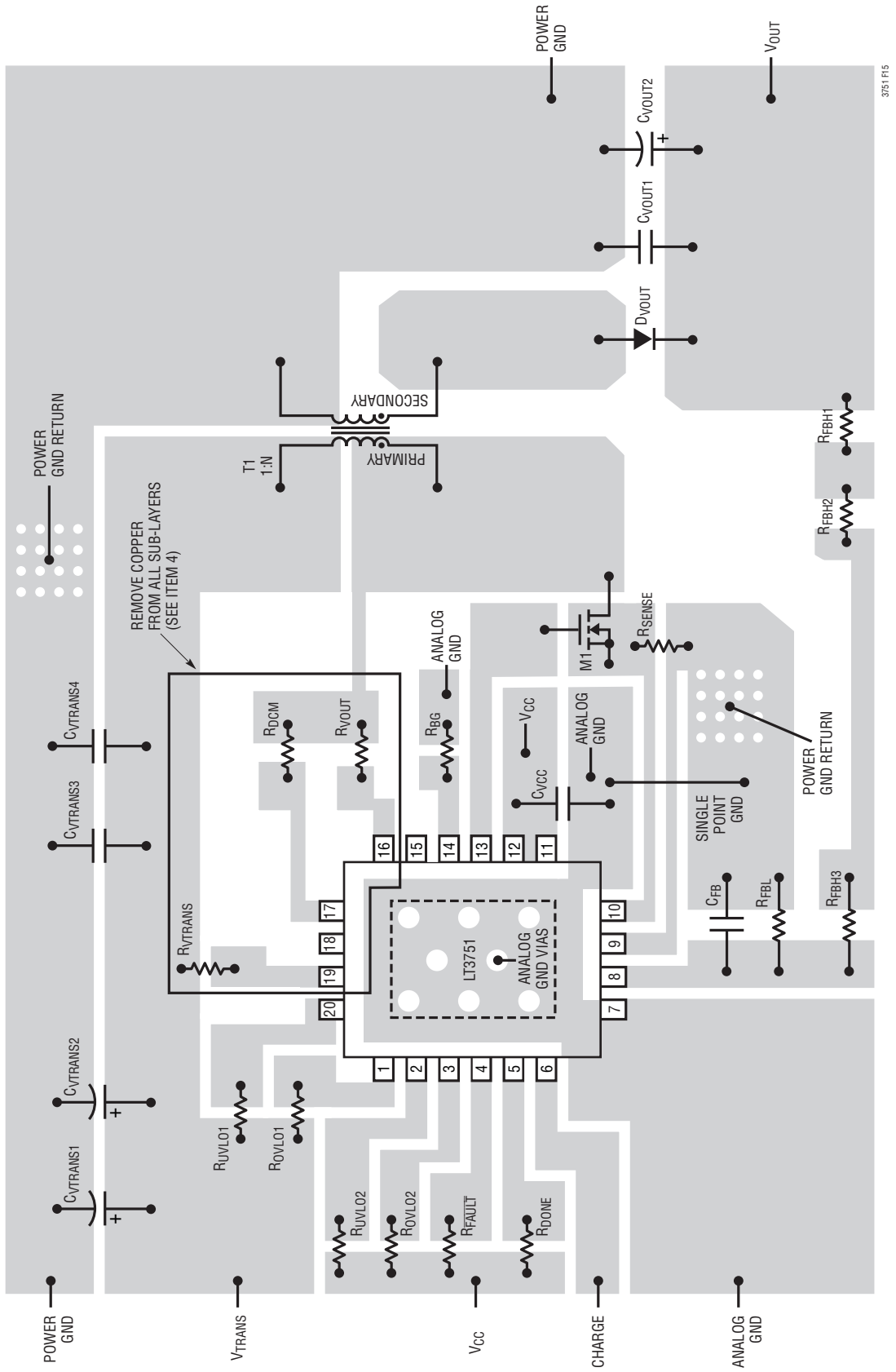


Figure 14. QFN Package Recommended Board Layout (Not to Scale)

APPLICATIONS INFORMATION

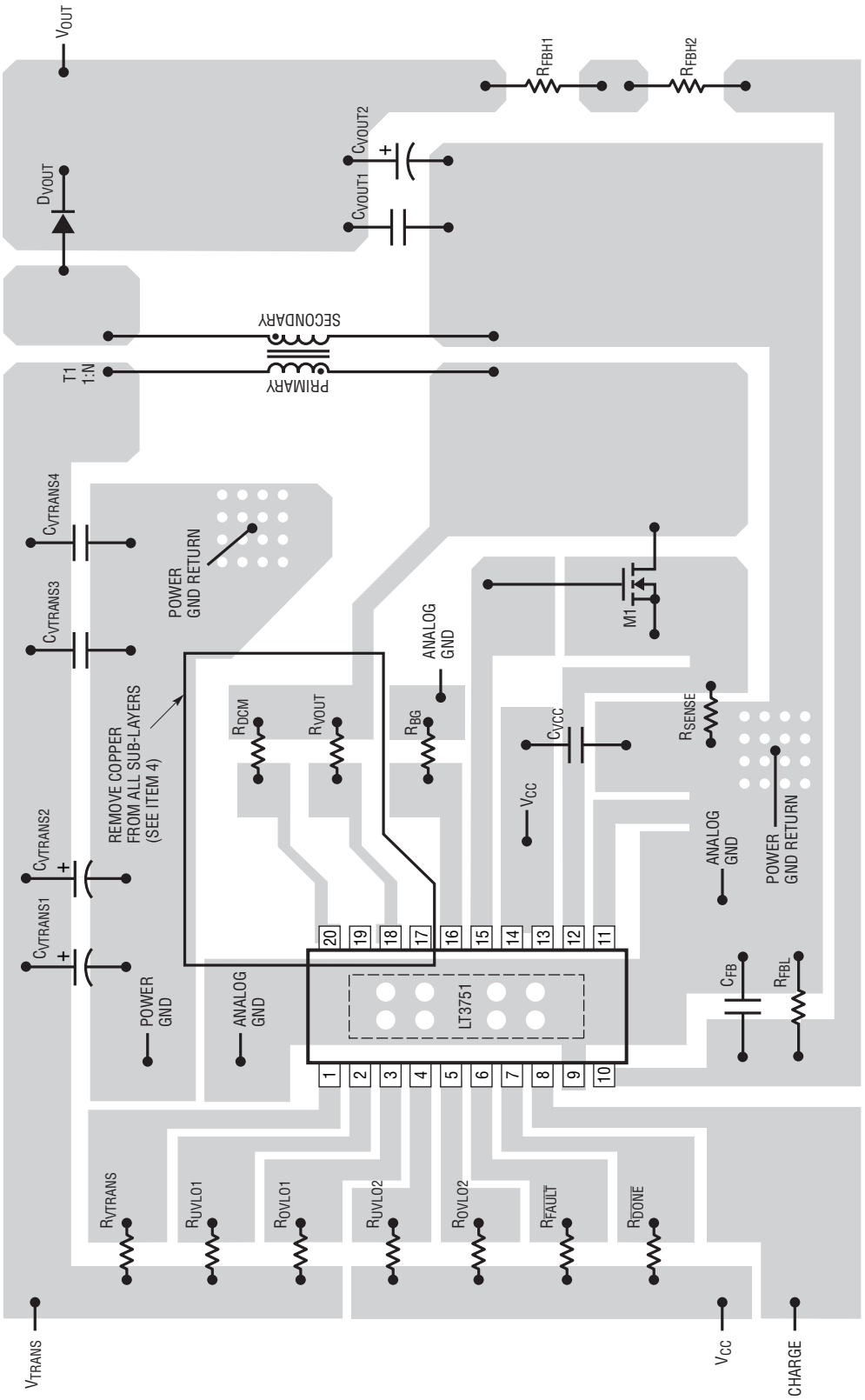
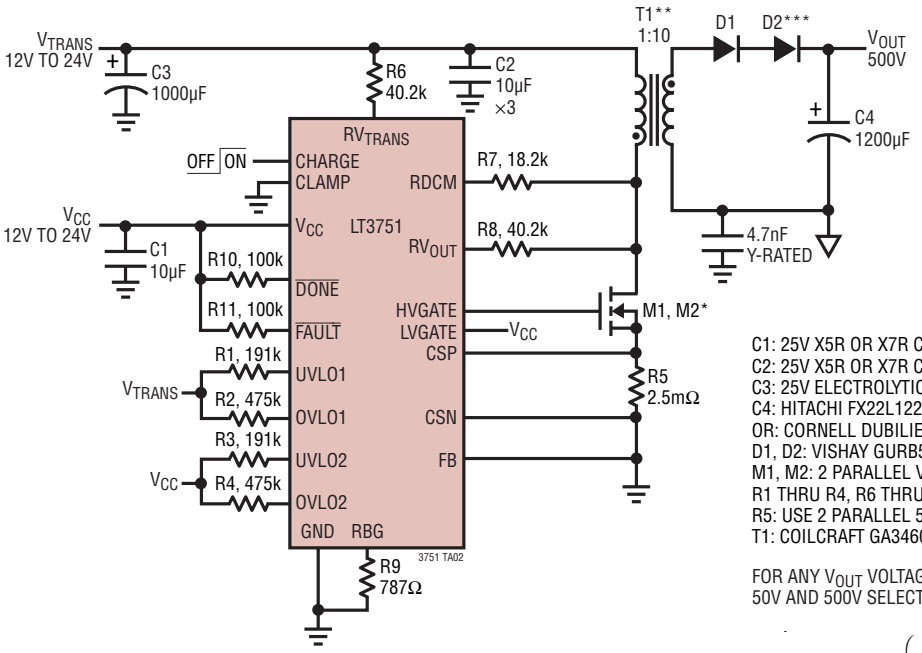


Figure 15. TSSOP Package Recommended Board Layout (Not to Scale)

TYPICAL APPLICATIONS

42A Capacitor Charger

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



* M1, M2 REQUIRES PROPER HEATSINK/THERMAL DISSIPATION TO MEET MANUFACTURER'S SPECIFICATIONS

** THERMAL DISSIPATION OF T1 WILL LIMIT THE CHARGE/DISCHARGE DUTY CYCLE OF C4

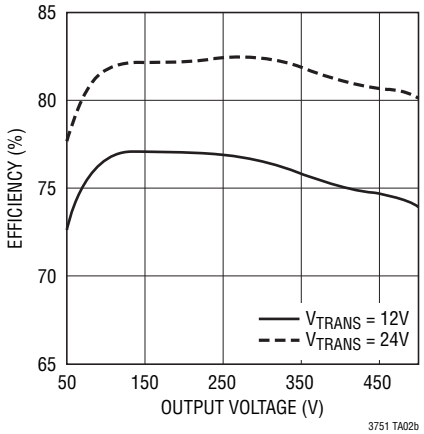
*** D2 MAY BE OMITTED FOR OUTPUT VOLTAGE OPERATION BELOW 300V

C1: 25V X5R OR X7R CERAMIC CAPACITOR
C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V ELECTROLYTIC
C4: HITACHI FX22L122Y 1200µF, 550V ELECTROLYTIC
OR: CORNELL DUBILIER DCMC192T550CE2B 1900µF, 550V ELECTROLYTIC
D1, D2: VISHAY GURB5H60 600V, 5A ULTRAFAST RECTIFIER
M1, M2: 2 PARALLEL VISHAY SUP33N20-60P 200V, 33A NMOS
R1 THRU R4, R6 THRU R11: USE 1% 0805 RESISTORS
R5: USE 2 PARALLEL 5mΩ IRC LR SERIES 2512 RESISTORS
T1: COILCRAFT GA3460-BL 50A SURACE MOUNT TRANSFORMER

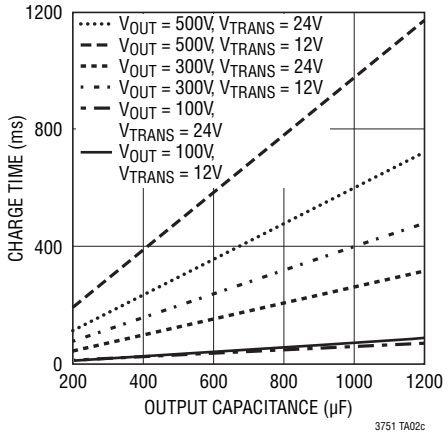
FOR ANY V_{OUT} VOLTAGE BETWEEN 50V AND 500V SELECT R9 ACCORDING TO:

$$R9 = 0.98 \bullet N \bullet \left(\frac{40.2k\Omega}{V_{OUT} + V_{DIODE}} \right)$$

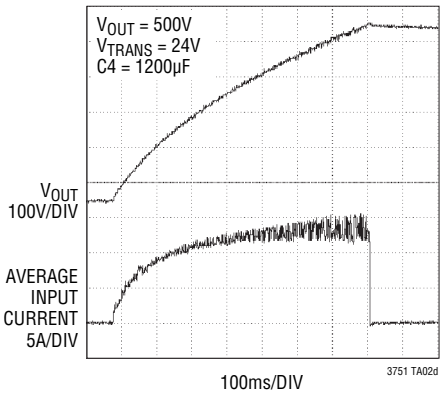
Efficiency



Output Capacitor Charge Times



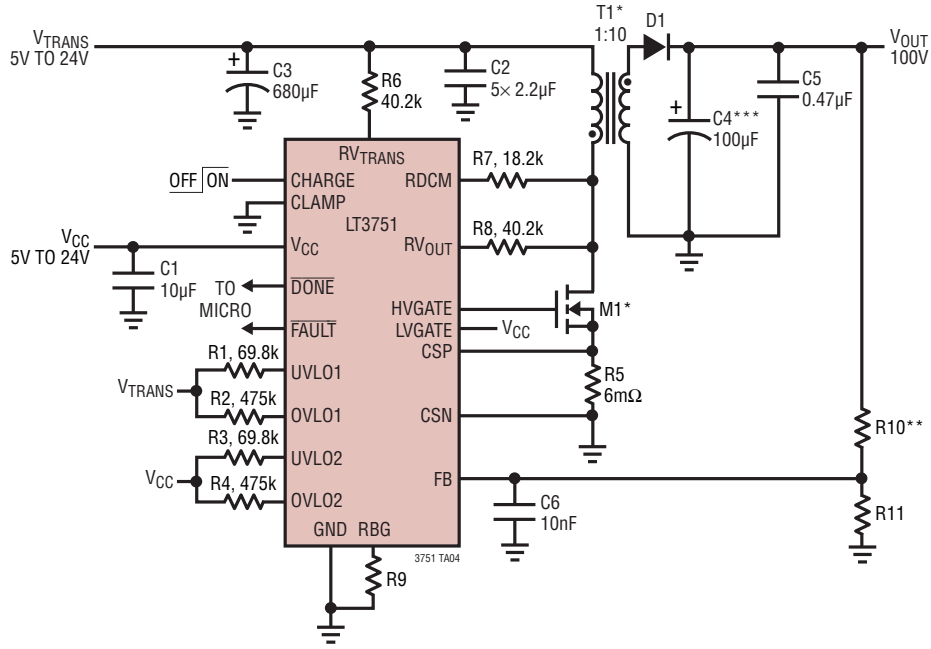
Charging Waveform



TYPICAL APPLICATIONS

High Voltage Regulator

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



* M1 AND T1 REQUIRE PROPER HEATSINK/THERMAL DISSIPATION TO MEET MANUFACTURER'S SPECIFICATIONS

** DEPENDING ON DESIRED OUTPUT VOLTAGES, R10 MUST BE SPLIT INTO MULTIPLE RESISTORS, TO MEET MANUFACTURER'S VOLTAGE SPECIFICATION.

*** C4 MUST BE SIZED TO MEET LARGE SIGNAL STABILITY CRITERIA DESCRIBED IN THE APPLICATIONS INFORMATION SECTION

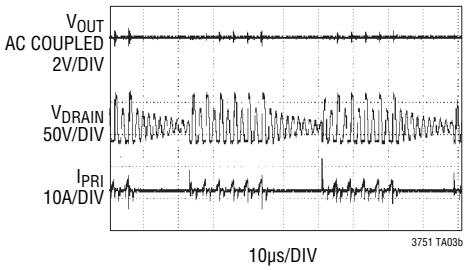
C1: 25V X5R OR X7R CERAMIC
C2: 25V X5R OR X7R CERAMIC
C3: 25V ELECTROLYTIC
C5: TDK CKG57NX7R2J474M
D1: VISHAY US1M 1000V
M1: FAIRCHILD FQP34N20L
R1 THRU R4, R6 THRU R9, R11: USE 1% 0805
R5: IRC LR SERIES 2512 RESISTORS
R10: USE 200V 1206 RESISTOR(S)
T1: COILCRAFT GA3459-AL

Suggested Component Values

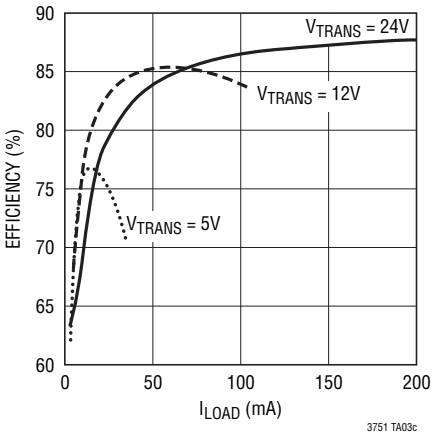
V_{OUT} (V)	$I_{OUT(MAX)}$ (mA) AT V_{TRANS} = 5V, 5% V_{OUT} DEFLECTION	$I_{OUT(MAX)}$ (mA) AT V_{TRANS} = 24V, 5% V_{OUT} DEFLECTION	R9 (kΩ)	R11 (kΩ)	R10 (kΩ)
100	180	270	3.32	0.383	30.9
200	110	315	1.65	0.768	124
300	75	245	1.10	1.13	274
400	55	200	0.825	1.54	499
500†	40	170	Tie to GND	1.74	715

†Transformer primary inductance limits V_{OUT} comparator operation to V_{OUT} = 400V_{MAX}. RV_{OUT} and R_{BG} should be tied to ground when operating V_{OUT} above 400V.

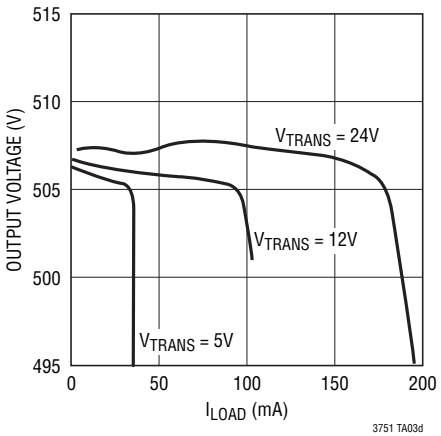
Steady-State Operation with 1.1mA Load Current



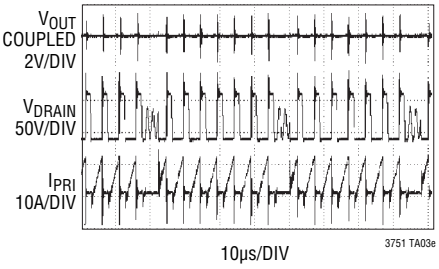
Efficiency (V_{OUT} = 500V)



Load Regulation (V_{OUT} = 500V)



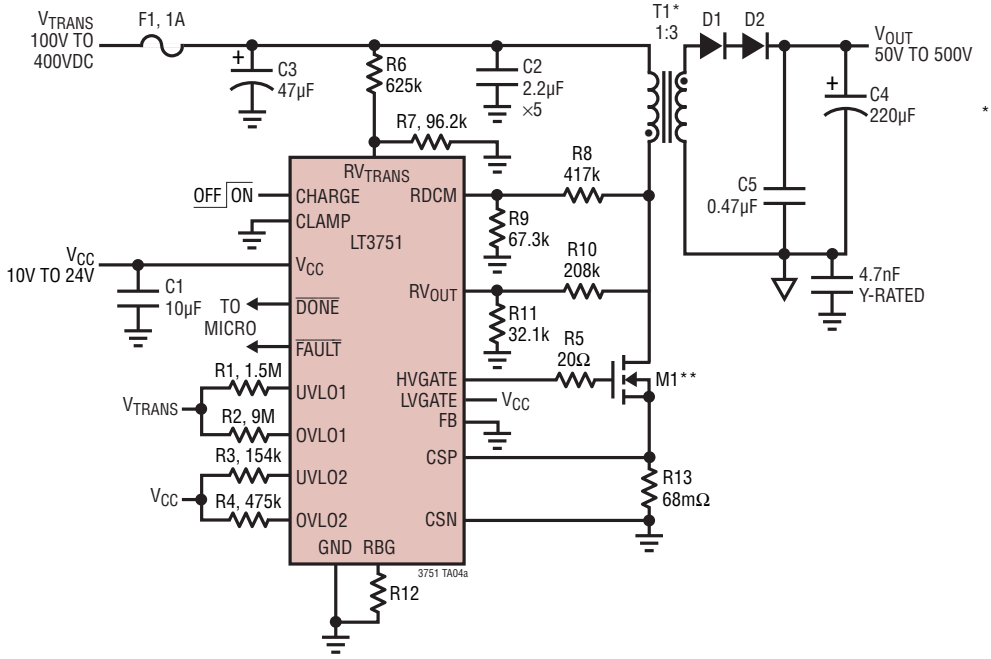
Steady-State Operation with 100mA Load Current



TYPICAL APPLICATIONS

1.6A High Input Voltage, Isolated Capacitor Charger

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



* T1 REQUIRES PROPER THERMAL MANAGEMENT TO ACHIEVE DESIRED OUTPUT POWER LEVELS

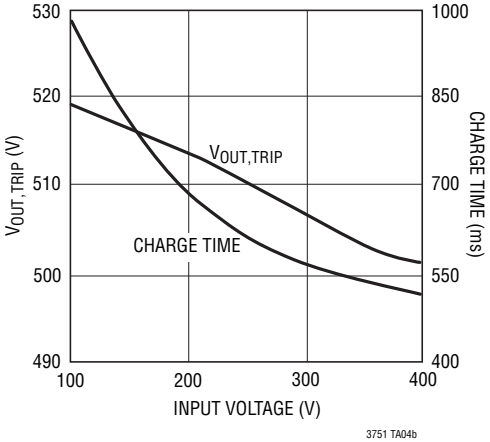
** M1 REQUIRES PROPER HEAT SINK/THERMAL DISSIPATION TO MEET MANUFACTURER'S SPECIFICATIONS

FOR ANY OUTPUT VOLTAGE BETWEEN 50V TO 500V, SET R12 GIVEN BY:

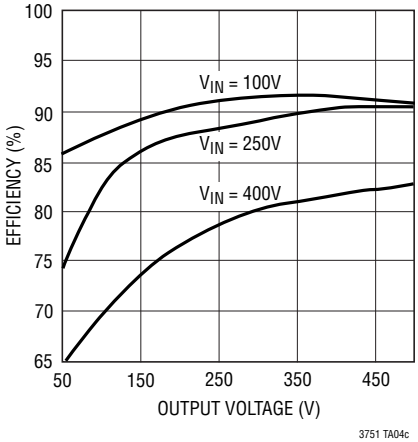
$$R12 = \frac{0.98}{\frac{V_{OUT,TRIP}}{3 \bullet R10} + 40\mu A \bullet 2}$$

C1: 25V X5R OR X7R CERAMIC
C2: 630V X5R OR X7R CERAMIC
C3: 450V ILLINOIS CAP 476CKE450MQW
C4: 50V TO 500V ELECTROLYTIC
C5: TDK CKG57NX7R2J474M
D1, D2: VISHAY US1M 1000V
F1: BUSSMANN PCB-1-R
M1: FAIRCHILD FQB4N80
R1, R2: 2 X 1206 RESISTORS IN SERIES, 1%
R3 THRU R5, R9, R12: 0805 RESISTORS, 1%
R6, R10: 3 X 1206 RESISTORS IN SERIES, 0.1%
R7, R11: 0805 RESISTORS, 0.1%
R8: 3 X 1206 RESISTORS IN SERIES, 1%
R13: IRC LR SERIES 1206 RESISTOR, 1%
T1: COILCRAFT HA4060-AL

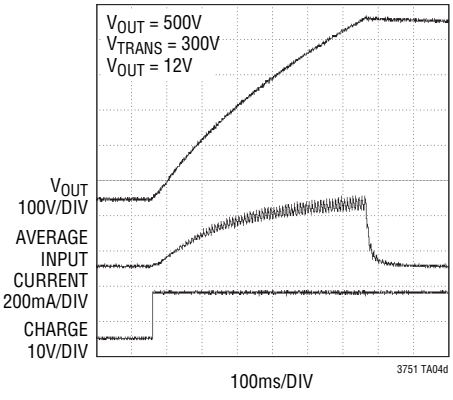
Output Trip Voltage and Charge Time (V_{OUT} = 500V, C_{OUT} = 220µF)



Efficiency



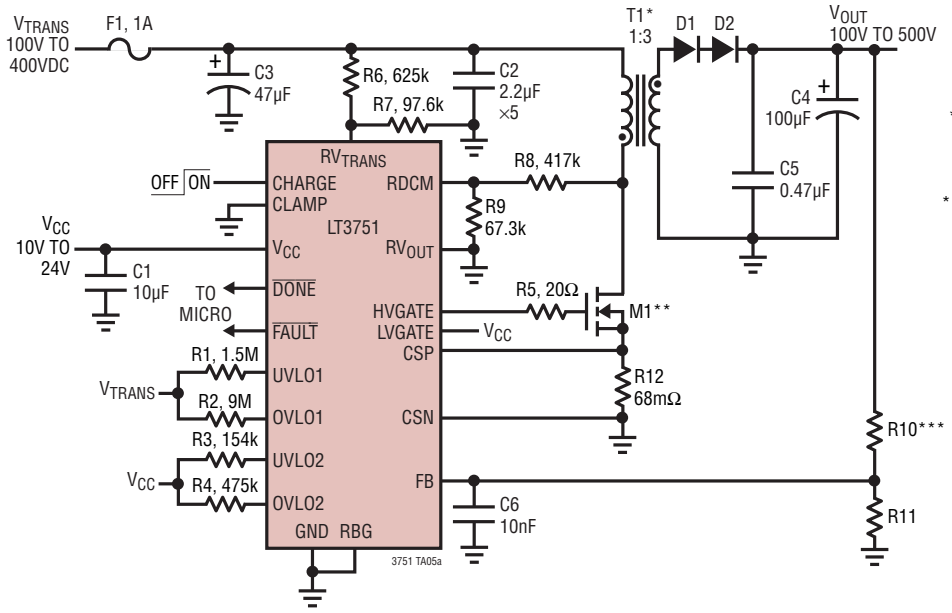
Charging Waveform



TYPICAL APPLICATIONS

High Input Voltage, High Output Voltage Regulator

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



* T1 REQUIRES PROPER THERMAL MANAGEMENT TO ACHIEVE DESIRED OUTPUT POWER LEVELS

** M1 REQUIRES PROPER HEAT SINK/THERMAL DISSIPATION TO MEET MANUFACTURER'S SPECIFICATIONS

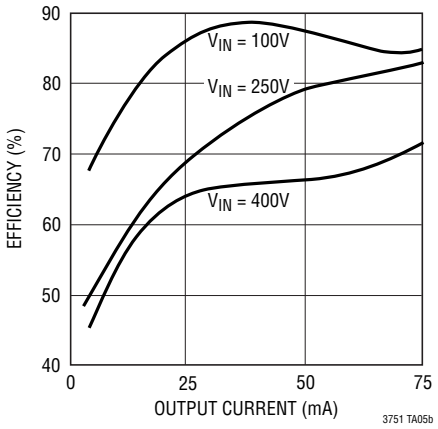
*** DEPENDING ON DESIRED OUTPUT VOLTAGE, R10 MUST BE SPLIT INTO MULTIPLE RESISTORS TO MEET MANUFACTURER'S VOLTAGE SPECIFICATION

C1: 25V X5R OR X7R CERAMIC
C2: 630V X5R OR X7R CERAMIC
C3: 450V ILLINOIS CAP 476CKE450MQW
C4: 50V TO 500V ELECTROLYTIC
C5: TDK CKG57NX7R2J474M
C6: 6.3V X5R OR X7R CERAMIC
D1, D2: VISHAY US1M 1000V
F1: BUSSMANN PCB-1-R
M1: FAIRCHILD FQB4N80
R1, R2: 2 X 1206 RESISTORS IN SERIES, 1%
R3 THRU R5, R7, R9, R11: 0805 RESISTORS, 1%
R6, R8: 3 X 1206 RESISTORS IN SERIES, 1%
R10: 1206 RESISTOR(S), 1%
R12: IRC LR SERIES 1206 RESISTOR, 1%
T1: COILCRAFT HA4060-AL

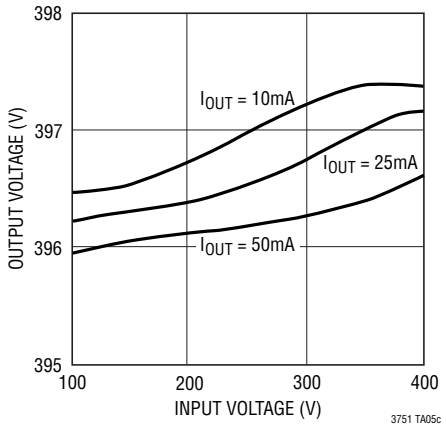
Suggested Component Values

V_{OUT} (V)	$I_{OUT(MAX)}$ (mA) AT V_{TRANS} = 100V, 1% V_{OUT} DEFLECTION	$I_{OUT(MAX)}$ (mA) AT V_{TRANS} = 400V, 1% V_{OUT} DEFLECTION	R10 (kΩ)	R11 (kΩ)
100	55	130	30.9	0.383
200	110	150	124	0.768
300	95	175	274	1.13
400	80	130	499	1.54
500	65	140	715	1.74

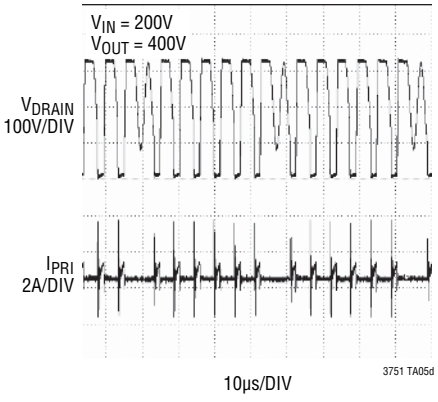
Efficiency



Line Regulation



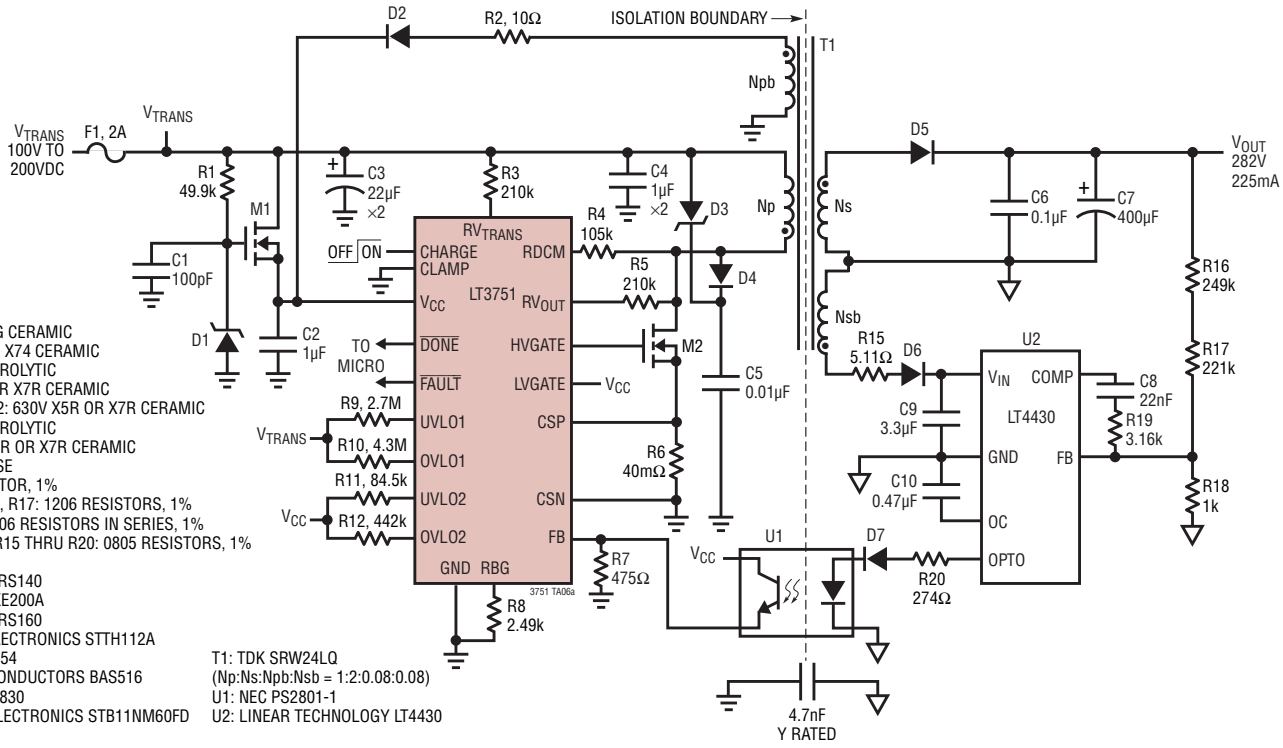
Steady-State Operation with 50mA Load Current



TYPICAL APPLICATIONS

Isolated 282V Voltage Regulator

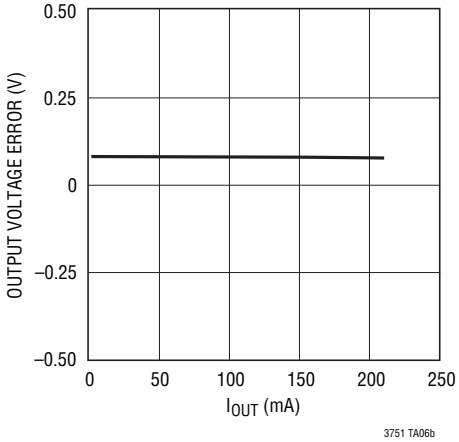
DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



C1, C8: 16V COG CERAMIC
C2: 16V X5R OR X74 CERAMIC
C3: 350V ELECTROLYTIC
C4: 250V X5R OR X7R CERAMIC
C5, C6, C11, C12: 630V X5R OR X7R CERAMIC
C7: 350V ELECTROLYTIC
C9, C10: 25V X5R OR X7R CERAMIC
F1: 250V, 2A FUSE
R1: 2010 RESISTOR, 1%
R2, R3, R6, R16, R17: 1206 RESISTORS, 1%
R4, R5: TWO 1206 RESISTORS IN SERIES, 1%
R7 THRU R12, R15 THRU R20: 0805 RESISTORS, 1%
D1: 12V ZENER
D2: VISHAY MURS140
D3: VISHAY P6KE200A
D4: VISHAY MURS160
D5: STMICROELECTRONICS STTH112A
D6: VISHAY BAT54
D7: NXP SEMICONDUCTORS BAS516
M1: VISHAY IRF830
M2: STMICROELECTRONICS STB11NM60FD

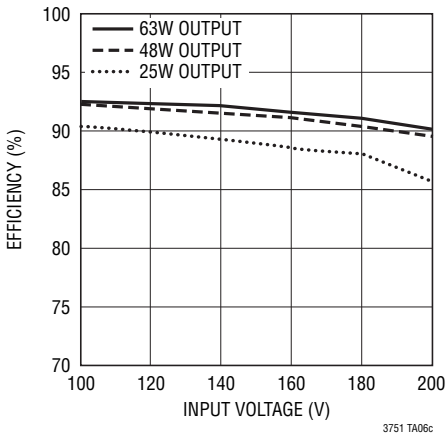
T1: TDK SRW24LQ
(Np:Ns:Npb:Nsb = 1:2:0.08:0.08)
U1: NEC PS2801-1
U2: LINEAR TECHNOLOGY LT4430

Load Regulation



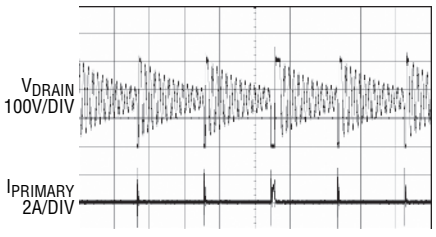
3751 TA06b

Efficiency



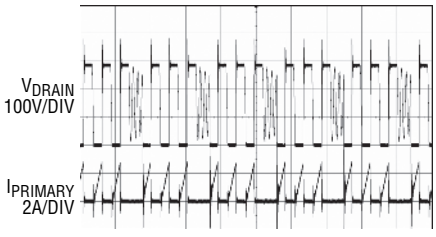
3751 TA06c

Steady-State Operation with 7.1mA Load Current



3751 TA06d

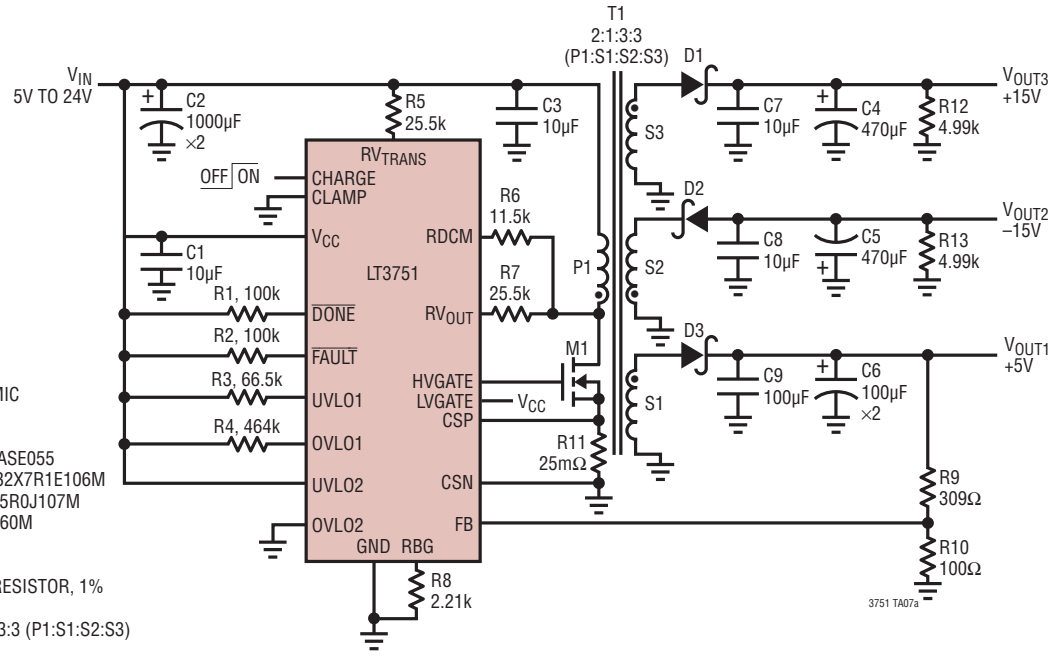
Steady-State Operation with 225mA Load Current



3751 TA06e

TYPICAL APPLICATIONS

Wide Input Voltage Range, 15 Watt, Triple Output Voltage Regulator



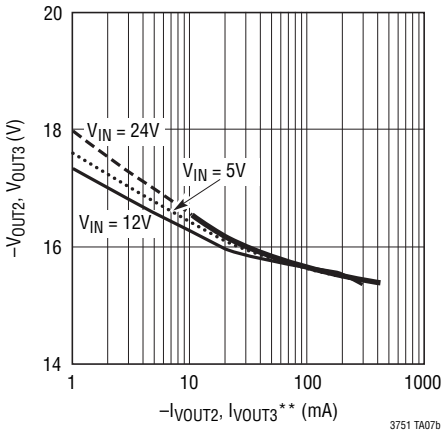
C1, C3: 25V X5R OR X7R CERAMIC
C2: 25V SANYO 25ME1000AX
C4, C5: 35V SANYO 35ME470AX
C6: 10V KEMET T520D107M010ASE055
C7, C8: 16V CERAMIC, TDK C4532X7R1E106M
C9: 6.3V CERAMIC, TDK C4532X5R0J107M
D1, D2: CENTRAL SEMI CMSH2-60M
D3: CENTRAL SEM1 CMSH5-40
M1: FAIRCHILD FQD12N20L
R1 THRU R10, R12, R13: 0805 RESISTOR, 1%
R11: 1206 RESISTOR, 1%
T1: COILCRAFT HA3994-AL, 2:1:3:3 (P1:S1:S2:S3)

Maximum Output Conditions

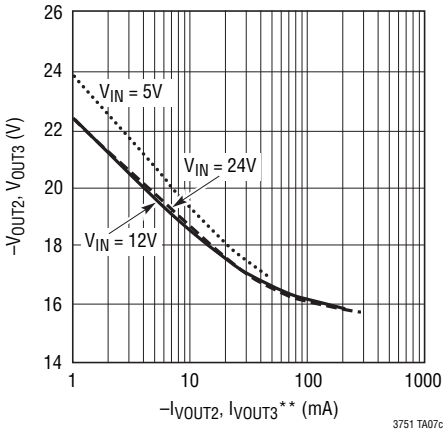
V_{CC} (V)	$P_{OUT(MAX)}$ (W)	$I_{OUT(MAX)}$* (mA)		
		V_{OUT1}	V_{OUT2}	V_{OUT3}
5	6.5	750	300	300
12	10	1750	300	300
24	13	2500	300	300

*All other output currents set to 0mA

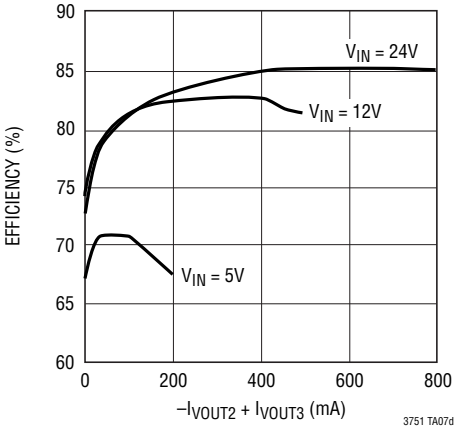
Cross Regulation (I_{VOUT1} = 100mA)



Cross Regulation (I_{VOUT1} = 500mA)



Efficiency (I_{VOUT1} = 500mA)

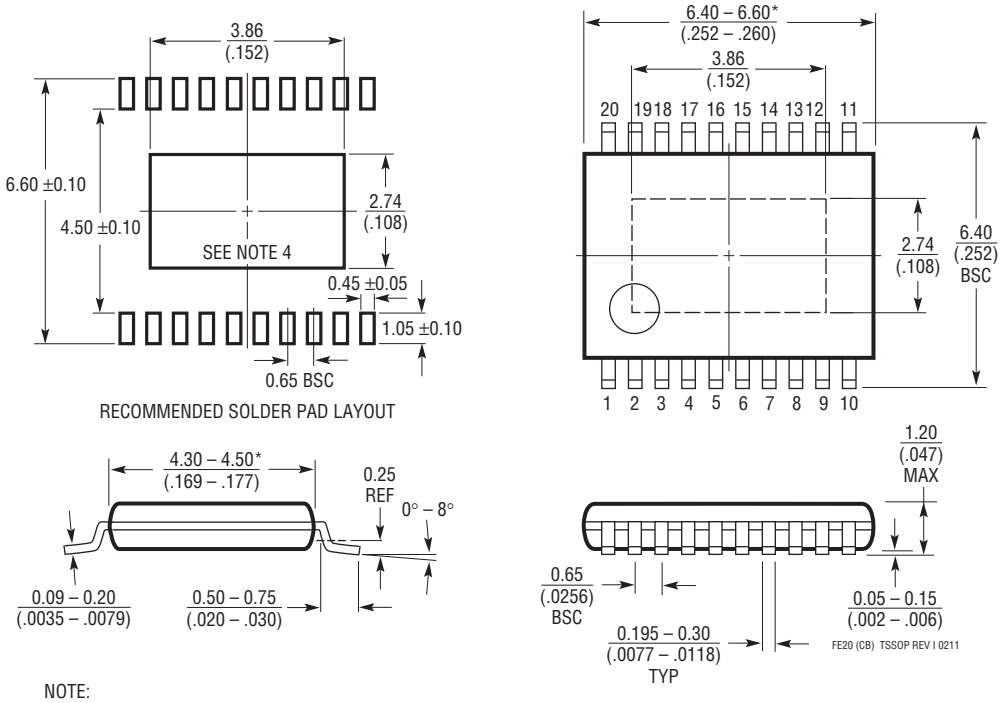


**SOURCE/SINK IDENTICAL CURRENTS FROM BOTH V_{OUT2} AND V_{OUT3}, RESPECTIVELY

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation CB

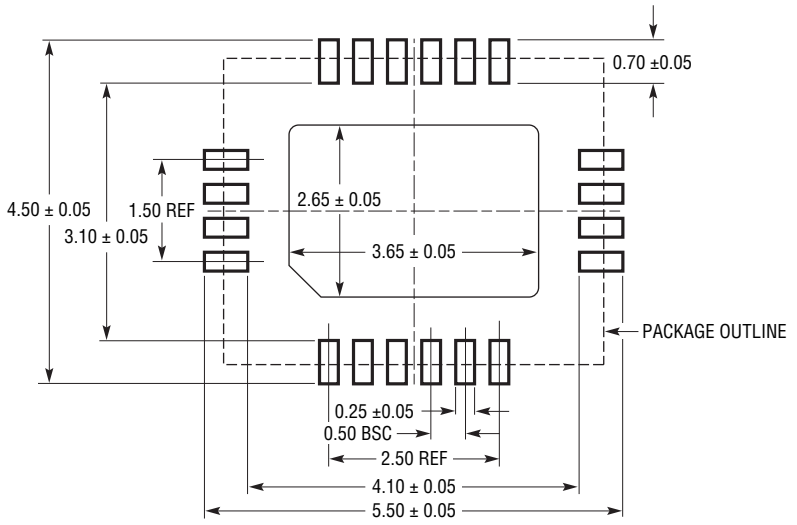


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

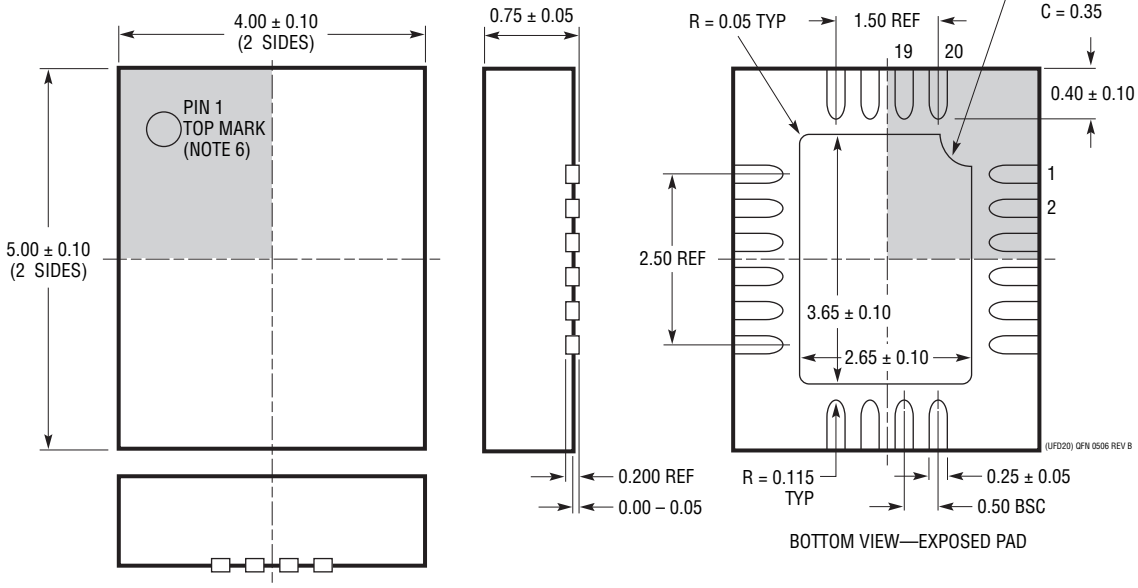
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
20-Pin Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

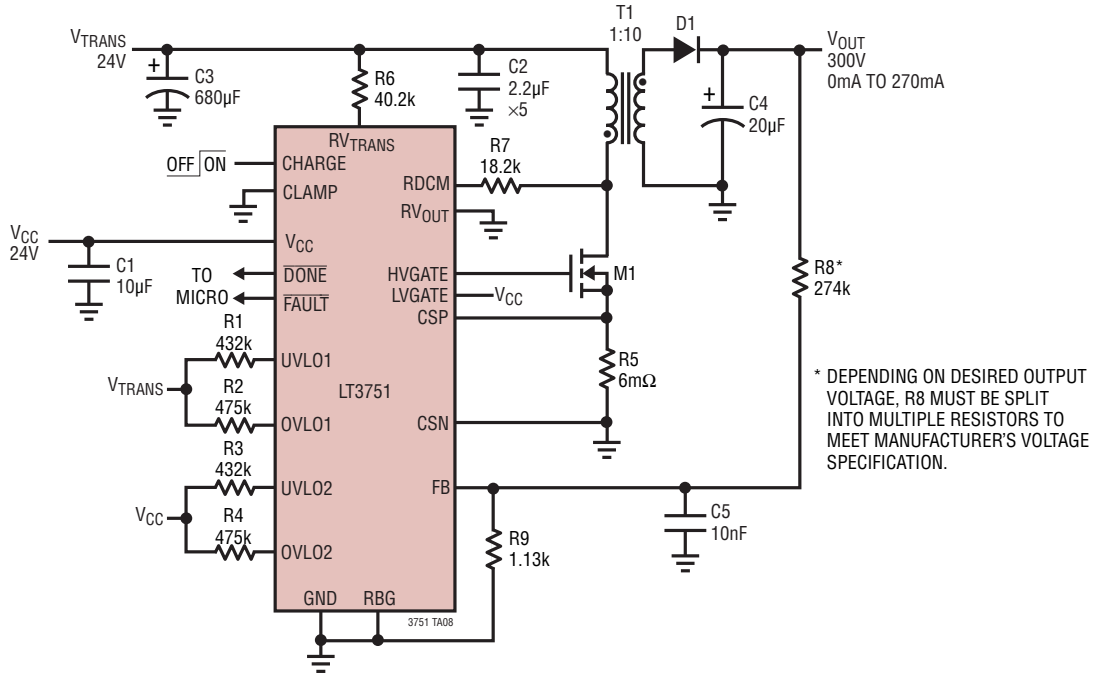
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/10	Updated FAULT (Pin 6/Pin 4) description in Pin Functions	7
		Updated DONE (Pin 7/Pin 5) description in Pin Functions	8
		Updated Block Diagram	9
		Revised Applications Information section	17, 18
		Revised Typical Applications illustration	30
C	6/12	Revised Applications Information section	20
		Corrected Schematic R8 value from 3.40k to 2.21k	30
		Updated FE package drawing	31

TYPICAL APPLICATION

300V Regulated Power Supply



C1: 25V X5R OR X7R CERAMIC CAPACITOR
C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V ELECTROLYTIC
C4: 330V RUBYCON PHOTOFLASH CAPACITOR
D1: VISHAY US1M 1000V

M1: FAIRCHILD FQP34N20L
R1 THROUGH R4: USE 1% 0805 RESISTORS
R5: IRC LR SERIES 2512 RESISTOR
T1: SUMIDA PS07-299, 20A TRANSFORMER

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3225	150mA Supercapacitor Charger	V_{IN}: 2.75V to 5.5V, Charges Two Supercapacitors in Series to 4.8V or 5.3V
LT3420/LT3420-1	1.4A/1A, Photoflash Capacitor Charger with Automatic Top-Off	Charges 220µF to 320V in 3.7 Seconds from 5V, V_{IN}: 2.2V to 16V, I_{SD} < 1µA, 10-Lead MS Package
LT3468/LT3468-1/ LT3468-2	1.4A, 1A, 0.7A, Photoflash Capacitor Charger	V_{IN}: 2.5V to 16V, Charge Time: 4.6 Seconds for LT3468 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, ThinSOT™ Package
LT3484-0/LT3484-1/ LT3484-2	1.4A, 0.7A, 1A Photoflash Capacitor Charger	V_{IN}: 1.8V to 16V, Charge Time: 4.6 Seconds for LT3484-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 2mm × 3mm 6-Lead DFN Package
LT3485-0/LT3485-1/ LT3485-2/LT3485-3	1.4A, 0.7A, 1A, 2A Photoflash Capacitor Charger with Output Voltage Monitor and Integrated IGBT	V_{IN}: 1.8V to 10V, Charge Time: 3.7 Seconds for LT3485-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 3mm × 3mm 10-Lead DFN Package
LT3585-0/LT3585-1/ LT3585-2/LT3585-3	1.2A, 0.55A, 0.85A, 1.7A Photoflash Capacitor Charger with Adjustable Input Current and IGBT Drivers	V_{IN}: 1.5V to 16V, Charge Time: 3.3 Seconds for LT3585-3 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 3mm × 2mm DFN-10 Package
LT3750	Capacitor Charger Controller	V_{IN}: 3V to 24V, Charge Time: 300ms for (0V to 300V, 100µF) MSOP-10 Package

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