



## PM6685

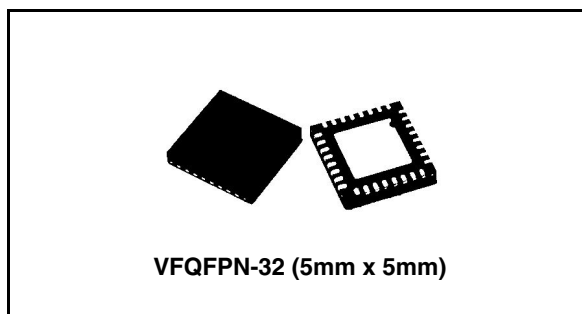
### Dual step-down main supply controller with auxiliary voltages for notebook system power

#### Features

- 6V to 28V input voltage range
- Fixed 5V - 3.3V output voltages
- 5V and 3.3V voltage always available to deliver 100mA of peak current
- 1.237V  $\pm 1\%$  reference voltage available
- No  $R_{SENSE}$  current sensing using low side MOSFETs  $R_{DS(on)}$
- Accurate current sense with  $R_{SENSE}$
- Negative current limit
- Soft-start internally fixed at 2ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33kHz) in pulse skip mode
- 4mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation

#### Applications

- Notebook computers
- Tablet PC or slates
- Mobile system power supply
- 3 and -4 Cells Li+ battery-powered devices



#### Description

PM6685 is a dual step-down controller specifically designed to provide extremely high efficiency conversion with loss-less current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation.

An embedded integrator control loop compensates the DC voltage error due to the output ripple. The pulse skipping technique increases efficiency for very light loads. Moreover, a minimum switching frequency of 33kHz is selectable in order to avoid audio noise issues.

The PM6685 provides a selectable switching frequency, allowing either 200kHz/300kHz, 300kHz/400kHz, or 400kHz/500kHz operation of the 5V/3.3V switching sections.

#### Order codes

Part number	Package	Packaging
PM6685	VFQFPN-32 (5mm x 5mm)	Tube
PM6685TR	VFQFPN-32 (5mm x 5mm)	Tape and Reel

# Contents

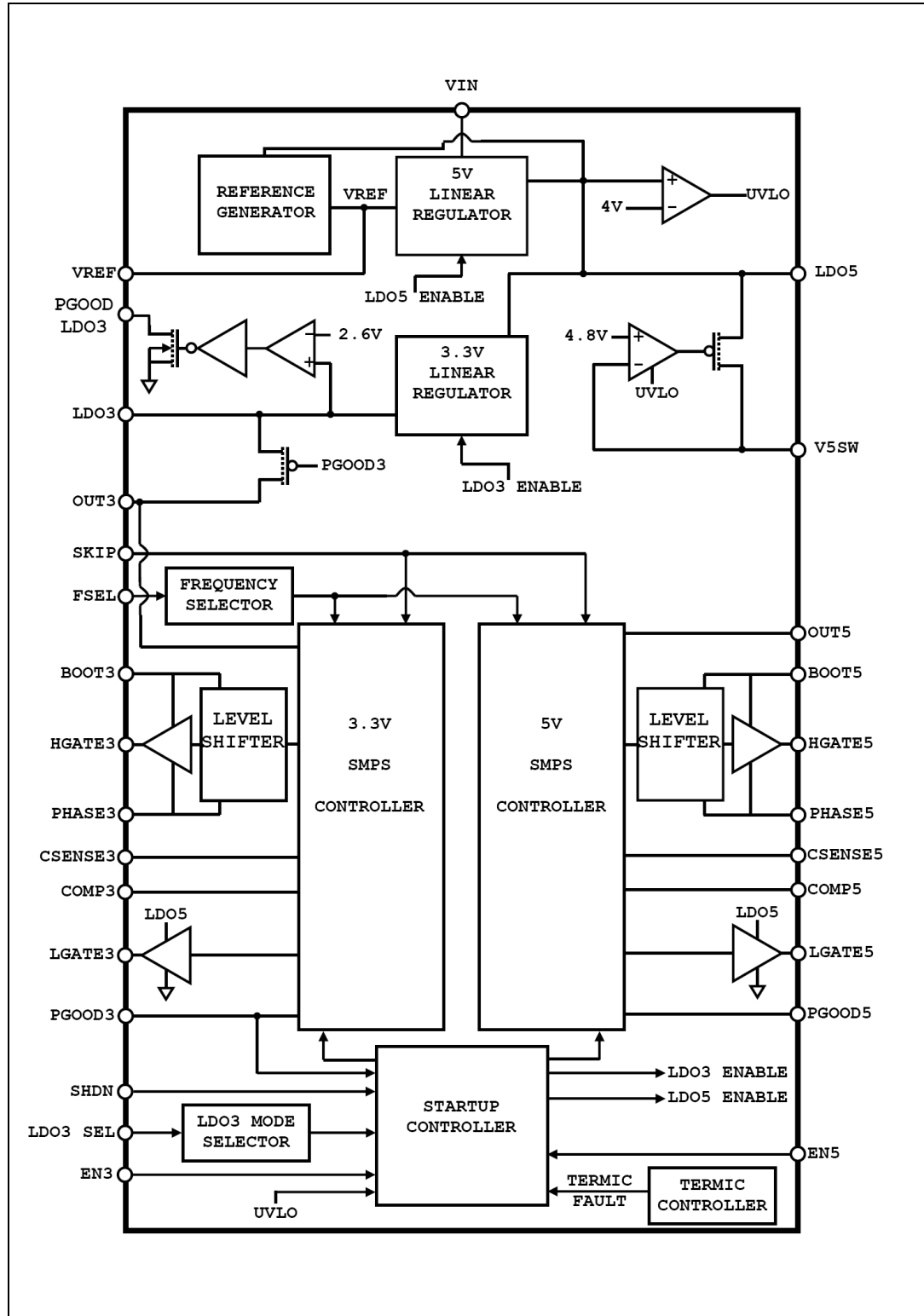
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# 1 Block diagram

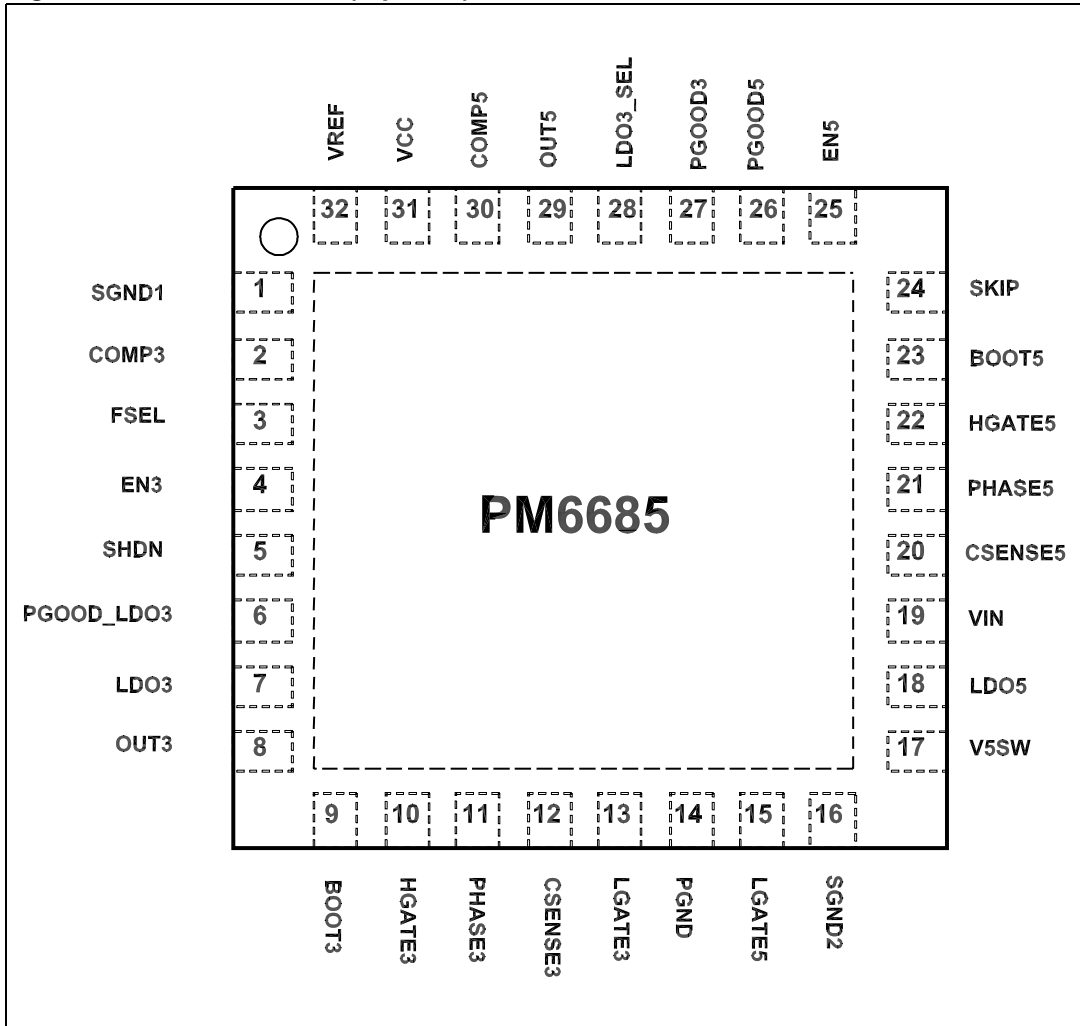
Figure 1. Functional block diagram



## 2 Pin settings

### 2.1 Connections

Figure 2. Pin connection (top view)



## 2.2 Functions

**Table 1. Pin functions**

N°	Pin	Function
1	SGND1	Signal ground. Reference for internal logic circuitry.
2	COMP3	DC voltage error compensation pin for the 3.3V switching section.
3	F <sub>SEL</sub>	Frequency selection pin.(return) It provides a selectable switching frequency for the 5V/3.3V sections with the following options: – 200kHz/300kHz, – 300kHz/400kHz ,or – 400kHz/500kz.
4	EN3	3.3V SMPS Enable Input. – EN3 = 1: the section is enabled by applying >2.4V to this pin. – EN3 = 0: the section is disabled by applying <0.8V to this pin. When the section is disabled, the high-side gate driver goes low and the low-side gate driver goes high. If the EN3 and EN5 pins are both low ('0') and the SHDN pin is high ('1'), then the device goes into Standby mode.
5	SHDN	Shutdown Control Input. The device enters Shutdown mode with 14µA of supply current, if VSHDN is less than the device-OFF threshold voltage. It does not restart until VSHDN is greater than the device-ON threshold voltage. The SHDN pin can be connected to V <sub>bat</sub> through a voltage divider to program an undervoltage lockout (UVLO). In Shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	PGOOD_LDO3	3.3V Linear Regulator Power Good Output. This pin is an open drain output. It is shorted to GND if the LDO3_SEL pin is at its low level or if the output voltage on LDO3 pin is lower than 2.6V.
7	LDO3	3.3V Linear Regulator Output. – LDO3_SEL = 0: LDO3 is always OFF. – LDO3_SEL = 1: LDO3 is always ON. The LDO3 pin can provide 100mA peak current. If the LDO3_SEL pin is connected to VREF and OUT3 is greater than the LDO3 bootstrap switch threshold, the LDO3 regulator shuts down and the LDO3 pin will be directly connected to OUT3 through a 3Ω (max) switch.
8	OUT3	3.3V Switching Section Output Voltage Sense. This pin must be directly connected to the switching section output voltage.
9	BOOT3	3.3V Switching Section Bootstrap Capacitor Connection. It supplies the high side gate driver.
10	HGATE3	3.3V Section High-side Gate Driver Output.
11	PHASE3	Switch node connection and return path for the 3.3V high side driver section.
12	CSENSE3	Current sense input for the switching 3.3V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R <sub>DS(on)</sub> sensing), or to the source of the synchronous rectifier (R <sub>SENSE</sub> sensing) to set the current limit threshold.

Table 1. Pin functions

N°	Pin	Function
13	LGATE3	Low side gate driver output for the 3.3V section.
14	PGND	Power ground.
15	LGATE5	Low side gate driver output for the 5V section.
16	SGND2	Analog circuitry signal ground.
17	V5SW	Internal 5V Regulator Bypass Connection. When the main 5V output voltage is greater than the bootstrap switch threshold, the LDO5 regulator shuts down and the LDO5 pin will be directly connected to OUT5 through a 3Ω (max) switch. <b>Note:</b> If it is not used, it must be tied to ground.
18	LDO5	5V Internal Regulator Output. The LDO5 pin supplies all gate drivers, the internal circuitry, and an external load. It can provide up to 100mA of peak current.
19	VIN	Device Input Supply Voltage. A bypass filter (4Ω and 4.7μF) between the battery and this pin is recommended..
20	CSENSE5	5V Section Current Sense Input. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDS(on) sensing), or to the source of the synchronous rectifier (RSENSE sensing) to set the current limit threshold.
21	PHASE5	Switch node connection and return path for the 5V section high side driver.
22	HGATE5	High side gate driver output for the 5V section.
23	BOOT5	5V Section Switching Bootstrap Capacitor Connection. It supplies the high side gate driver.
24	SKIP	Pulse Skipping Mode Control Input. It is a three-state pin: – SKIP = '1' (e.g. high, connected to LDO5), PWM mode is enabled. – SKIP = '0' (e.g. low, connected to GND), Pulse Skip mode is enabled. – SKIP = mid-level (e.g. connected to VREF), Pulse Skip mode is enabled and limited to a minimum frequency of 33kHz.
25	EN5	5V SMPS Enable Input. The 5V section is enabled by applying a logic high ('1', >2.4V) to this pin and is disabled by applying a logic low ('0', <0.8V). When the section is disabled the High Side Gate driver goes low and Low Side Gate driver goes high. If the EN3 and EN5 pins are low and the SHDN pin is high, the device enters into Standby mode.
26	PGOOD5	5V Section Power Good Output Signal. This pin is an open drain output. It is pulled low if the output is disabled or is out of the specified window (approximately ± 10% of its nominal value).
27	PGOOD3	3.3V Section Power Good Output Signal. This pin is an open drain output. It is pulled low if the output is disabled or is out of the specified window (approximately ± 10% of its nominal value).

Table 1. Pin functions

N°	Pin	Function
28	LDO3_SEL	3.3V Internal Linear Regulator Control pin. It is the operative mode LDO3 pin: – LDO3_SEL = '1' (e.g. high), LDO3 is always ON. – LDO3_SEL = '0' (e.g. low), LDO3 is always OFF. If the LDO3_SEL pin is connected to VREF and OUT3 is greater than the LDO3 bootstrap switch threshold, the LDO3 regulator shuts down and the LDO3 pin will be directly connected to OUT3 through a 3Ω (max) switch.
29	OUT5	5V Switching Section Output Voltage Sense. This pin must be directly connected to the output voltage of the switching section.
30	COMP5	5V Switching Section DC Voltage Error Compensation pin.
31	VCC	Device Supply Voltage pin. Connect this pin to LDO5
32	VREF	High Accuracy Output Voltage Reference (1.237V). It can deliver 50μA. Bypass to SGND with a 100nF capacitor.

## 3 Electrical data

### 3.1 Maximum rating

**Table 2. Absolute maximum ratings**

Parameter	Value	Unit	
SGND1 to SGND2	Shorted		
COMPx, FSEL, LDO3_SEL, VREF, SKIP to SGND1, SGND2	-0.3 to $V_{CC} + 0.3$	V	
ENx, SHDN, PGOD_LDO3, OUTx, PGOODx, $V_{CC}$ to SGND1, SGND2	-0.3 to 6	V	
LDO3 to SGND1, SGND2	-0.3 to LDO5 + 0.3	V	
LGATEx to PGND	-0.3 to LDO5 + 0.3	V	
HGATEx and BOOTx, to PHASEx	-0.3 to 6	V	
PHASEx to PGND	-0.6 to 36	V	
CSENSEx, to PGND	-0.6 to 42	V	
CSENSEx to BOOTx	-6 to 0.3	V	
V5SW, LDO5 to PGND	-0.3 to 0.6	V	
VIN to PGND	-0.3 to 36	V	
PGND to SGND1, SGND2	-0.3 to 0.3	V	
VIN pin Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- "Human Body Model" acceptance criteria: "	Normal Performance	$\pm 1000$	V
	Other pins	$\pm 2000$	

### 3.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal Resistance Junction to Ambient	35	°C/W
$T_{STG}$	Storage Temperature Range	-40 to 150	°C
$T_J$	Junction Operating Temperature Range	-10 to 125	°C

## 4 Electrical characteristics

$V_{IN} = 12V, T_A = 0^{\circ}C$  to  $85^{\circ}C$ , unless otherwise specified

**Table 4. Electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Supply section</b>						
$V_{IN}$	Input Voltage Range	$V_{OUT} = V_{REF}$ LDO5 in regulation FSEL to GND	5.5		28	V
$V_{CC}$	IC Supply Voltage		4.5		5.5	V
$V_{V5SW}$	Turn-on Voltage Threshold			4.8	4.9	V
	Turn-off Voltage Threshold		4.6	4.75		V
	Hysteresis		20	50		mV
$V_{V5SW}$	Maximum Operating Range				5.5	V
$R_{DS(on)}$	LDO5 Internal Bootstrap Switch Resistance	$V_{5SW} > 4.9V$		1.8	3	$\Omega$
	LDO3 Internal Bootstrap Switch Resistance	$V_{OUT3} = 3.3V$		1.8	3	$\Omega$
	OUT3, OUT5 Discharge Mode On-resistance			16	25	$\Omega$
	OUT3, OUT5_ Discharge Mode Synchronous Rectifier Turn-on level		0.2	0.35	0.5	V
$P_{IN}$	Operating Power Consumption	$V_{OUT5} > 5.1V, V_{OUT3} > 3.34V$ $V_{5SW}$ to 5V LDO5, LDO3 no load			4	mW
$I_{SH}$	$V_{IN}$ Shutdown Current	SHDN connected to GND,		14	18	$\mu A$
$I_{SB}$	$V_{IN}$ Standby Current	ENx to GND, $V_{5SW}$ to GND, LDO3_SEL to 5V		270	380	$\mu A$
<b>Shutdown section</b>						
$V_{SHDN}$	Device On Threshold		1.2	1.5	1.7	V
	Device Off Threshold		0.8	0.85	0.9	V

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Soft start section</b>						
	Soft Start Ramp Time		2		3.5	ms
<b>Current limit and zero crossing comparator</b>						
$I_{CSENSE}$	Input Bias Current Limit		90	100	110	$\mu$ A
	Comparator Offset	$V_{CSENSE} - V_{PGND}$	-6		6	mV
	Zero Crossing Comparatot Offset	$V_{PGND} - V_{PHASE}$	-1		11	mV
	Fixed Negative Current Limit Threshold	$V_{PGND} - V_{PHASE}$		-120		mV

**Table 5. Electrical characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>ON time pulse width</b>						
T <sub>ON</sub>	ON-Time Duration	FSEL to GND	OUT5 = 5V		2083	ns
			OUT3 = 3.3V		917	
		FSEL to VREF	OUT5 = 5V		1390	
			OUT3 = 3.3V		688	
		FSEL to LDO5	OUT5 = 5V		1040	
			OUT3 = 3.3V		550	
<b>OFF Time</b>						
T <sub>OFFMIN</sub>	Minimum Off Time			400	500	ns
<b>Voltage reference</b>						
V <sub>REF</sub>	Voltage Accuracy	4.2V < V <sub>LDO5</sub> < 5.5V	1.224	1.237	1.249	V
	Load Regulation	-100µA < I <sub>REF</sub> < 100µA	-4		4	mV
	Undervoltage Lockout Fault Threshold	Falling edge of REF			0.95	V
<b>Integrator</b>						
COMP	Over Voltage Clamp	Normal mode		250		mV
		Pulse skip mode		60		
	Under Voltage Clamp			-150		
<b>Line regulation</b>						
		Both SMPS, 6V < V <sub>IN</sub> < 28V			0.004	%/V
<b>LDO5 linear regulator</b>						
V <sub>LDO5</sub>	LDO5 Linear Output Voltage	6V < V <sub>IN</sub> < 28V, 0 < I <sub>LDO5</sub> < 50mA	4.9	5.0	5.1	V
	LDO5 Line Regulation	6V < V <sub>IN</sub> < 28V, I <sub>LDO5</sub> = 50mA, LDO3_SEL tied to GND			0.004	%/V
I <sub>LDO5</sub>	LDO5 Current Limit	V <sub>LDO5</sub> > UVLO, I <sub>LDO3</sub> = 0A, V <sub>OUT5</sub> > 5.1V, V <sub>OUT3</sub> > 3.34V	300	350	400	mA
UVLO	Under Voltage Lockout of LDO5		3.94	4	4.13	V
<b>LDO3 linear regulator</b>						
V <sub>LDO3</sub>	LDO3 Linear Output Voltage	0.5mA < I <sub>LDO3</sub> < 50mA	3.23	3.3	3.37	V

Table 5. Electrical characteristics

$I_{LDO3}$	LDO3 Current limit	$V_{LDO5} > UVLO$	130		200	mA
<b>High and low gate drivers</b>						
	HGATE Driver On-resistance	HGATEx high state(pullup)		2.0	3	$\Omega$
		HGATEx low state (pulldown)		1.6	2.7	$\Omega$
	LGATE Driver On-resistance	LGATEx high state(pullup)		1.4	2.1	$\Omega$
		LGATEx low state (pulldown)		0.8	1.2	$\Omega$
<b>PGOOD pins UVP/OVP Protections</b>						
OVP	Over Voltage Threshold	Both SMPS sections with respect to VREF.	113	116	120	%
UVP	Under Voltage Threshold		66	70	72	%
PGOOD3,5	Upper Threshold (VFB-VREF)		107	110	113	%
	Lower Threshold (VFB-VREF)		90	92	94	%
$I_{PGOOD3,5}$	PGOOD Leakage Current	$V_{PGOOD3,5}$ forced to 5.5V			1	$\mu$ A
$V_{PGOOD3,5}$	Ouput Low Voltage	ISink=4mA	0	150	250	mV
PGOOD LDO3	Rising Voltage Threshold			77.7	81.1	%
	Falling Voltage Threshold		72.1	76.6		%
	Hysteresis		20	30		mV
$I_{PGOOD\_LDO3}$	PGOOD Leakage Current	$V_{PGOOD\_LDO3}$ forced to 5.5V			1	$\mu$ A
$V_{PGOOD\_LDO3}$	Ouput Low Voltage	ISink=4mA	0	150	250	mV
<b>Thermal shutdown</b>						
$T_{SDN}$	SHUTDOWN Temperature				150	$^{\circ}$ C
<b>Power management pins</b>						
EN3,5	SMPS Disabled threshold		0.8			V
	SMPS Enabled threshold				2.4	
FSEL	Frequency Selection Range	Low level <sup>(1)</sup>			0.5	V
		Middle level <sup>(1)</sup>	1.0		$V_{LDO5}-1.5$	
		High level <sup>(1)</sup>	$V_{LDO5}-0.8$			
LDO3 SEL	3.3V Linear Regulator Selection Pin	Always-off level <sup>(1)</sup>			0.5	
		Bootstrap level <sup>(1)</sup>	1.0		$V_{LDO5}-1.5$	
		Always-on level <sup>(1)</sup>	$V_{LDO5}-0.8$			

Table 5. Electrical characteristics

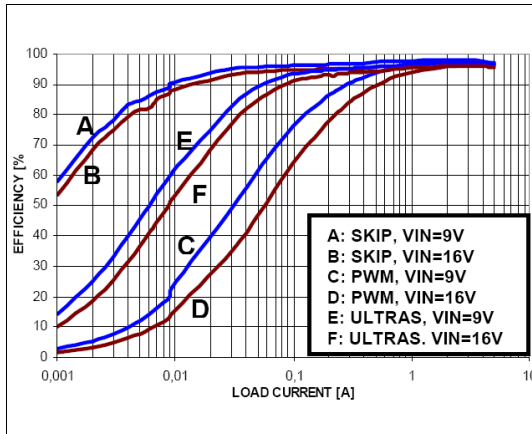
SKIP	Pulse Skip Mode	(1)			0.5	V
	PWM Mode	(1)	1.0		$V_{LDO5}-1.5$	
	No audible Mode	(1)	$V_{LDO5}-0.8$			
	Input leakage current	$V_{EN3,4} = 0 \text{ to } 5V$			1	$\mu A$
		$V_{SKIP} = 0 \text{ to } 5V$			1	
		$V_{SHDN} = 0 \text{ to } 5V$			0.1	
		$V_{FSEL} = 0 \text{ to } 5V$			1	
		$V_{LDO3\_SEL} = 0 \text{ to } 5V$			1	

1. By design

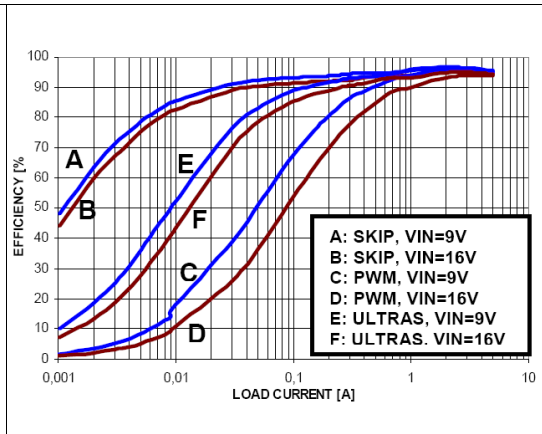
## 5 Typical operating characteristics

FSEL = GND (200/300KHz), SKIP = GND (skip mode), LDO3\_SEL = VREF, V5SW = OUT5, input voltage VIN = 12V, SHDN, EN3 and EN5 high, no load unless specified.

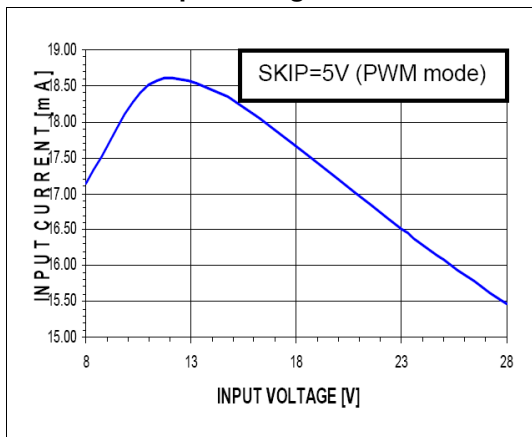
**Figure 3. 5V Output efficiency vs. load current**



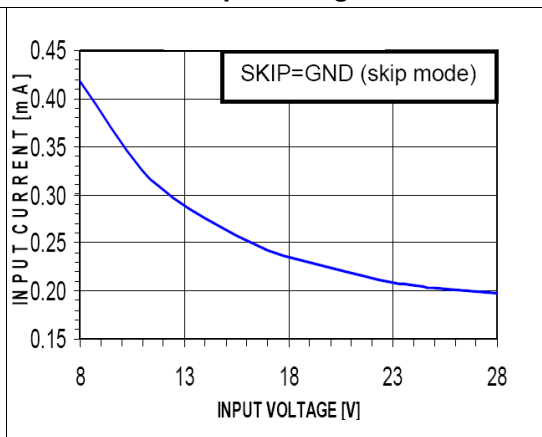
**Figure 4. 3.3V Output efficiency vs. load current**



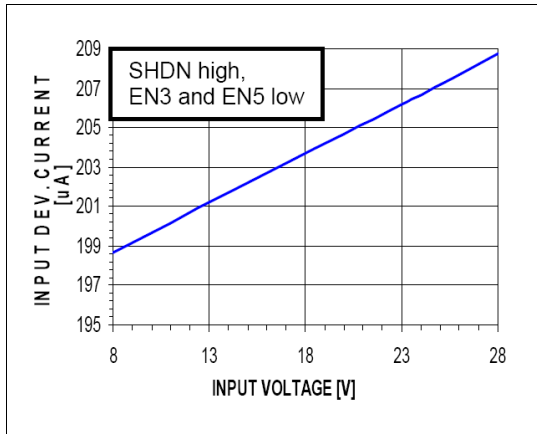
**Figure 5. PWM no load input battery vs. input voltage**



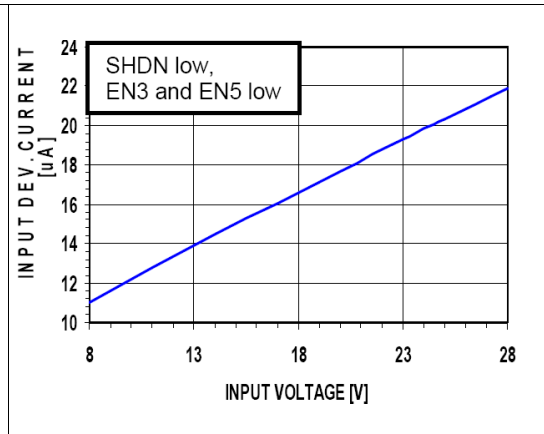
**Figure 6. Skip no load battery current vs. input voltage**



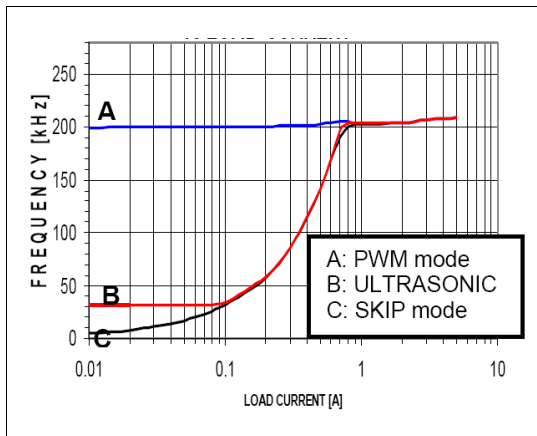
**Figure 7. Standby mode input battery current vs. input voltage**



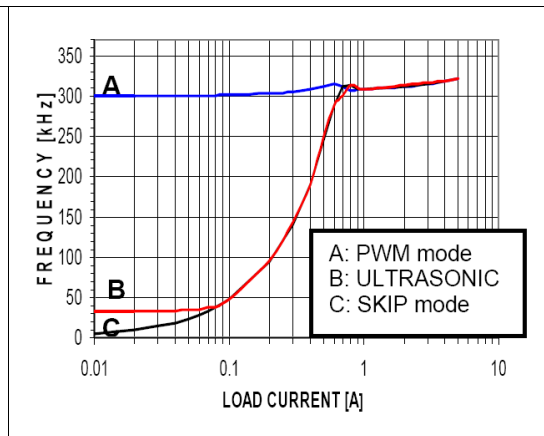
**Figure 8. Shutdown mode input device current vs. input voltage**



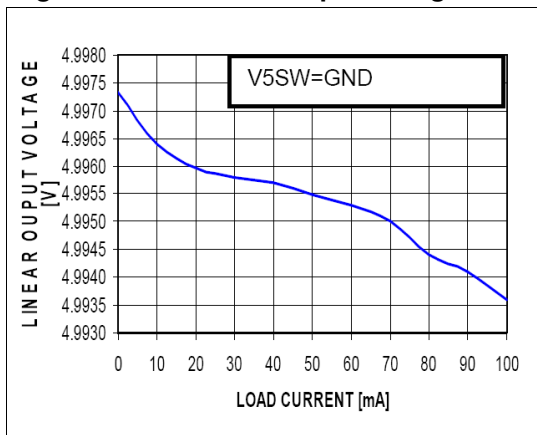
**Figure 9. 5V switching frequency vs. load current**



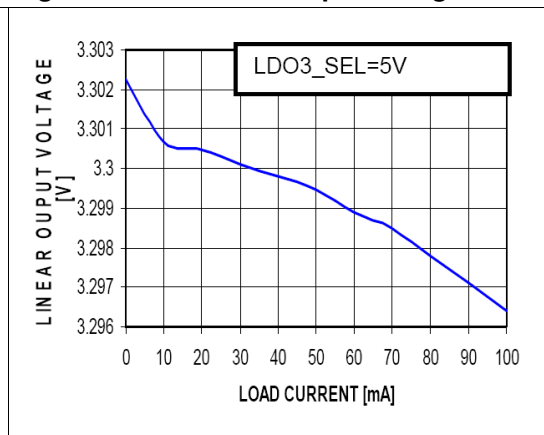
**Figure 10. 3.3V switching frequency vs. load current**



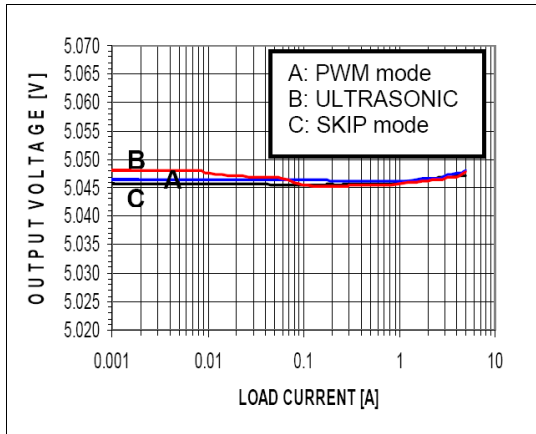
**Figure 11. LDO5 vs. output voltage**



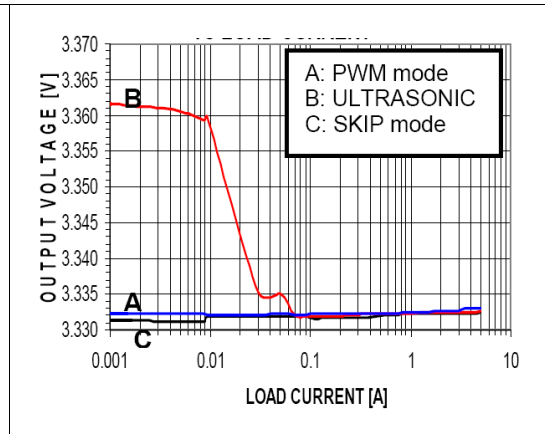
**Figure 12. LDO3 vs. output voltage**



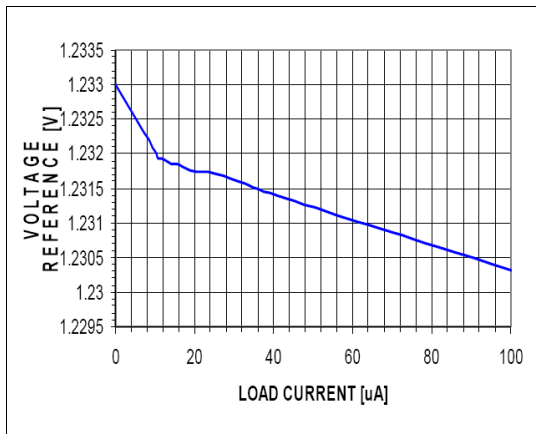
**Figure 13. 5V Voltage regulation vs. load current**



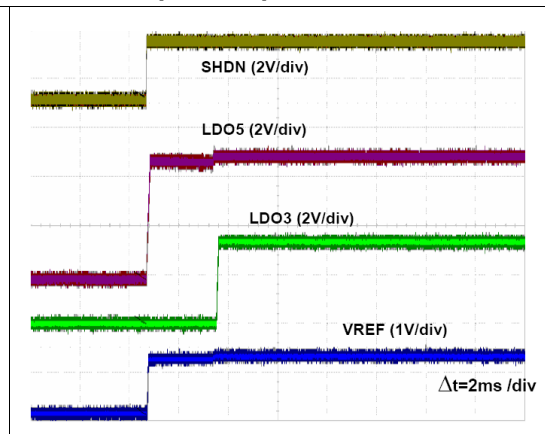
**Figure 14. 3.3V voltage regulation vs. load current**



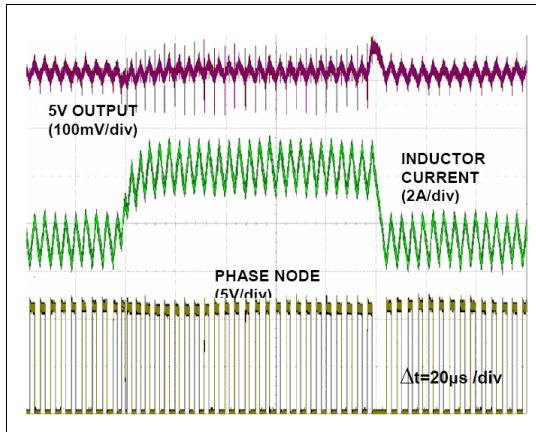
**Figure 15. Voltage reference vs. load current**



**Figure 16. REF, LDO3 and LDO5 power-up**



**Figure 17. 5V load transient**



**Figure 18. 3.3V load transient**

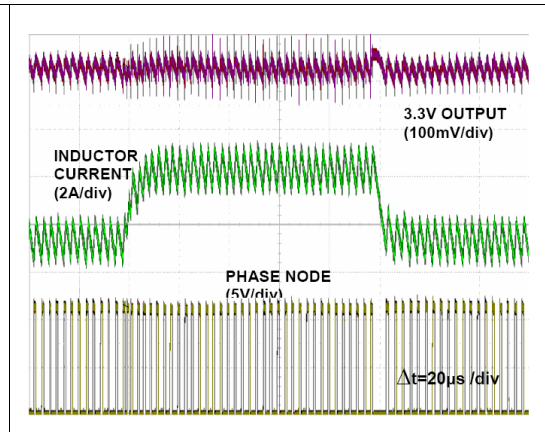


Figure 19. 5V Soft start (0.75Ω Load)

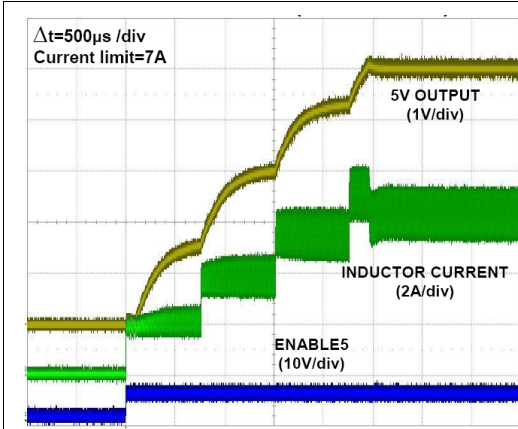


Figure 20. 3.3V soft start (0.55Ω Load)

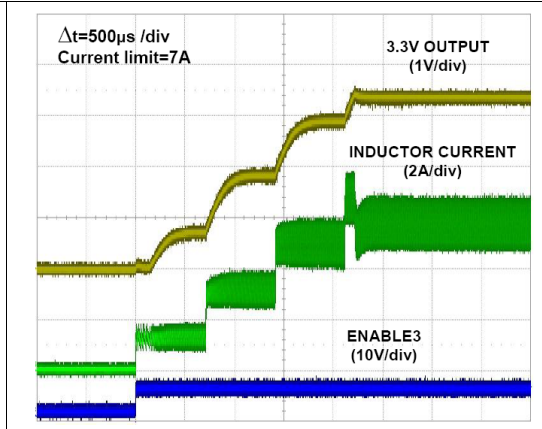


Figure 21. 5V Soft end (No Load)

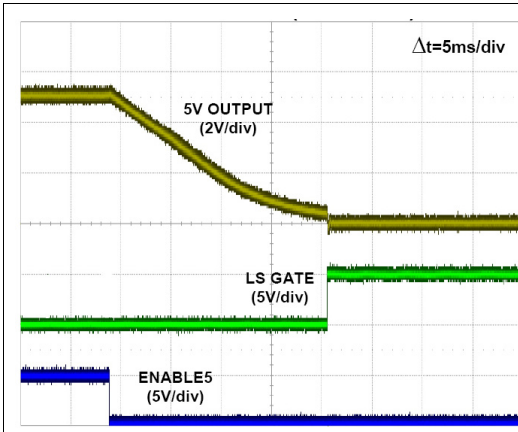


Figure 22. 3.3V Soft end (No Load)

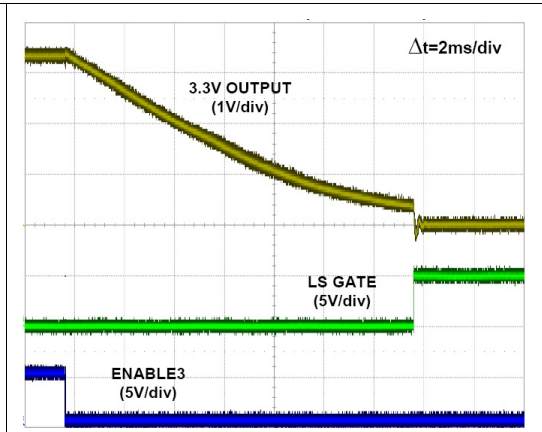


Figure 23. 5V Soft end (1Ω Load)

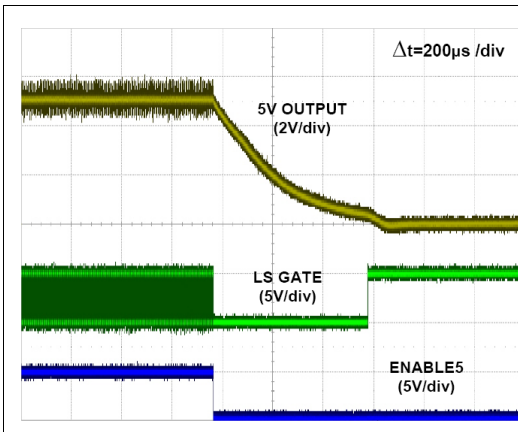


Figure 24. 3.3V Soft end (1Ω Load)

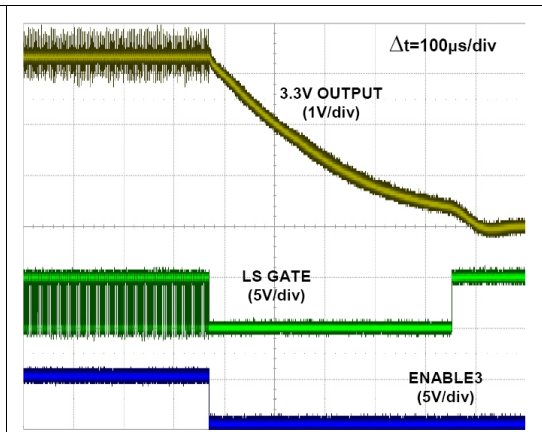


Figure 25. 5V No audible skip mode

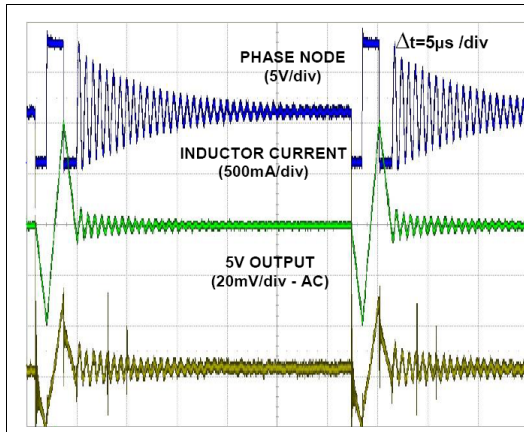
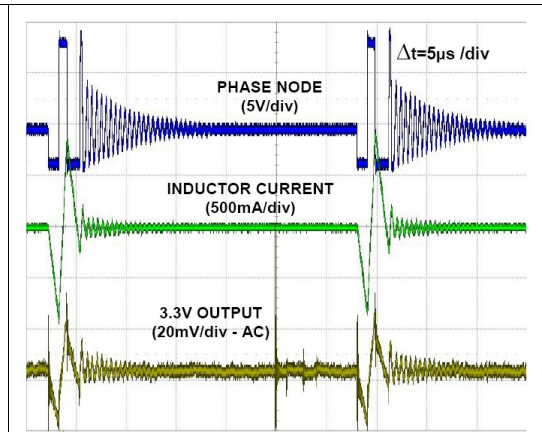
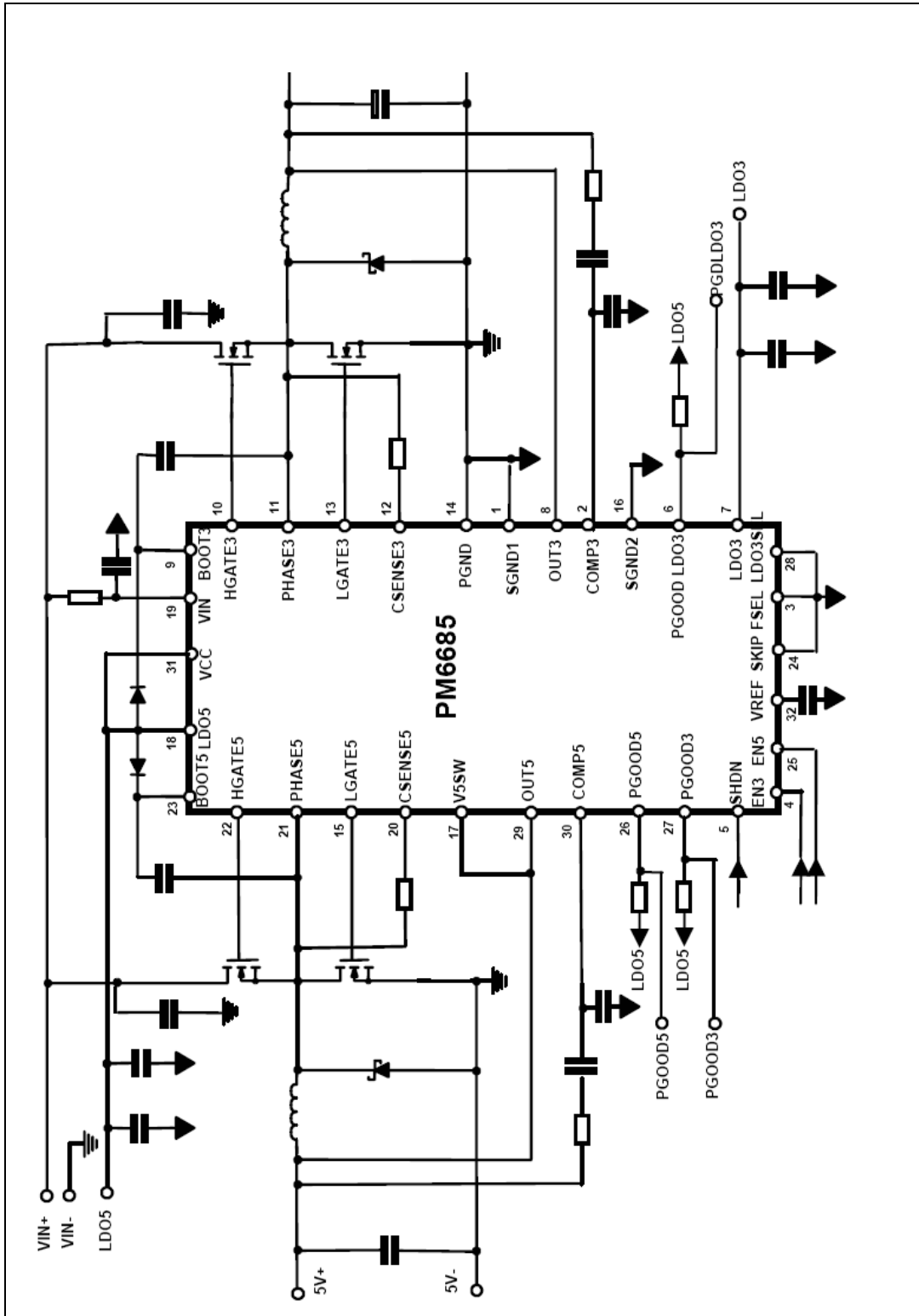


Figure 26. 3.3V No audible skip mode



# 6 Application schematic

Figure 27. Simplified application schematic



## 7 Device description

The PM6685 is a dual step-down controller dedicated to provide logic voltages for notebook computers.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in [Figure 27](#). The PM6685 regulates two fixed output voltages: 5V and 3.3V. The switching frequency of the two sections can be adjusted to 200/300kHz, 300/400kHz or 400/500kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected. The PM6685 includes also two linear regulators (LDO5 and LDO3) that allow the shutdown of the respective switching sections in low consumption status. On the other hand, to maximize the efficiency in higher consumption status, the linear regulators can be turned OFF and their outputs can be supplied directly from the switching outputs. The PM6685 provides protection versus overvoltage, undervoltage and overtemperature as well as power good signals for monitoring purposes. An external 1.237V reference is available.

### 7.1 Constant ON time PWM control

If the SKIP pin is tied to 5V, the device works in PWM mode. Each power section has an independent on time control. The PM6685 implements a pseudo-fixed switching frequency, Constant ON Time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator.

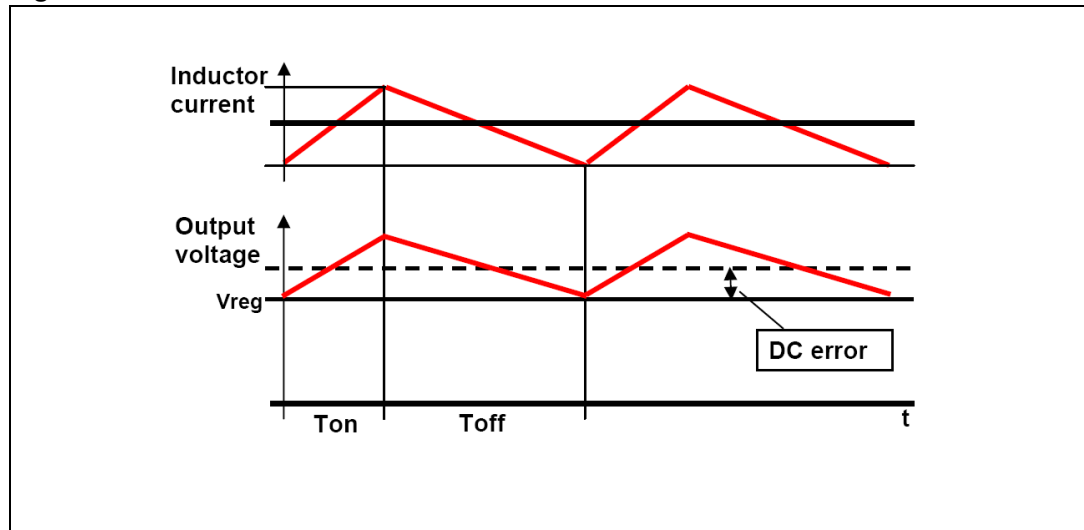
In this way, the output capacitor's ESR acts as a current sense resistor, providing the appropriate ramp signal to the PWM comparator. ON-time one-shot duration is directly proportional to the output voltage, sensed at the OUT5/OUT3 pins, and inversely proportional to the input voltage, sensed at the VIN pin, as follows:

#### Equation 1

$$T_{ON} = K \cdot \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages. When the output voltage goes lower than the regulated voltage  $V_{REG}$ , the ON-time one shot generator directly drives the high side mosfet for a fixed ON time, allowing the inductor current to increase; After the ON time, an OFF time phase, where the low side MOSFET is turned on, will follow. [Figure 28](#) shows the inductor current and the output voltage waveforms in PWM mode.

**Figure 28. Constant ON time PWM Control**



The duty cycle of the buck converter in steady state is:

**Equation 2**

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency  $f_{SW}$ :

**Equation 3**

$$f_{SW} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{on} \times \frac{V_{OUT}}{V_{IN}}} = 1 / K_{on}$$

The steady-state switching frequency is theoretically independent from the battery and output voltages (see [Figure 28: Constant ON time PWM Control on page 22](#)).

The frequency depends on the parasitic voltage drops that are present during the charging path:

- High side switch resistance,
- Inductor resistance (DCR), and
- Discharging path (low side switch resistance, DCR).

This results in the switching frequency increasing as a function of the load current.

Standard switching frequency values can be selected for both sections by the FSEL pin FSEL as shown in [Table 6](#).

Table 6.  $F_{SEL}$  pin selection

FSEL	SMPS 5V		SMPS 3.3V	
	Frequency	$K_{ON}$	Frequency	$K_{ON}$
SGND	200KHz	5.0us	300kHz	3.33us
VREF	300kHz	3.33us	400kHz	2.5us
LDO5	400kHz	2.5us	500kHz	2.0us

## 7.2 Constant ON time architecture

A minimum OFF time constraint (300ns, typ) is introduced to allow inductor valley current sensing on the synchronous switch. A minimum ON time(70ns, typ) is also introduced to ensure the start-up switching sequence.

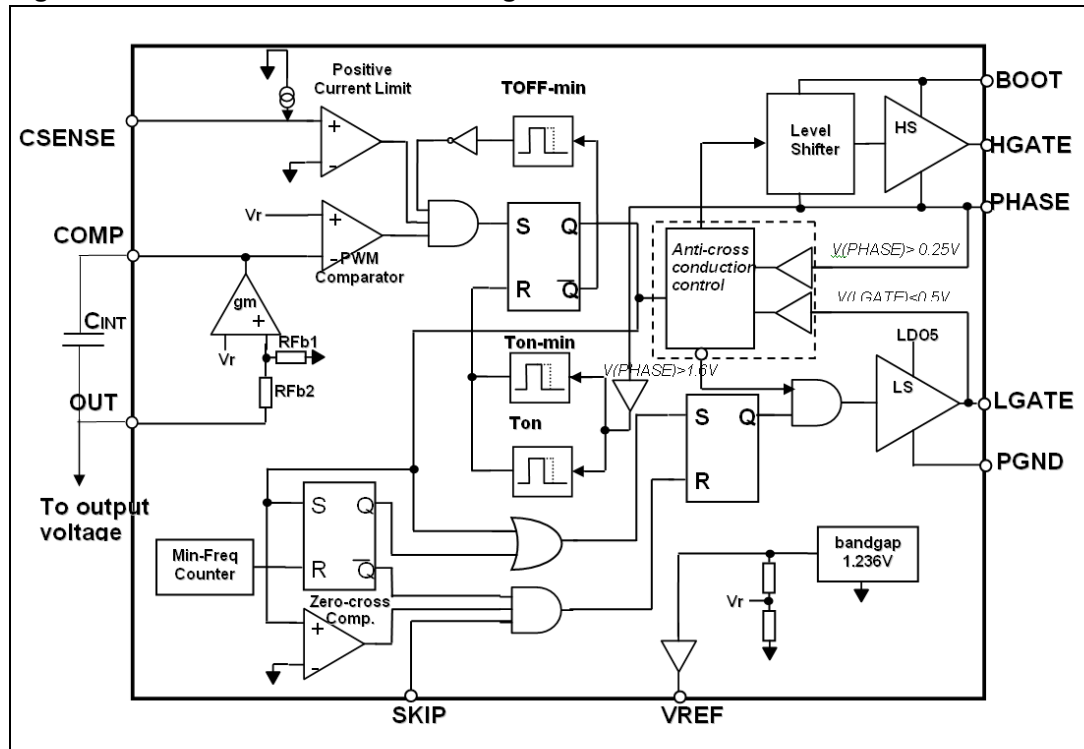
PM6685 has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously:

- The PWM comparator is high,
- The synchronous rectifier current is below the current limit threshold, and
- The minimum OFF time has timed-out.

Once the ON time has timed-out, the high side switch is turned off, while the synchronous switch is turned on, according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator, which is a scaled-down replica of the output voltage ripple (see the Rfb1/Rfb2 divider, [Figure 29](#)), reaches the valley limit (determined by internal reference  $V_r = 0.9V$ ), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 29. Constant ON-time block diagram



### 7.3 Output ripple compensation and loop stability

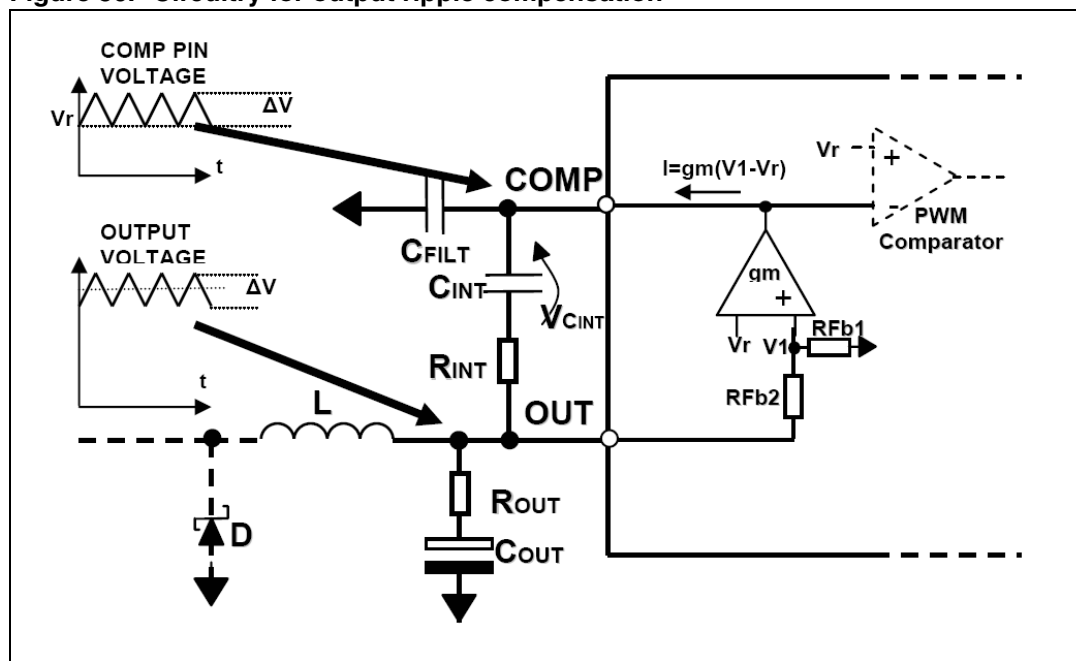
In a classic Constant ON Time control system, the output voltage valley value is regulated, and not the average value, as shown in [Figure 28](#). In this condition, the output voltage ripple is the source of a DC static error.

To compensate for this error, a network integrator can be introduced in the control loop by connecting the output voltage to the COMP5/COMP3 pin (for the 5V and 3.3V sections, respectively) through a capacitor  $C_{INT}$  (see [Figure 30](#)).

The integrator amplifier generates a current proportional to the DC errors, which decreases the output voltage, in order to compensate for the total static error, including the voltage drop on the PCB traces.

Additionally,  $C_{INT}$  provides an AC path for the output ripple. In steady-state, the voltage on the COMP5/COMP3 pin is the sum of the reference voltage  $V_R$  and the output ripple (see [Figure 30](#)). In fact, when the voltage on the COMP pin reaches  $V_R$ , a fixed  $t_{ON}$  begins and the output increases.

**Figure 30. Circuitry for output ripple compensation**



For example, we consider  $V_O = 5V$  with an output ripple of  $\Delta V = 50mV$ . Considering  $C_{INT} \gg C_{FILT}$ , the  $C_{INT}$  DC voltage drop  $V_{CINT}$  is about  $5V - V_R + 25mV = 4.125V$ .  $C_{INT}$  ensures that there is an AC path for the output voltage ripple. The COMP pin ripple is a replica of the output ripple with a DC value of  $V_R + 25mV = 925mV$ .

The design of external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 30mV, the feedback network is usually enough to keep the loop stable. The system stability depends primarily on the output capacitor zero frequency. The following condition should be satisfied:

**Equation 4**

$$\int SW > k \times \int Z_{OUT} = \frac{k}{2\pi \times C_{OUT} \times R_{OUT}}$$

Where  $k$  is a design parameter greater than 3 and  $R_{out}$  is the ESR of the output capacitor. It determinates the minimum integrator capacitor value  $C_{INT}$ :

**Equation 5**

$$C_{INT} > \frac{g_m}{2\pi \times \left( \frac{f_{SW}}{k} - f_{Z_{OUT}} \right)} \times \frac{V_R}{V_{OUT}}$$

where  $g_m = 50\mu S$  is the integrator transconductance.

In order to reduce noise on COMP pin, it is possible to add a resistor  $R_{INT}$  and a capacitor  $C_{FILT}$  that, together with  $C_{INT}$ , realize a low pass filter (See [Figure 30](#)). The cutoff frequency  $f_{CUT}$  must be much greater (10 or more times) than the switching frequency of the section:

**Equation 6**

$$R_{INT} = \frac{1}{2\pi \times f_{CUT} \times \frac{C_{INT} \times C_{FILT}}{C_{INT} + C_{FILT}}}$$

Due to the capacitive divider ( $C_{INT}$ ,  $C_{FILT}$ ), the ripple voltage at the COMP pin is given by:

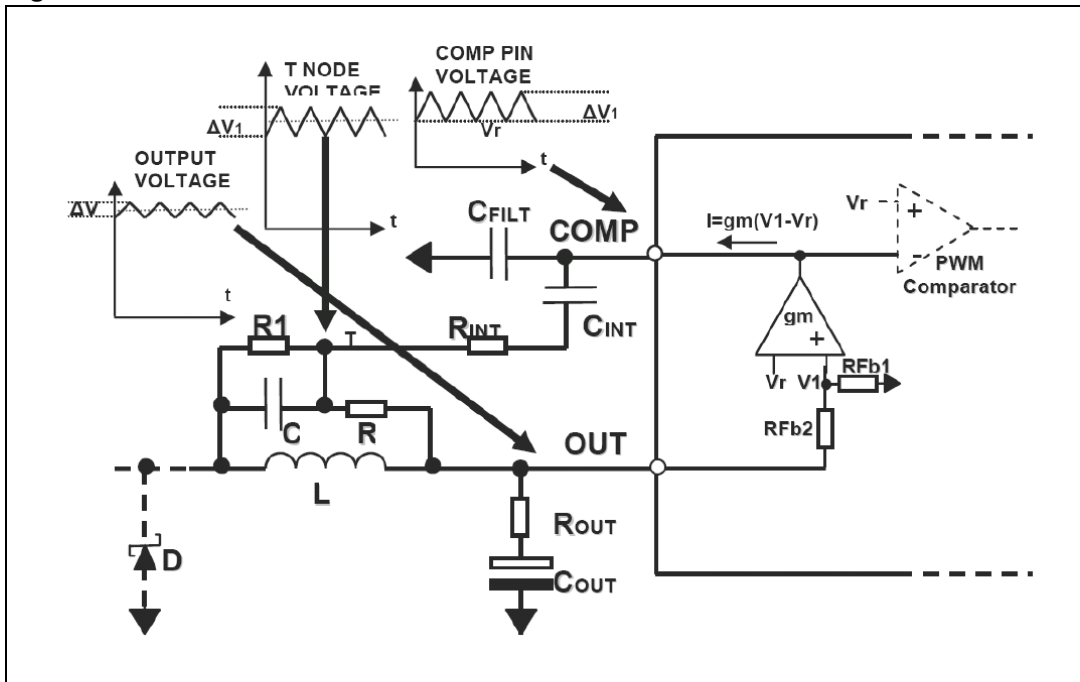
**Equation 7**

$$V_{RIPPLE_{INT}} = V_{RIPPLE_{OUT}} \times \frac{C_{INT}}{C_{INT} + C_{FILT}} = V_{RIPPLE_{OUT}} \times q$$

Where  $V_{RIPPLE_{OUT}}$  is the output ripple and  $q$  is the attenuation factor of the output ripple.

If the ripple is very small (lower than approximately 30mV), a further compensation network, named virtual ESR network, is needed. This additional part generates a triangular ripple that is added to the ESR output voltage ripple at the input of the integrator network. The complete control schematic is represented in [Figure 30](#).

Figure 31. Virtual ESR network



The integrator input voltage (T node) is the sum of the output voltage and the triangular waveform generated by the virtual ESR network. In fact the virtual ESR network behaves like a further equivalent ESR  $R_{ESR}$ .

A good trade-off is to design the network in order to achieve an RESR given by:

**Equation 8**

$$R_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L} - R_{OUT}$$

where,

- $\Delta I_L$  = the inductor current ripple, and
- $V_{RIPPLE}$  is the overall ripple of the T node voltage.

It should be chosen higher than approximately 30mV.

The new closed loop gain depends on  $C_{INT}$ . In order to ensure stability it must be verified that:

**Equation 9**

$$C_{INT} > \frac{g_m}{2\pi \times \int Z} \times \frac{V_R}{V_{OUT}}$$

Where:

**Equation 10**

$$\int Z = \frac{1}{2\pi \times C_{OUT} \times R_{TOT}}$$

with:

**Equation 11**

$$R_{TOT} = R_{OUT} + R_{ESR}$$

Moreover  $C_{INT}$  must meet the following condition:

**Equation 12**

$$\int SW > k \times \int Z = \frac{k}{2\pi \times C_{OUT} \times R_{TOT}}$$

where  $R_{TOT}$  is the sum of the ESR of the output capacitor  $R_{OUT}$  and the equivalent ESR given by the virtual ESR network RESR.  $k$  is a free design parameter greater than 1 (usually 10) and determines the minimum integrator capacitor value  $C_{INT}$ :

**Equation 13**

C must be selected as shown:

$$C_{INT} > \frac{g_m}{2\pi \times \left( \frac{\int SW}{k} - \int Z \right)} \times \frac{V_R}{V_{OUT}}$$

**Equation 14**

$$C > 5 \times C_{INT}$$

R must be chosen in order to have enough ripple voltage on integrator input:

**Equation 15**

$$R = \frac{L}{R_{ESR} \times C}$$

R1 can be selected as follows:

**Equation 16**

$$R1 = \frac{R \times \left( \frac{1}{C \times \pi \times \int Z} \right)}{R - \frac{1}{C \times \pi \times \int Z}}$$

Example:

- 5V section
- $f_{SW} = 200\text{KHz}$
- $L = 4.7\mu\text{H}$
- $C_{OUT} = 100\mu\text{F}$  ceramic ( $R_{OUT} \approx 0\Omega$ )
- We design  $R_{ESR} = 30\text{m}\Omega$
- We choose  $C_{INT} = 560\text{pF}$  by equations 9, 10 and 12
- $C_{FILT} = 110\text{pF}$ ,  $R_{INT} = 1\text{K}\Omega$  by eq.6, 7
- $C = 4.7\text{nF}$  by Eq.14
- Then  $R = 33\text{K}\Omega$  (eq.15)
- and  $R1 = 1.3\text{K}\Omega$  (eq.16)

## 7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in Skip mode.

At light loads, a zero-crossing comparator truncates the low side switch ON time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode (DCM). The threshold between continuous conduction mode (CCM) and DCM is:

**Equation 17**

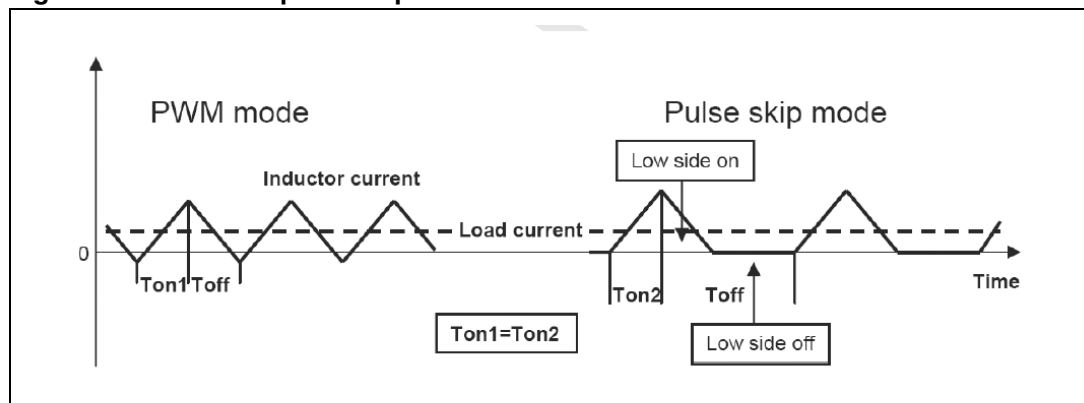
$$I_{LOAD(Skip)} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current does not cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

Figure 32 shows inductor current waveforms in PWM and SKIP mode. In order to keep average inductor current equal to load current, in SKIP mode some switching cycles are skipped. When the output ripple reaches the regulated voltage  $V_{REG}$ , a new cycle begins. The off cycle duration and the switching frequency depend on the load condition.

As a result of the control technique, losses are reduced at light loads, improving the system efficiency.

**Figure 32. PWM and pulse skip mode inductor current**



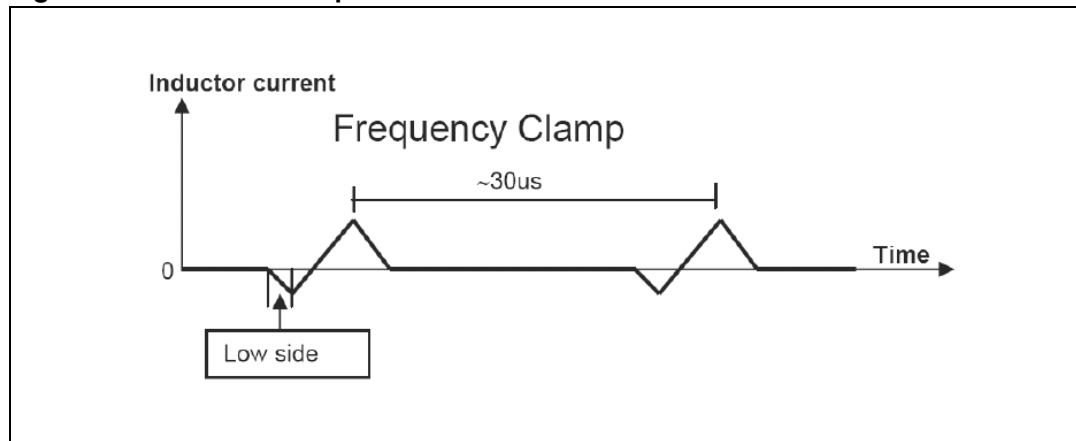
## 7.5 No-audible skip mode

If the SKIP pin is tied to VREF, a no-audible Skip mode with a minimum switching frequency of 33kHz is enabled. At light load condition, if there is not a new switching cycle within a 30µs(typ) period, a no-audible Skip mode cycle begins.

The low side switch is turned on until the output voltage crosses about  $V_{REG} + 1\%$ . The high side MOSFET is then turned on for a fixed ON time period. Afterwards, the low side switch is

enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33kHz. As a consequence of this control, the regulated voltage can be slightly higher than  $V_{REG}$  (up to 1%). If, due to the load, the frequency is higher than 33kHz, the device will work as in regular Skip mode. No-audible Skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

Figure 33. No-audible skip mode



### 7.6 Current limit

The current-limit circuit employs a "valley" current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element can be the low side MOSFET ON-resistance (Figure 33) or a discrete resistor in series with the source of the low side MOSFET (Figure 34). The first method ensures higher efficiency but lower accuracy, while with the second one ensures higher accuracy but lower efficiency

Figure 34.  $R_{SENSE}$  sensing technique

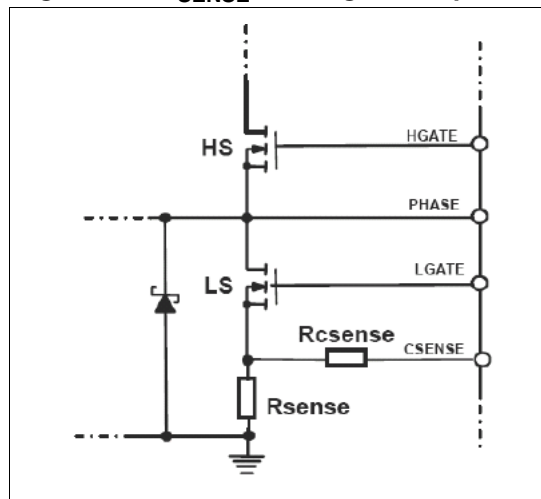
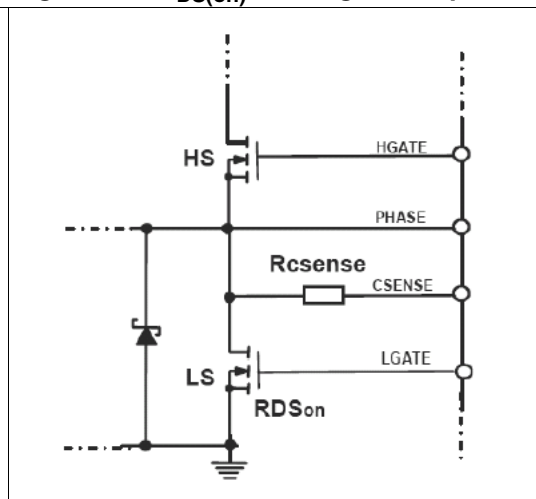


Figure 35.  $R_{DS(on)}$  sensing technique



An internal  $100\mu A$  current source is connected to  $C_{SENSE}$  pin and determines a voltage drop on  $R_{CSENSE}$ . If the voltage across the sensing element is greater than this voltage drop, the

controller does not initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current. Moreover the maximum DC load is equal to the valley current limit plus half of the inductor ripple current.

The valley current limit can be set with resistor  $R_{CSENSE}$ :

**Equation 18**

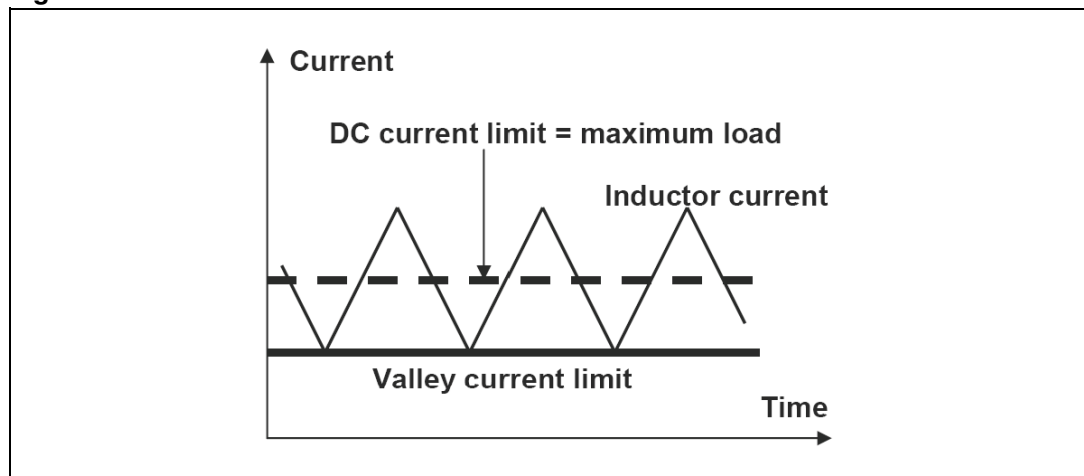
$$R_{CSENSE} = \frac{R_{DS(on)} \times I_{Lvalley}}{100\mu A} \quad (R_{DS(on)} \text{ sensing technique})$$

**Equation 19**

$$R_{CSENSE} = \frac{R_{SENSE} \times I_{Lvalley}}{100\mu A} \quad (R_{SENSE} \text{ sensing technique})$$

PM6685 also provides a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between the PHASE and SGND pins, comparing the magnitude drop on the PHASE node with an internal fixed voltage of 120mV.

**Figure 36. Current waveforms in current limit conditions**

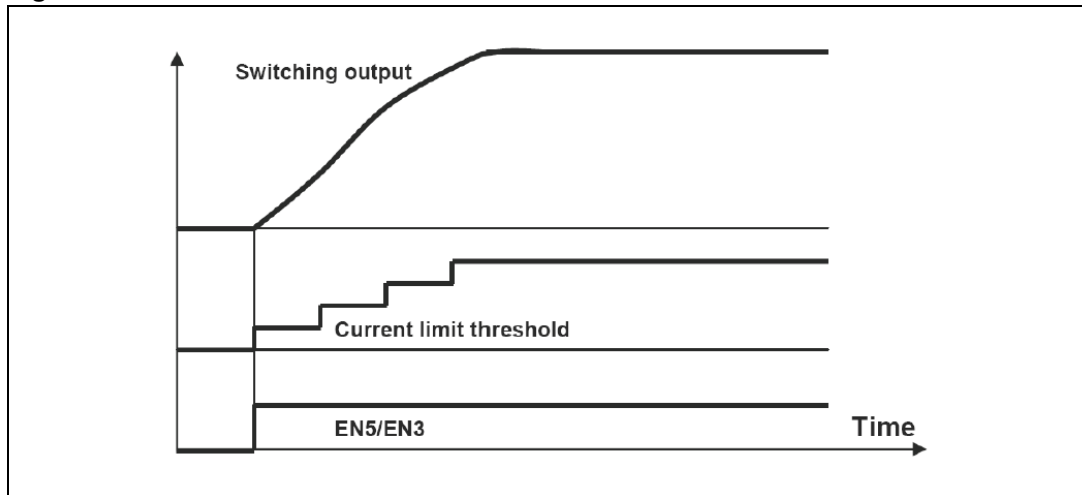


**7.7 Soft start and soft end**

Each switching section is enabled separately by asserting the EN5 and EN3 pins high, respectively. In order to realize the soft start, the overcurrent threshold is set 25% of the nominal value and the undervoltage protection is disabled at startup (see related section). The controller starts charging the output capacitor working within the current limit. The overcurrent threshold is increased from 25% to 100% of the nominal value with steps of 25% every 700µs (typ). After 2.8ms (typ), the undervoltage protection is enabled. The soft start time is not programmable.

When a switching section is turned off (EN5/EN3 pins are low), the controller enters into Soft End mode. The output capacitor is discharged through an internal 10Ω Power MOSFET switch; when the output voltage reaches 0.3V, the low side MOSFET turns on, keeping the output to ground. The Soft End time also depends on load conditions.

**Figure 37. Soft start waveforms**



## 7.8 Gate drivers

The integrated, high current drivers allow users to choose different power MOSFETs for their applications. The high side driver MOSFET uses a bootstrap circuit which is indirectly supplied by the LDO5 output. The BOOT and PHASE pins work as supply and return rails for the HS driver, respectively. The low side driver uses the internal LDO5 output for the supply rail and PGND pin as the return rail.

An important feature of the gate drivers is the adaptive anti-cross conduction protection, which prevents the high side and low side MOSFET from being ON at the same time. When the high side MOSFET is turned off, the voltage at the phase node begins to fall.

The low side MOSFET is turned on when the voltage at the phase node reaches an internal threshold. When the low side MOSFET is turned off, the high side remains OFF until the LGATE pin voltage goes approximately under 1V.

The drivers' power dissipation is a function of the total gate charge of the external power MOSFETs, and the switching frequency, as shown in Equation 19:

**Equation 20**

$$P_{\text{driver}} = V_{\text{driver}} \times Q_g \times \int \text{sw}$$

## 7.9 Reference voltage and band gap

The 1.237V (typ) internal band gap voltage is accurate to ±1% over the temperature range. It is externally available (VREF pin), and can supply up to ±100μA. It can also be used as a voltage threshold for the multifunction pins FSEL, SKIP, and LDO3\_SEL to select the appropriate working mode. Bypass VREF to ground with a 100nF minimum capacitor.

If  $V_{REF}$  goes below 0.87V (typ), the system detects a fault condition and all of the circuitry is turned off. A toggle on the input voltage (power-on reset) or a toggle on the SHDN pin is required to restart the device.

An internal band gap divider provides a voltage reference  $V_R$  of 0.9V. This voltage is used as a reference for the linear and the switching regulator outputs. The overvoltage protection, the undervoltage protection, and power good signals are referenced to  $V_R$ .

## 7.10 Internal linear regulators

The PM6685 has two linear regulators providing 5V (LDO5) and 3.3V (LDO3), respectively, at 2% accuracy. High side drivers, low side drivers, and most of internal circuitry are supplied by the LDO5 output through the  $V_{CC}$  pin (an external RC filter may be applied between LDO5 and  $V_{CC}$ ). Both linear regulators can provide an average output current of 50mA, and a peak output current of 100mA.

Bypass both LDO5 and LDO3 outputs with a minimum 1 $\mu$ F ceramic capacitor and a 4.7 $\mu$ F tantalum capacitor (ESR 2 $\Omega$ ). If the 5V output goes below 4V, the system detects a fault condition and all of the circuitry is turned off. A power-on reset or a toggle on the SHDN pin is required to restart the device.

The V5SW pin allows users to keep the 5V linear regulator "always active" or to enable the internal bootstrap-switchover function. If the 5V switching output is connected to V5SW when the voltage on the V5SW pin is above 4.8V, an internal 3.0 $\Omega$  (max) p-channel MOSFET switch connects the V5SW pin to the LDO5 pin, and LDO5 shuts down simultaneously. This configuration achieves higher efficiency.

V5SW can also be connected to an external 5V supply. The LDO5 regulator turns off and LDO5 is supplied externally. If V5SW is connected to ground, the internal 5V regulator is always ON and supplies LDO5 output.

**Table 7. V5SW multifunction pin**

V5SW	Description
GND	The 5V linear regulator is always turned on and supplies LDO5 output.
Switching 5V output	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the switching 5V output.
External 5V supply	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the external 5V.

The 3.3V linear regulator is supplied by the LDO5 output. The LDO3\_SEL pin allows users to keep 3.3V linear regulator "always enabled", "always disabled", or to enable the internal bootstrap-switchover function.

According to [Table 8](#):

- If LDO3\_SEL is connected to  $V_{REF}$  pin when the power good signal of the 3.3V switching output voltage (PGOOD3) is high, the internal linear regulator is turned off

and the LDO3 output is connected directly to the OUT3 pin through an internal 3Ω (max) p-channel MOSFET switch.

- If LDO3\_SEL is connected to 5V, the internal 3.3V regulator is always ON and supplies LDO3 output.
- If LDO3\_SEL is connected to ground, the internal 3.3V regulator is always OFF and LDO3 output is clamped to ground.

**Table 8. LDO3\_SEL multifunction pin**

LDO3_SEL	Description
GND	The 3.3V linear regulator is always turned OFF.
VREF	The 3.3V linear regulator is turned OFF when PGOOD3 is high. LDO3 output is supplied by the switching 3.3V output.
LDO5	The 3.3V linear regulator is always turned ON and supplies LDO3 output.

### 7.11 Power-up sequencing and operative modes

When the SHDN, EN5, and EN3 pins are low in the beginning, the battery voltage is applied as input voltage, and the device goes into Shutdown mode.

When the SHDN pin voltage is above the shutdown device ON threshold (1.5V typ), the controller begins the power-up sequence. All of the latched faults are cleared. LDO5 undervoltage control is blanked for 4ms, and the internal regulator LDO5 turns ON. If the LDO5 output is above the UVLO threshold after this time, the device enters into Standby mode. The switching outputs are kept grounded by turning on the low side MOSFETs. When the EN5 and EN3 pins are forced high, the switching sections begin their soft start sequence.

LDO3 management is independent from the general power-up sequence and depends only on the LDO3\_SEL pin.

**Table 9. Operatives modes**

<b>Mode</b>	<b>Conditions</b>	<b>Description</b>
Run	SHDN is high, EN3/EN5 pins are high	Switching and internal linear regulator outputs are enabled.
Standby	Both EN5/EN3 pins are low and SHDN pin is high	Internal Linear regulators active (LDO5 is always ON while LDO3 depends on the LDO3_SEL pin). In Standby mode, the LGATE5/LGATE3 pins are forced high while the HGATE5/HGATE3 pins are forced low.
Shutdown	SHDN is low	All circuits OFF.

## 8 Monitoring and protections

### 8.1 Power good signals

The PM6685 provides three independent power good signals, one for each switching section (PGOOD5/PGOOD3), and the other for the internal linear regulator LDO3 (PGOOD\_LDO3).

The PGOOD5/PGOOD3 signals are low if the output voltage is out of  $\pm 10\%$  of the designed set point, or during the Soft-start, Standby and Shutdown modes. The PGOOD\_LDO3 signal is low when the output voltage of LDO3 output is lower than its falling voltage threshold (2.6V, typ). Each power good pin is an open-drain output and can sink current up to 4mA.

### 8.2 Thermal protection

The PM6685 provides thermal protection to keep the device from overheating. The thermal shutdown occurs when the die temperature goes above  $+150^{\circ}\text{C}$ . In this case, all internal circuitry and power sections are turned off after the discharge mode. A power-on reset or a toggle on the SHDN pin is required to restart the device.

### 8.3 Overvoltage protection

When the switching output voltage is about 115% of its nominal value, latched overvoltage protection occurs. In this case, the synchronous rectifier immediately turns on while the high side MOSFET turns off. The output capacitor is rapidly discharged and the load is preserved from being damaged. The overvoltage protection is also active during soft-start. Once an overvoltage protection has been detected, a toggle on the SHDN, EN3/EN5 pins or a power-on reset is required to exit from the latched state.

### 8.4 Undervoltage protection

When the switching output voltage is below 70% of its nominal value, latched undervoltage protection occurs. In this case, the switching section is immediately disabled and both switches are opened. The controller enters into Soft End mode, and the output is eventually grounded, turning the low side MOSFET ON. The undervoltage circuit protection is enabled only at the end of the soft-start. Once an undervoltage protection has been detected, a toggle on the SHDN, EN5/EN3 pin or a power-on reset is required to clear the undervoltage fault and starts with a new soft-start phase.

**Table 10. Protections and operatives modes**

Mode	Conditions	Description
Overvoltage protection	OUT5/OUT3 > 115% of the nominal value	The LGATE5/LGATE3 pin is forced high, and LDO5 remains active. Exit by a power-on reset, or by toggling SHDN or EN5/EN3.

**Table 10. Protections and operatives modes**

Undervoltage protection	OUT5/OUT3 < 70% of the nominal value	LGATE5/LGATE3 is forced high after the Soft End mode, and LDO5 remains active. Exit by a power-on reset, or toggling SHDN or EN5/EN3.
Thermal shutdown	$T_J > +150^\circ\text{C}$	All circuitry off. Exit by a POR on <i>VIN</i> or toggling <i>SHDN</i> .

## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Table 11. VFQFPN 5x5x1.0 32L Pitch 0.50**

Dim.	Databook (mm)		
	Min	Typ	Max
A	0.8	0.9	1
A1	0	0.02	0.05
A3		0.2	
b	0.18	0.25	0.3
D	4.85	5	5.15
D2	See exposed pad variations <sup>(2)</sup>		
E	4.85	5	5.15
E2	See exposed pad variations <sup>(2)</sup>		
e		0.5	
L	0.3	0.4	0.5
ddd			0.05

**Table 12. Exposed pad variations**

D2			E2		
Min	Typ	Max	Min	Typ	Max
2.90	3.10	3.20	2.90	3.10	3.20

- VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A = 1.00mm Max.
- Dimensions D2 & E2 are not in accordance with JEDEC.



## 10 Revision history

**Table 13. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
17-Jan-2006	1	Initial release
21-Apr-2006	2	Few updates
03-May-2006	3	Graphical updates
29-Jun-2006	4	Mechanical data updated
11-Sep-2006	5	Changes electrical characteristics, added COMP value skip mode, pin out updated
24-Oct-2006	6	Order code table updated

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