

FEATURES

Latch-up immune under all circumstances
 Human body model (HBM) ESD rating: 8 kV
 Low on resistance: 6.5 Ω
 ± 9 V to ± 22 V dual-supply operation
 9 V to 40 V single-supply operation
 48 V supply maximum ratings
 Fully specified at ± 15 V, ± 20 V, $+12$ V, and $+36$ V
 V_{DD} to V_{SS} analog signal range

APPLICATIONS

High voltage signal routing
 Automatic test equipment
 Analog front-end circuits
 Precision data acquisition
 Amplifier gain select
 Industrial instrumentation
 Relay replacement

GENERAL DESCRIPTION

The **ADG5401** is a monolithic industrial, complementary metal oxide semiconductor (CMOS) analog switch containing a latch-up immune single-pole/single-throw (SPST) switch. The switch conducts equally well in both directions when on, and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical. The latch-up immune construction and high ESD rating make these switches more robust in harsh environments.

FUNCTIONAL BLOCK DIAGRAM

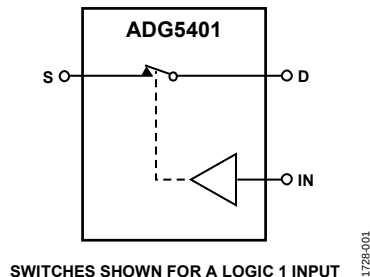


Figure 1.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P channel and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} of 6.5 Ω .
3. Dual-supply operation. For applications where the analog signal is bipolar, the **ADG5401** can operate from dual supplies of up to ± 22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the **ADG5401** can operate from a single-rail power supply of up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_I logic power supply required.
7. Available in 8-lead MSOP package.

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REVISION HISTORY

9/13—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	6.5 8	10	12	Ω typ Ω max	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 19 $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Flatness, $R_{FLAT(ON)}$	1 1.4	1.7	2	Ω typ Ω max	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
Source Off Leakage, I_S (Off)	± 0.1 ± 0.5	± 2	± 20	nA typ nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 18
Drain Off Leakage, I_D (Off)	± 0.1 ± 0.5	± 2	± 20	nA typ nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 18
Channel On Leakage, I_D (On), I_S (On)	± 0.2 ± 1	± 8	± 40	nA typ nA max	$V_S = V_D = \pm 10\text{ V}$; see Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t_{ON}	160 193	230	253	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 24
t_{OFF}	175 207	230	242	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 24
Charge Injection, Q_{INU}	220			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 25
Off Isolation	−50			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 20
Total Harmonic Distortion + Noise (THD + N)	0.01			% typ	$R_L = 1\text{ k}\Omega$, 15 V p-p , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 22
−3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 23
Insertion Loss	−0.4			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23
C_S (Off)	22			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	24			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	75			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	45 55		70	μA typ μA max	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001		1	μA typ μA max	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	$GND = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance, R _{ON}	6			Ω typ	V _S = ±15 V, I _S = −10 mA; see Figure 19
On-Resistance Flatness, R _{FLAT(ON)}	7	9	11	Ω max	V _{DD} = +18 V, V _{SS} = −18 V
	1.2			Ω typ	V _S = ±15 V, I _S = −10 mA
	1.7	2.1	2.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.1			nA typ	V _{DD} = +22 V, V _{SS} = −22 V
Drain Off Leakage, I _D (Off)	±0.5 ±0.1	±2	±20	nA max nA typ	V _S = ±15 V, V _D = ∓ 15 V; see Figure 18
Channel On Leakage, I _D (On), I _S (On)	±0.5 ±0.2 ±1	±2 ±8	±20 ±40	nA max nA typ nA max	V _S = V _D = ±15 V; see Figure 21
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ μA max	V _{IN} = V _{GND} or V _{DD}
Digital Input Capacitance, C _{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t _{ON}	150 175	207	219	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V; see Figure 24
t _{OFF}	170 196	214	223	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V; see Figure 24
Charge Injection, Q _{INJ}	275			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 25
Off Isolation	−50			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 20
Total Harmonic Distortion + Noise (THD + N)	0.01			% typ	R _L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 22
−3 dB Bandwidth	170			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 23
Insertion Loss	−0.5			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 23
C _S (Off)	21			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	23			pF typ	V _S = 0 V, f = 1 MHz
C _D (On), C _S (On)	75			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	50 70		110	μA typ μA max	V _{DD} = +22 V, V _{SS} = −22 V Digital inputs = 0 V or V _{DD}
I _{SS}	0.001		1	μA typ μA max	Digital inputs = 0 V or V _{DD}
V _{DD} /V _{SS}			±9/±22	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	V _S = 0 V to 10 V, I _S = −10 mA; see Figure 19 V _{DD} = 10.8 V, V _{SS} = 0 V V _S = 0 V to 10 V, I _S = −10 mA
On Resistance, R _{ON}	14			Ω typ	
On-Resistance Flatness, R _{FLAT (ON)}	16	19	22	Ω max	
	2.8			Ω typ	
	4	5.5	7	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.1			nA typ	V _{DD} = +13.2 V, V _{SS} = 0 V V _S = 1 V to 10 V, V _D = 10 V to 1 V; see Figure 18
Drain Off Leakage, I _D (Off)	±0.5 ±0.1	±2	±20	nA max nA typ	V _S = 1 V to 10 V, V _D = 10 V to 1 V; see Figure 18
Channel On Leakage, I _D (On), I _S (On)	±0.5 ±0.2	±2	±20	nA max nA typ	
	±1	±8	±40	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ μA max	
Digital Input Capacitance, C _{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t _{ON}	260 327	406	454	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 24
t _{OFF}	200 244	280	300	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 24
Charge Injection, Q _{INJ}	95			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF; see Figure 25
Off Isolation	−50			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 20
Total Harmonic Distortion + Noise (THD + N)	0.02			% typ	R _L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 22
−3 dB Bandwidth	190			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 23
Insertion Loss	−0.9			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 23
C _S (Off)	28			pF typ	V _S = 6 V, f = 1 MHz
C _D (Off)	30			pF typ	V _S = 6 V, f = 1 MHz
C _D (On), C _S (On)	60			pF typ	V _S = 6 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	40 50		65	μA typ μA max	V _{DD} = 13.2 V Digital inputs = 0 V or V _{DD}
V _{DD}			9/40	V min/V max	GND = 0 V, V _{SS} = 0 V

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	V _S = 0 V to 30 V, I _S = −10 mA; see Figure 19 V _{DD} = 32.4 V, V _{SS} = 0 V V _S = 0 V to 30 V, I _S = −10 mA
On Resistance, R _{ON}	7			Ω typ	
On-Resistance Flatness, R _{FLAT (ON)}	9	11	13	Ω max	
	1.8			Ω typ	
	2.6	3	3.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.1			nA typ	V _{DD} = +39.6 V, V _{SS} = 0 V V _S = 1 V to 30 V, V _D = 30 V to 1 V; see Figure 18
Drain Off Leakage, I _D (Off)	±0.5	±2	±20	nA max	V _S = 1 V to 30 V, V _D = 30 V to 1 V; see Figure 18
	±0.1			nA typ	
Channel On Leakage, I _D (On), I _S (On)	±0.5	±2	±20	nA max	V _S = V _D = 1 V to 30 V; see Figure 21
	±0.2			nA typ	
	±1	±8	±40	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ	
				μA max	
Digital Input Capacitance, C _{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t _{ON}	160	212	230	ns typ	R _L = 300 Ω, C _L = 35 pF
	187			ns max	V _S = 18 V; see Figure 24
t _{OFF}	180			ns typ	R _L = 300 Ω, C _L = 35 pF
	213	221	225	ns max	V _S = 18 V; see Figure 24
Charge Injection, Q _{INJ}	255			pC typ	V _S = 18 V, R _S = 0 Ω, C _L = 1 nF; see Figure 25
Off Isolation	−50			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 20
Total Harmonic Distortion + Noise (THD + N)	0.01			% typ	R _L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 22
−3 dB Bandwidth	170			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 23
Insertion Loss	−0.55			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 23
C _S (Off)	26			pF typ	V _S = 18 V, f = 1 MHz
C _D (Off)	28			pF typ	V _S = 18 V, f = 1 MHz
C _D (On), C _S (On)	65			pF typ	V _S = 18 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	80			μA typ	V _{DD} = 39.6 V
	100		130	μA max	Digital inputs = 0 V or V _{DD}
V _{DD}			9/40	V min/V max	GND = 0 V, V _{SS} = 0 V

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Condition/Comments
CONTINUOUS CURRENT, S OR D					MSOP ($\theta_{JA} = 133.1^{\circ}\text{C/W}$)
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	171	116	79	mA maximum	
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	177	120.5	81	mA maximum	
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	139	99	70	mA maximum	
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	174	118	81	mA maximum	

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	–0.3 V to +48 V
V_{SS} to GND	+0.3 V to –48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D Pin	630 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D ²	Data + 15%
Temperature Range	
Operating	–40°C to +125°C
Storage	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
8-Lead MSOP (4-Layer Board)	133.1°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
Human Body Model (HBM) ESD	8 kV

¹ Overvoltages at the IN, S, and D pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

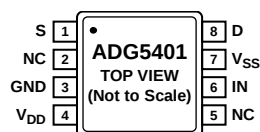
Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT. NOT INTERNALLY CONNECTED.

11728-002

Figure 2. Pin Configuration

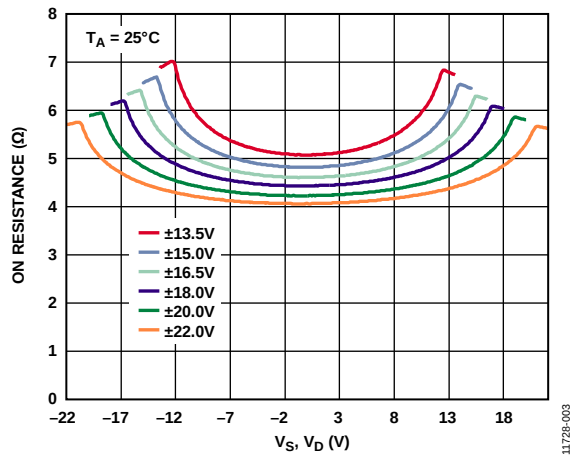
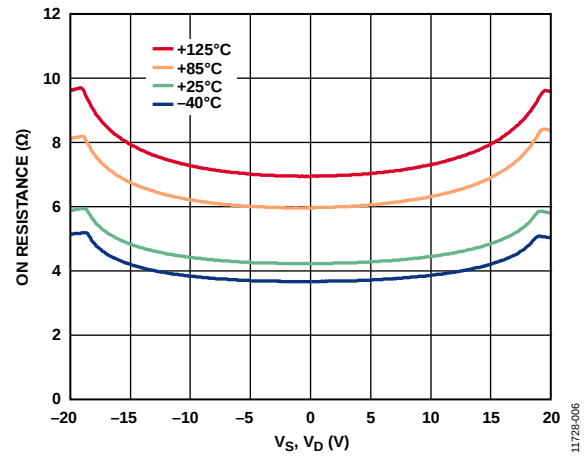
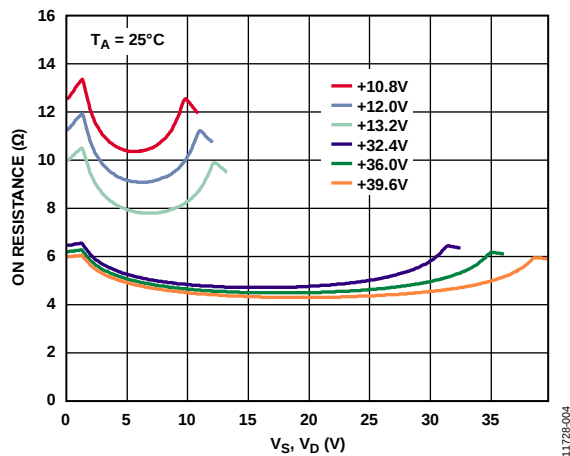
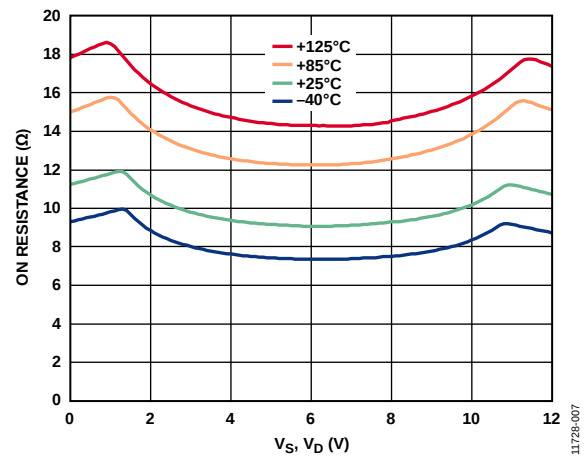
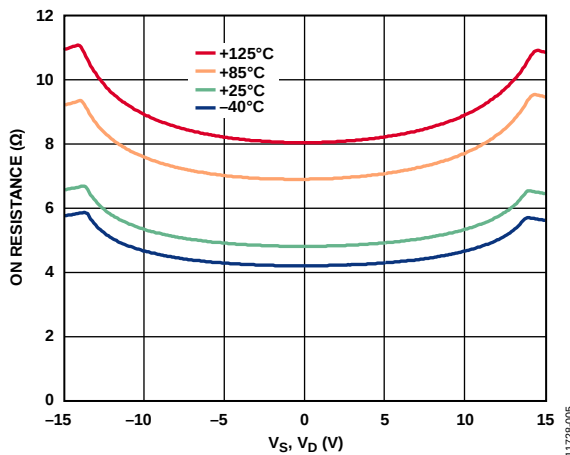
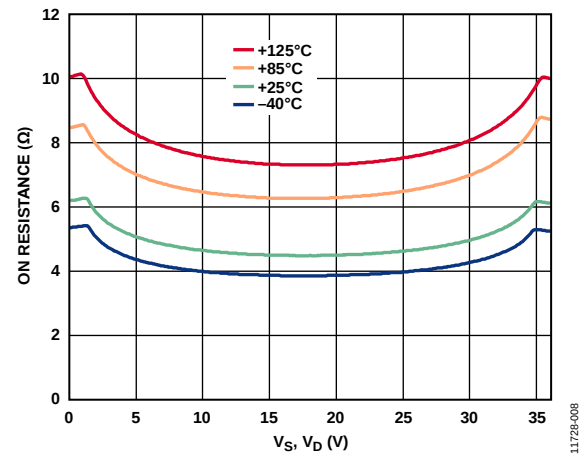
Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S	Source Terminal. This pin can be an input or output.
2	NC	No Connect. Not internally connected.
3	GND	Ground (0 V) Reference.
4	V _{DD}	Most Positive Power Supply Potential.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V _{SS}	Most Negative Power Supply Potential.
8	D	Drain Terminal. This pin can be an input or output.

Table 8. Truth Table

IN	Switch Condition
1	On
0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. On Resistance as a Function of V_S , V_D (Dual Supply)Figure 6. On Resistance as a Function of V_S , V_D for Different Temperatures, ± 20 V Dual SupplyFigure 4. On Resistance as a Function of V_S , V_D (Single Supply)Figure 7. On Resistance as a Function of V_S , V_D for Different Temperatures, 12 V Single SupplyFigure 5. On Resistance as a Function of V_S , V_D for Different Temperatures, ± 15 V Dual SupplyFigure 8. On Resistance as a Function of V_S , V_D for Different Temperatures, 36 V Single Supply

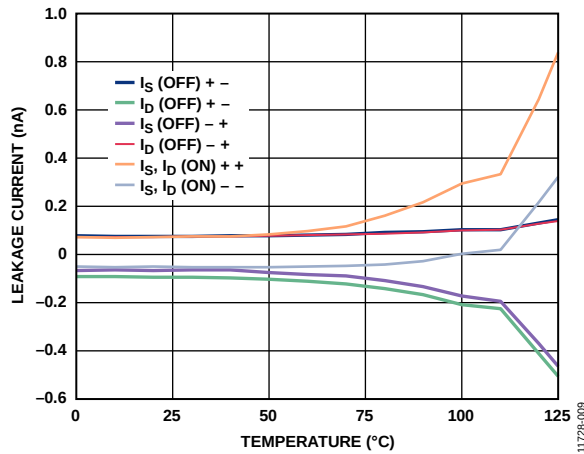
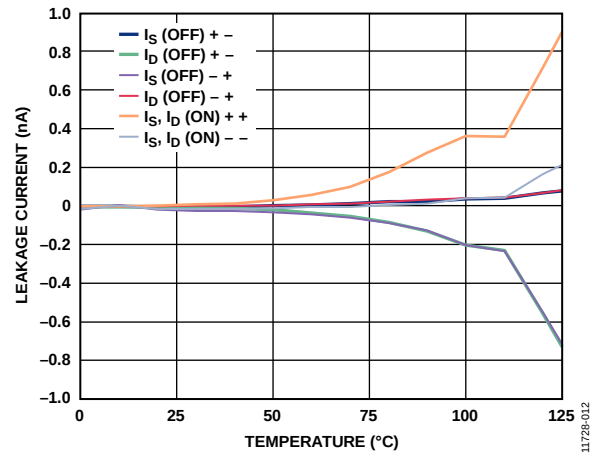
Figure 9. Leakage Currents as a Function of Temperature, ± 15 V Dual Supply

Figure 12. Leakage Currents as a Function of Temperature, 36 V Single Supply

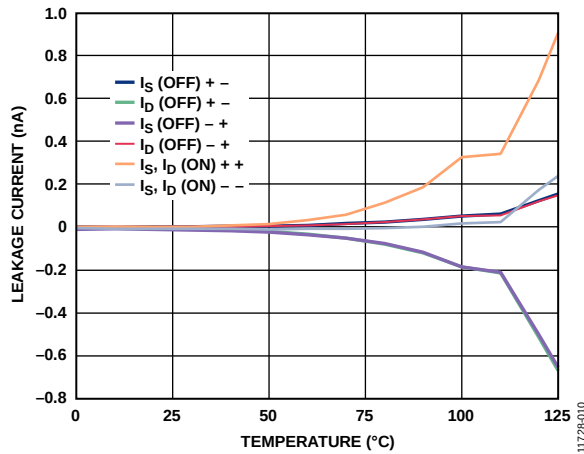
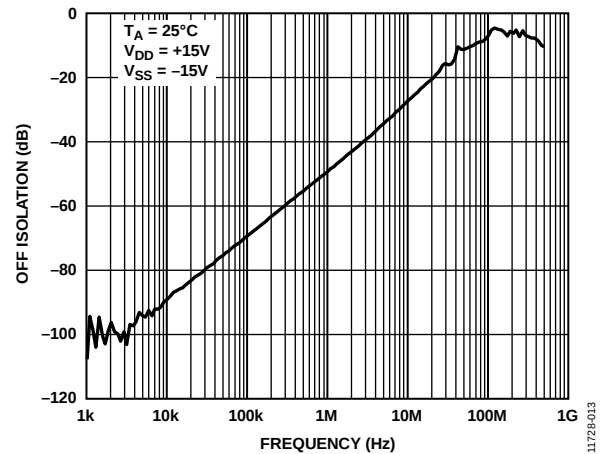
Figure 10. Leakage Currents as a Function of Temperature, ± 20 V Dual Supply

Figure 13. Off Isolation vs. Frequency

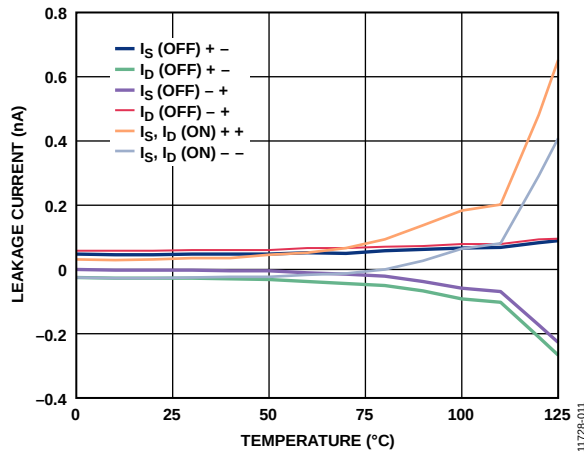
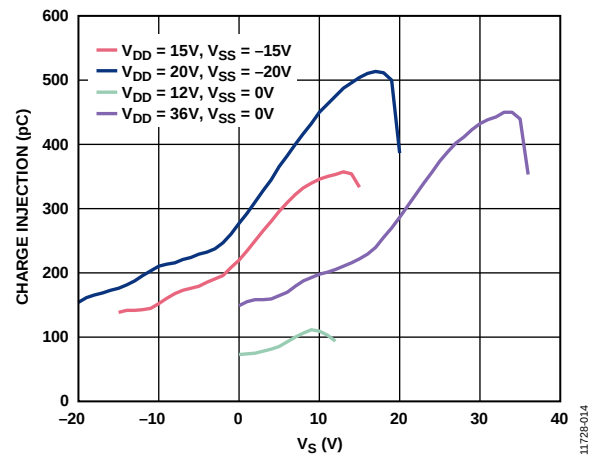


Figure 11. Leakage Currents as a Function of Temperature, 12 V Single Supply

Figure 14. Charge Injection vs. Source Voltage (V_S)

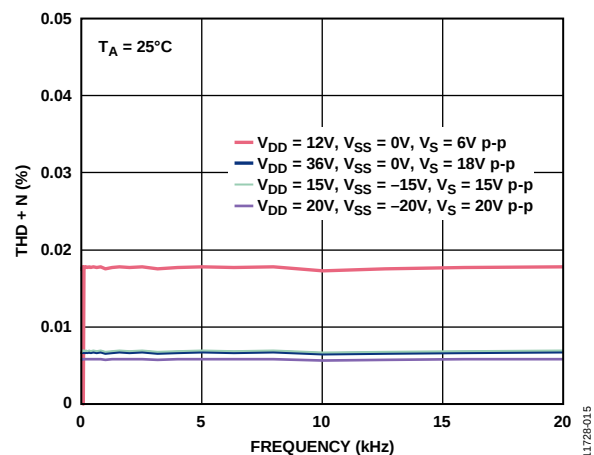


Figure 15. THD + N vs. Frequency

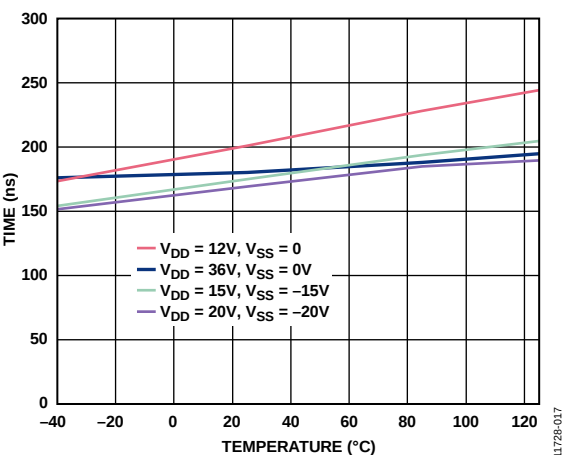


Figure 17. $t_{\text{TRANSITION}}$ Times vs. Temperature

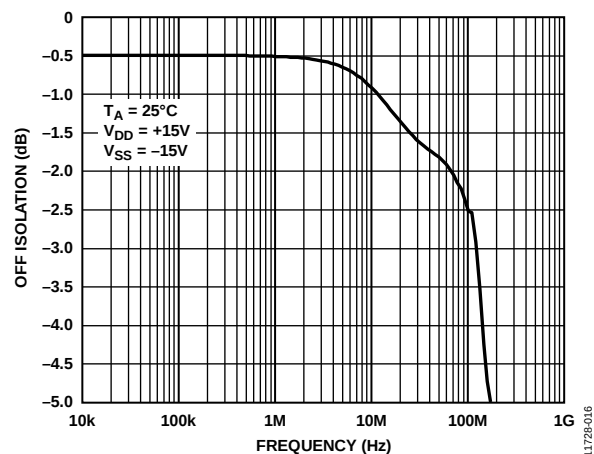


Figure 16. Bandwidth

TEST CIRCUITS

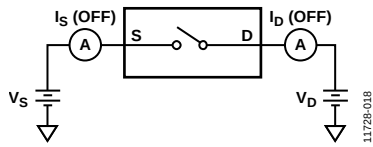


Figure 18. Off Leakage

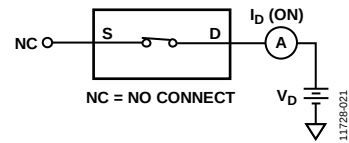


Figure 21. On Leakage

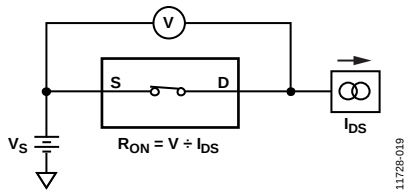


Figure 19. On Resistance

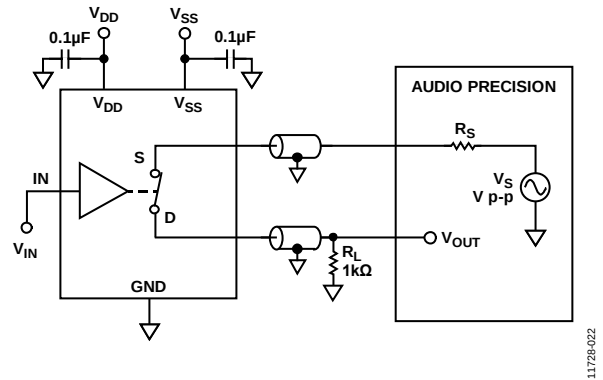


Figure 22. THD + N

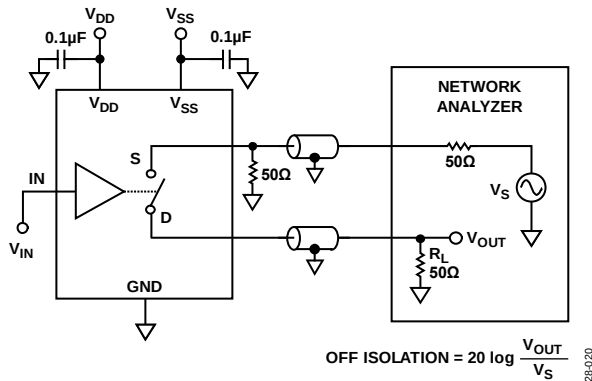


Figure 20. Off Isolation

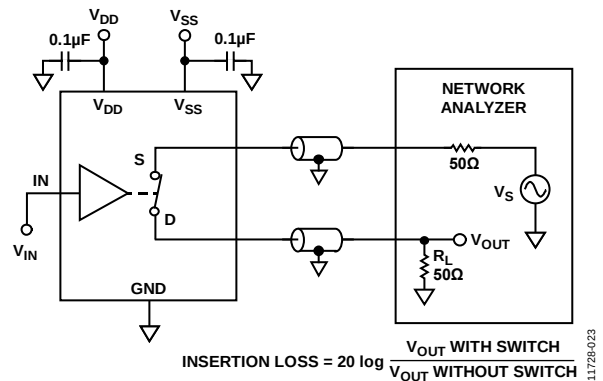
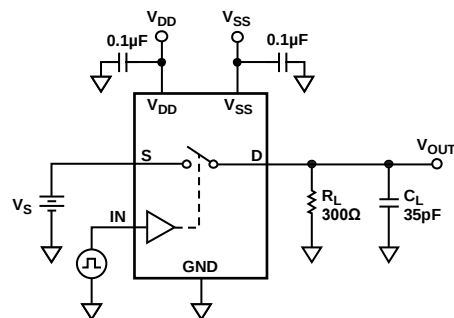
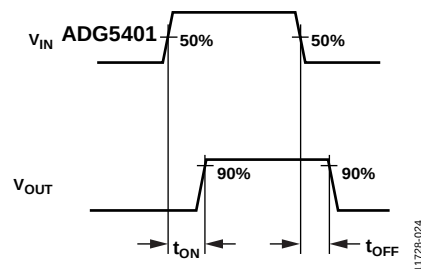


Figure 23. Bandwidth

Figure 24. Switching Times, t_{ON} and t_{OFF} 

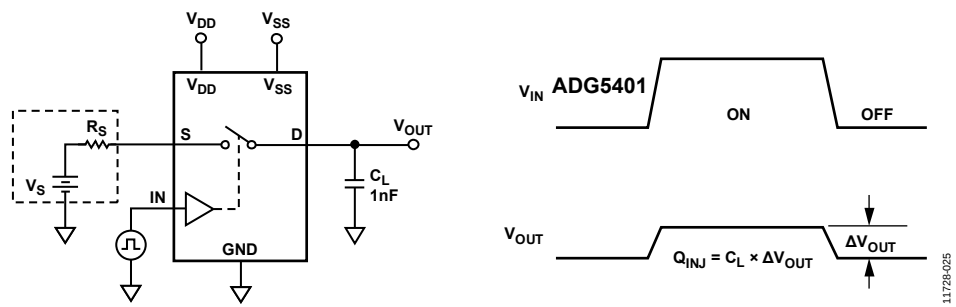


Figure 25. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

R_{FLAT (ON)}

R_{FLAT (ON)} represents the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

t_{ON}

t_{ON} represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

t_{OFF} represents the delay time between the 50% and 90% points of the digital input and switch off condition.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB from its dc value.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

APPLICATIONS INFORMATION

The [ADG54xx](#) family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The [ADG5401](#) high voltage switch allows single-supply operation from 9 V to 40 V and dual-supply operation from ± 9 V to ± 22 V. The [ADG5401](#) (as well as other select devices within this family) achieves an 8 kV human body model ESD rating, which provides a robust solution, eliminating the need for separate protection circuitry designs in some applications.

TRENCH ISOLATION

In the [ADG5401](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a latch-up immune switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. The two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up immune switch.

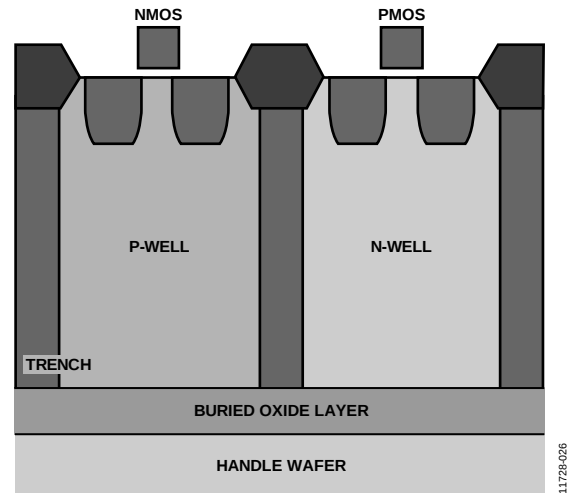
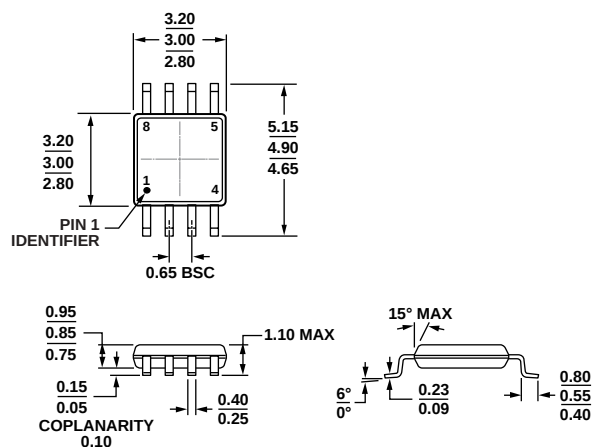


Figure 26. Trench Isolation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 27. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG5401BRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2M
ADG5401BRMZ-RL7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2M

¹ Z = RoHS Compliant Part.

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