

ZXMP2120G4

200V P-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS} = -200V$; $R_{DS(ON)} = 25\Omega$; $I_D = 200mA$

DESCRIPTION

This 200V enhancement mode P-channel MOSFET provides users with a competitive specification offering efficient power handling capability, high impedance and is free from thermal runaway and thermally induced secondary breakdown. Applications benefiting from this device include a variety of telecom and general high voltage circuits.

A SOT23-5 version is also available (ZXMP2120E5).

FEATURES

- High voltage
- Low on-resistance
- Fast switching speed
- Low gate drive
- Low threshold
- SOT223 package variant engineered to increase spacing between high voltage pins.

APPLICATIONS

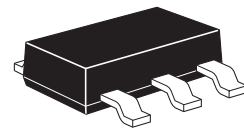
- Active clamping of primary side MOSFETs in 48 volt DC-DC converters

ORDERING INFORMATION

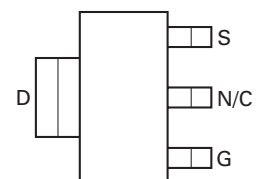
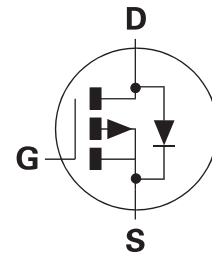
DEVICE	REEL SIZE (inches)	TAPE WIDTH (mm)	QUANTITY PER REEL
ZXMP2120G4TA	7	12mm embossed	1,000 units
ZXMP2120G4TC	13	12mm embossed	4,000 units

DEVICE MARKING

ZXMP
2120



SOT223



Pinout - top view

ZXMP2120G4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-200	V
Gate Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS}=10V$; $T_{amb}=25^{\circ}C$) ^(a)	I_D	-200	mA
Pulsed Drain Current ^(b)	I_{DM}	-1	A
Pulsed Source Current (Body Diode) ^(b)	I_{SM}	-1	A
Power Dissipation at $T_{amb}=25^{\circ}C$ ^(a)	P_{tot}	2.0	W
Linear derating factor		1.6	mW/ $^{\circ}C$
Operating and Storage Temperature Range	$T_j:T_{stg}$	-55 to +150	$^{\circ}C$

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient ^(a)	$R_{\theta JA}$	62.5	$^{\circ}C/W$

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions

(b) Repetitive rating - pulse width limited by maximum junction temperature. Refer to Transient Thermal Impedance graph.

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ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	-200		V	$I_D = -1\text{mA}$, $V_{GS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D = -1\text{mA}$, $V_{DS} = V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		-10 -100	μA μA	$V_{DS} = -200\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = -160\text{V}$, $V_{GS} = 0\text{V}$, $T = 125^{\circ}\text{C}$ ⁽²⁾
On-State Drain Current ⁽¹⁾	$I_{D(on)}$	-300		mA	$V_{DS} = -25\text{V}$, $V_{GS} = -10\text{V}$
Static Drain-Source On-State Resistance ⁽¹⁾	$R_{DS(on)}$		25	Ω	$V_{GS} = -10\text{V}$, $I_D = -150\text{mA}$
Forward Transconductance ⁽¹⁾⁽²⁾	g_{fs}	50		mS	$V_{DS} = -25\text{V}$, $I_D = -150\text{mA}$
Input Capacitance ⁽²⁾	C_{iss}		100	pF	$V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$
Common Source Output Capacitance ⁽²⁾	C_{oss}		25	pF	
Reverse Transfer Capacitance ⁽²⁾	C_{rss}		7	pF	
Turn-On Delay Time ⁽²⁾⁽³⁾	$t_{d(on)}$		7	ns	$V_{DD} = -25\text{V}$, $I_D = -150\text{mA}$
Rise Time ⁽²⁾⁽³⁾	t_r		15	ns	
Turn-Off Delay Time ⁽²⁾⁽³⁾	$t_{d(off)}$		12	ns	
Fall Time ⁽²⁾⁽³⁾	t_f		15	ns	

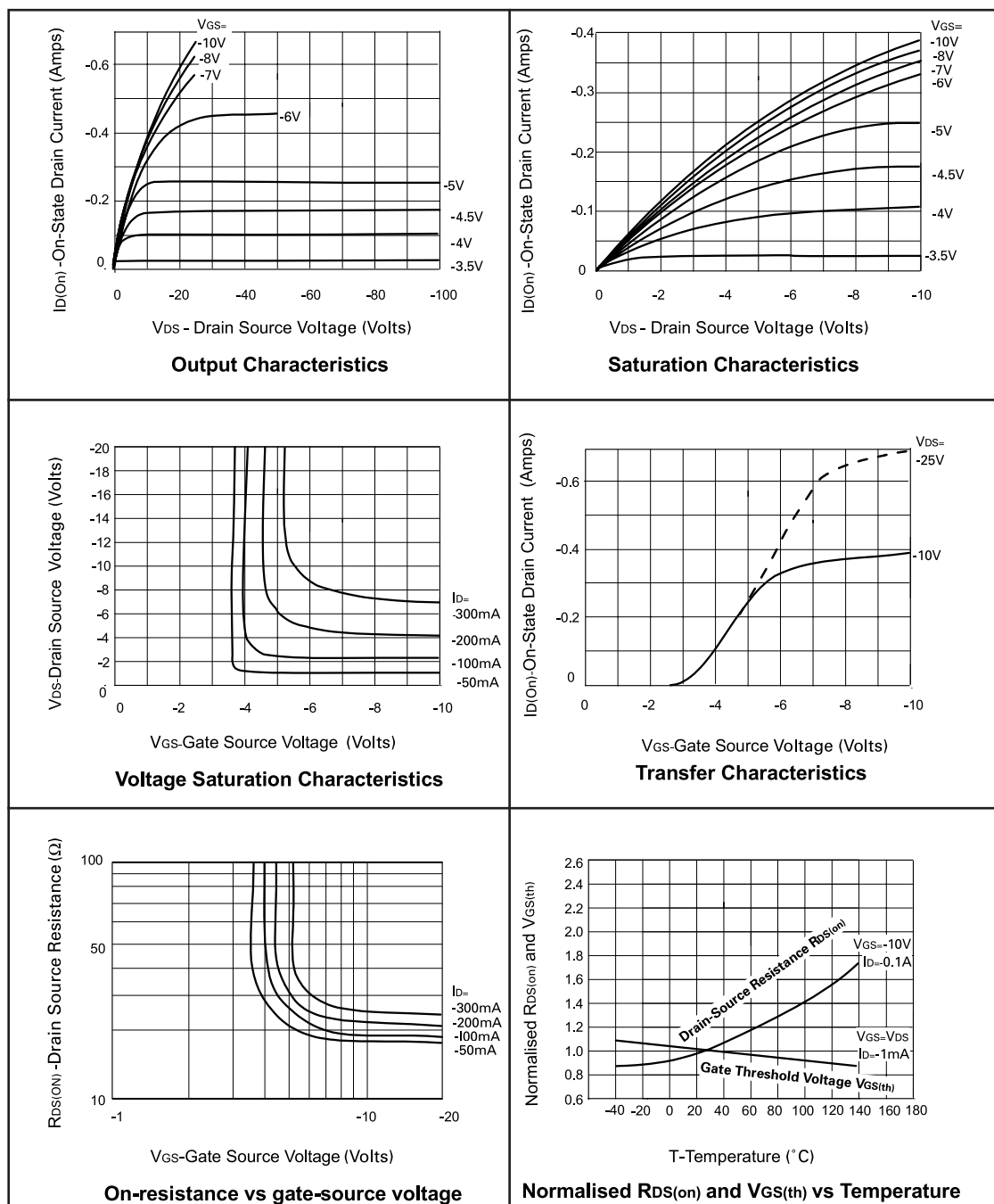
(1) Measured under pulsed conditions. Width=300 μs . Duty cycle @2%

(2) Sample test.

(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator

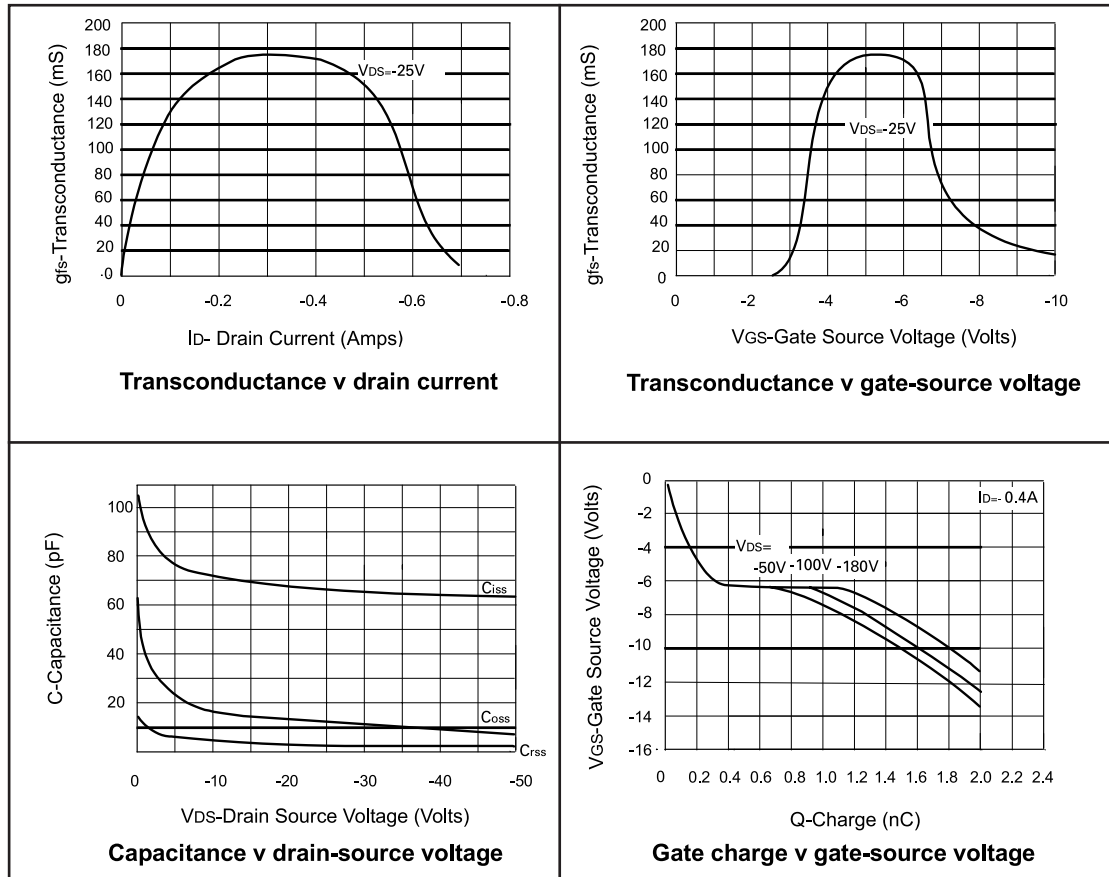
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TYPICAL CHARACTERISTICS



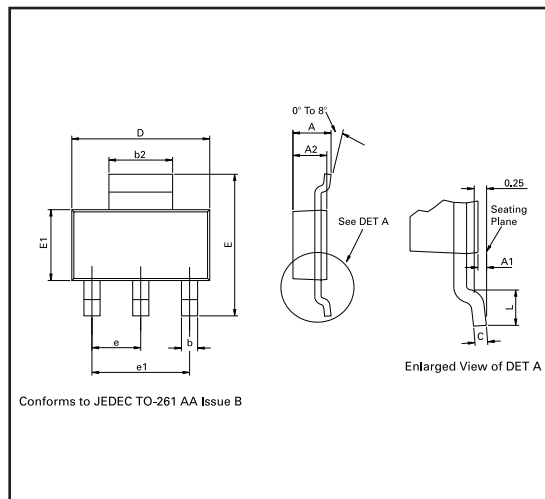
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CHARACTERISTICS

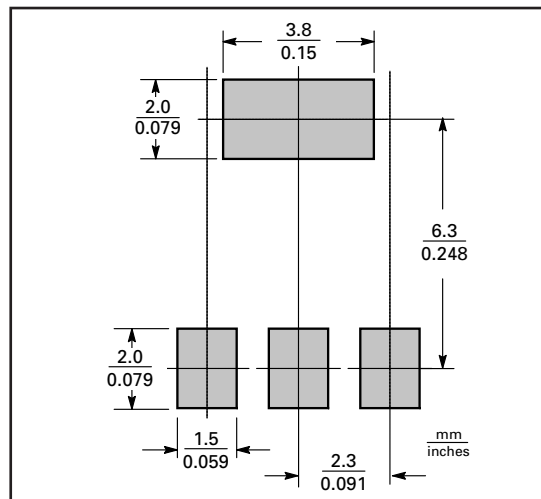


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PACKAGE OUTLINE



PAD LAYOUT DETAILS



Controlling dimensions are in millimeters. Approximate conversions are given in inches

PACKAGE DIMENSIONS

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	-	1.80	-	0.071	e	2.30 BSC		0.0905 BSC	
A1	0.02	0.10	0.0008	0.004	e1	4.60 BSC		0.181 BSC	
b	0.66	0.84	0.026	0.033	E	6.70	7.30	0.264	0.287
b2	2.90	3.10	0.114	0.122	E1	3.30	3.70	0.130	0.146
C	0.23	0.33	0.009	0.013	L	0.90	-	0.355	-
D	6.30	6.70	0.248	0.264	-	-	-	-	-

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Europe	Americas	Asia Pacific	Corporate Headquarters
Zetex GmbH Kustermann-park Balanstraße 59 D-81541 München Germany Telefon: (49) 89 45 49 49 0 Fax: (49) 89 45 49 49 49 europe.sales@zetex.com	Zetex Inc 700 Veterans Memorial Hwy Hauppauge, NY 11788 USA Telephone: (1) 631 360 2222 Fax: (1) 631 360 8222 usa.sales@zetex.com	Zetex (Asia) Ltd 3701-04 Metroplaza Tower 1 Hing Fong Road, Kwai Fong Hong Kong Telephone: (852) 26100 611 Fax: (852) 24250 494 asia.sales@zetex.com	Zetex Semiconductors plc Zetex Technology Park Chadderton, Oldham, OL9 9LL United Kingdom Telephone (44) 161 622 4444 Fax: (44) 161 622 4446 hq@zetex.com

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