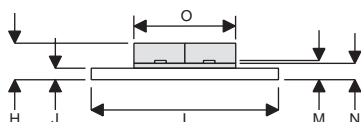
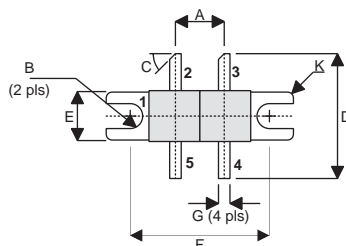


MECHANICAL DATA



DK

PIN 1 SOURCE (COMMON) PIN 2 DRAIN 1
 PIN 3 DRAIN 2 PIN 4 GATE 2
 PIN 5 GATE 1

DIM	mm	Tol.	Inches	Tol.
A	6.45	0.13	0.254	0.005
B	1.65R	0.13	0.065R	0.005
C	45°	5°	45°	5°
D	16.51	0.76	0.650	0.03
E	6.47	0.13	0.255	0.005
F	18.41	0.13	0.725	0.005
G	1.52	0.13	0.060	0.005
H	4.82	0.25	0.190	0.010
I	24.76	0.13	0.975	0.005
J	1.52	0.13	0.060	0.005
K	0.81R	0.13	0.032R	0.005
M	0.13	0.02	0.005	0.001
N	2.16	0.13	0.085	0.005

**GOLD METALLISED
 MULTI-PURPOSE SILICON
 DMOS RF FET
 40W – 28V – 500MHz
 PUSH-PULL**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- USEFUL P_O at 1 GHz
- LOW NOISE
- HIGH GAIN – 13 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
 from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	100W
BV_{DSS}	Drain – Source Breakdown Voltage *	70V
BV_{GSS}	Gate – Source Breakdown Voltage *	$\pm 20V$
$I_{D(sat)}$	Drain Current *	5A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

* Per Side

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PER SIDE					
B _V DSS	Drain–Source Breakdown Voltage V _{GS} = 0 I _D = 100mA	70			V
I _D DSS	Zero Gate Voltage Drain Current V _{DS} = 28V V _{GS} = 0			1	mA
I _G DSS	Gate Leakage Current V _{GS} = 20V V _{DS} = 0			1	μA
V _{GS(th)}	Gate Threshold Voltage * I _D = 10mA V _{DS} = V _{GS}	1		7	V
g _{fs}	Forward Transconductance * V _{DS} = 10V I _D = 1A	0.8			S
TOTAL DEVICE					
G _{PS}	Common Source Power Gain P _O = 40W	13			dB
η	Drain Efficiency V _{DS} = 28V I _{DQ} = 0.4A	50			%
VSWR	Load Mismatch Tolerance f = 400MHz	20:1			—
PER SIDE					
C _{iss}	Input Capacitance V _{DS} = 28V V _{GS} = -5V f = 1MHz			60	pF
C _{oss}	Output Capacitance V _{DS} = 28V V _{GS} = 0 f = 1MHz			30	pF
C _{rss}	Reverse Transfer Capacitance V _{DS} = 28V V _{GS} = 0 f = 1MHz			2.5	pF
R _{dson}	Saturation Resistance V _{GS} = 20V I _{DS} = 2.5A		1		Ω

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 1.75°C / W
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Semelab plc. Telephone +44(0)1455 556565. Fax +44(0)1455 552612.

E-mail: sales@semelab.co.uk Website: <http://www.semelab.co.uk>

Document Number 6219

Issue 1

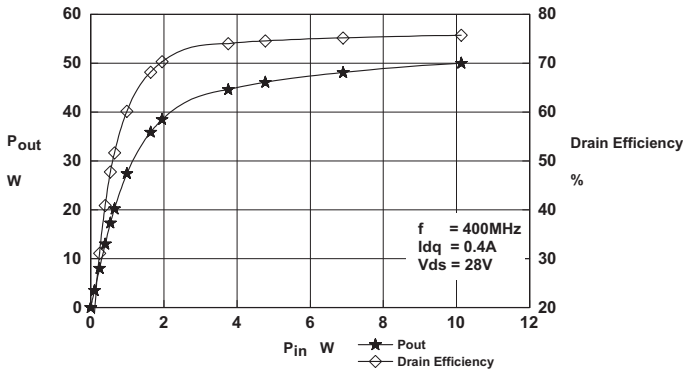


Figure 1

Power Output and efficiency vs. Power Input.

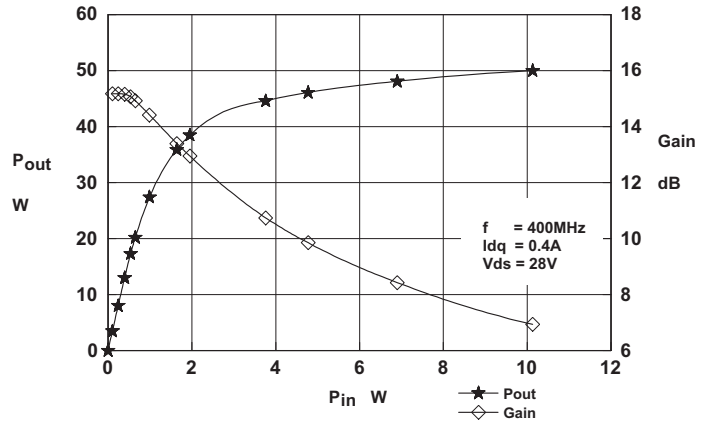


Figure 2

Power Output and Gain vs. Power Input.

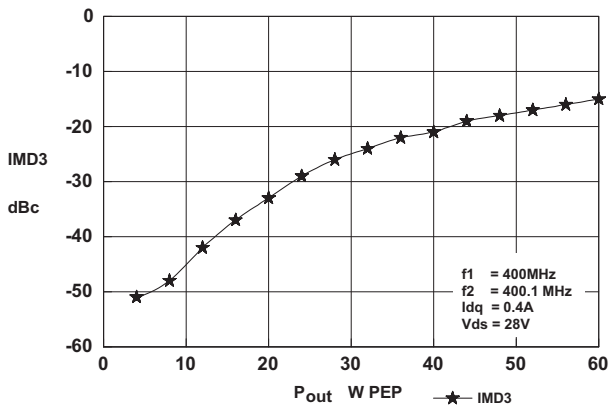


Figure 3

IMD Vs. Output Power.

OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z _S Ω	Z _L Ω
400MHZ	10.7 - j35.4	13.8 - j22.2

Typical S Parameters

! V_{DS} = 28V, I_{DQ} = 1A
MHZ S MA R 50

!Freq !MHz	S11 mag ang	S21 mag ang	S12 mag ang	S22 mag ang
100	0.767 -135	22.646 88	0.0155 9	0.531 -103
200	0.813 -153	10.116 57	0.0099 4	0.692 -131
300	0.841 -161	5.623 39	0.0076 49	0.794 -143
400	0.861 -169	3.548 25	0.013 79	0.841 -151
500	0.882 -175	2.82 20	0.021 78	0.875 -156
600	0.902 180	2.093 14	0.0285 78	0.91 -161
700	0.923 174	1.365 9	0.0376 77	0.944 -166
800	0.912 170	1.096 2	0.0457 66	0.944 -170
900	0.923 164	0.902 -3	0.0484 66	0.933 -176
1000	0.923 161	0.724 -4	0.0596 64	0.944 -177

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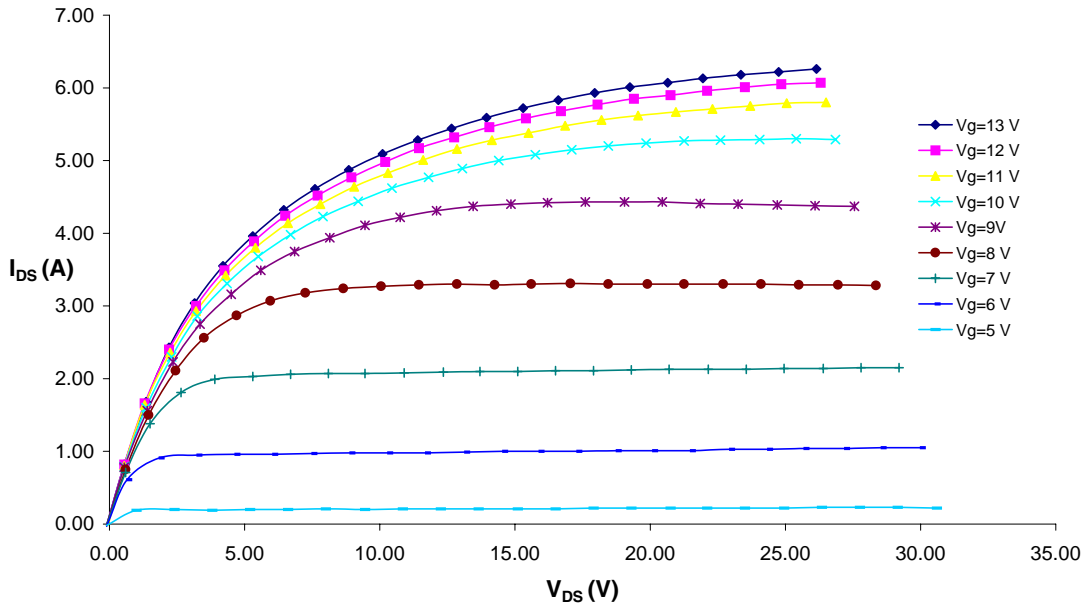


Figure 4 – Typical IV Characteristics.

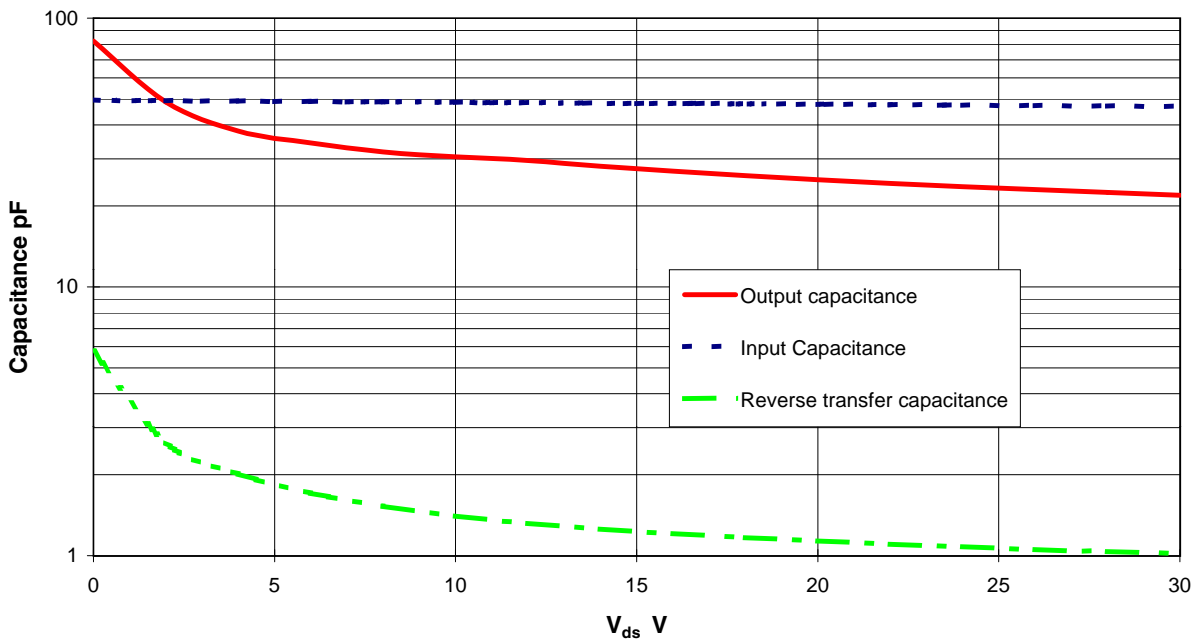
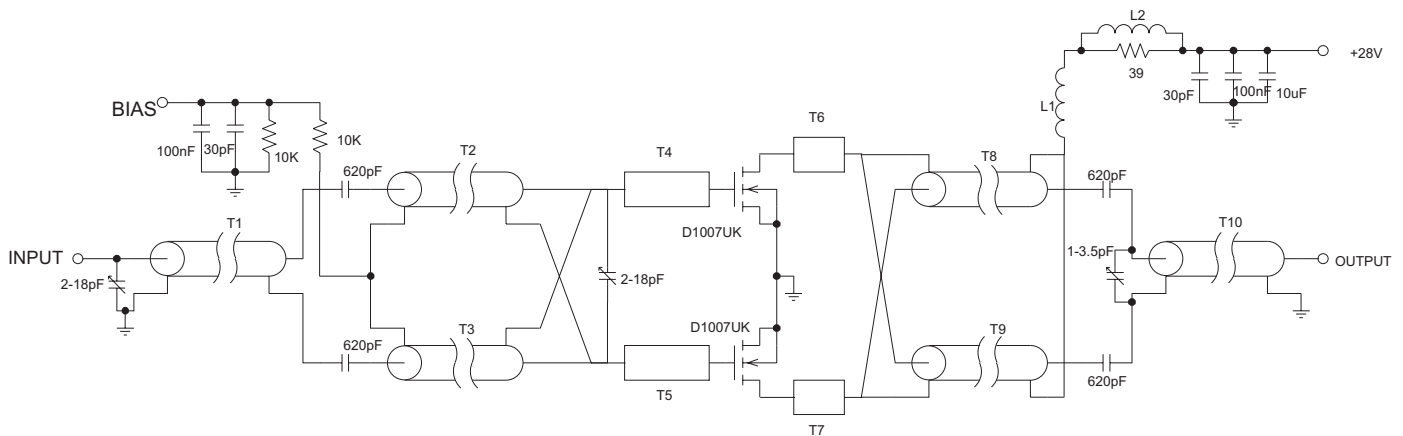


Figure 5 – Typical CV Characteristics.

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D1007UK TEST FIXTURE

Substrate 1.6mm FR4
 All microstrip lines $W = 2.5\text{mm}$

T1	45mm 50 OHM UT34 semi-rigid coax
T2, T3	55mm 50 OHM UT 34 semi-rigid coax
T4, T5	25mm microstrip line
T6, T7	10mm microstrip line
T8, T9	45mm 25 OHM UT 34-25 semi-rigid coax
T10	60mm 50OHM UT34 semi-rigid coax
L1	4 turns 19swg enamelled copper wire, 7mm i.d.
L2	2.5 turns of 19swg enamelled copper wire on T50-6 ferrite toroid