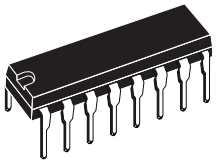
80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

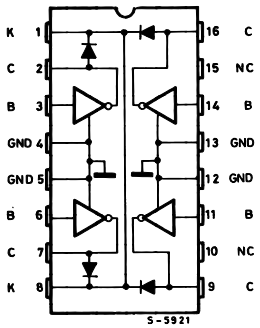


POWERDIP
12 + 2 + 2

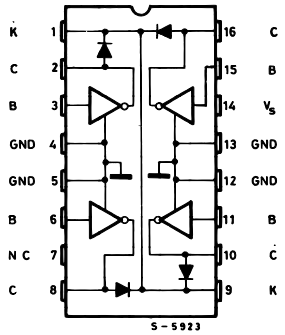
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

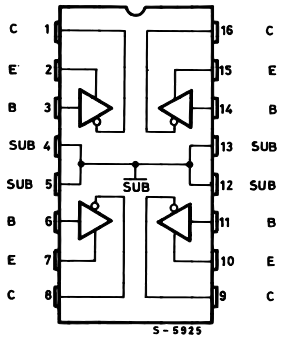
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



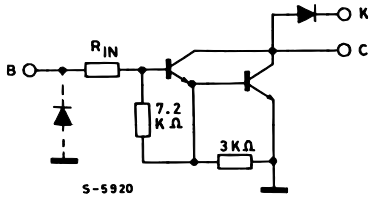
ULN2069B
ULN2071B



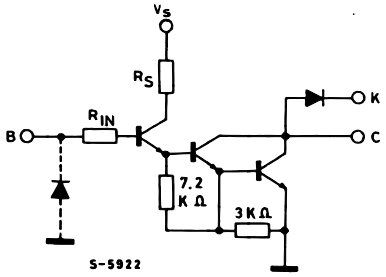
ULN2075B
ULN2077B

SCHEMATIC DIAGRAM

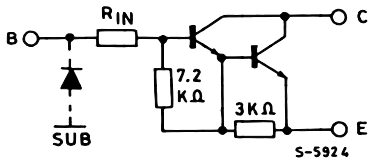
ULN2065B : R_{IN} = 350Ω
ULN2067B : R_{IN} = 3kΩ



ULN2069B : R_{IN} = 2.5kΩ, R_S = 900Ω
ULN2071B : R_{IN} = 11.6kΩ, R_S = 3.4kΩ



ULN2075B : R_{IN} = 350Ω
ULN2077B : R_{IN} = 3kΩ



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CEX}	Output Voltage		80	V
$V_{CE(sus)}$	Output Sustaining Voltage		50	V
I_O	Output Current		1.75	A
V_i	Input Voltage	for ULN2075B – 2077B for ULN2067B – 2071B for ULN2065B – 2069B	60 30 15	V V V
I_I	Input Current		25	mA
V_S	Supply Voltage	for ULN2069B for ULN2071B	10 20	V V
P_{tot}	Power Dissipation	at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range		– 20 to 85	°C
T_{stg}	Storage Temperature		– 55 to 150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 80V T_{amb} = 25°C T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	I_C = 100mA, V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA I_C = 1.5A I_B = 2.25mA			1.1 1.2 1.3 1.4 1.5	V V V V V	3 3 3 3 3
$I_{i(on)}$	Input Current	for ULN2065B and ULN2075B V_i = 2.4V V_i = 3.75V for ULN2067B and ULN2077B V_i = 5V V_i = 12V for ULN2069B V_i = 2.75V V_i = 3.75V for ULN2071B V_i = 5V V_i = 12V	 1.4 3.3 0.6 1.7 		 4.3 9.6 1.8 5.2 5.5 10 4 12.5	 mA mA mA mA mA mA mA mA	 4 4 4 4 4 4 4 4

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{i(on)}$	Input Voltage	V_{CE} = 2V, I_C = 1A ULN2065B, ULN2075B ULN2067B, ULN2077B V_{CE} = 2V, I_C = 1.5A ULN2065B, ULN2075B ULN2067B, ULN2077B ULN2069B ULN2071B			 2 6.5 2.5 10 2.75 5	 V V V V V V	 5 5 5 5 5 5
I_S	Supply Current	for ULN2069B I_C = 500mA, V_i = 2.75V for ULN2071B I_C = 500mA, V_i = 5V			 6 4.5	 mA mA	 8 8
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for ULN2065B-ULN2067B and ULN2069B-ULN2071B V_R = 80 V T_{amb} = 25°C T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp Diode Forward Voltage	for ULN2065B-ULN2067B and ULN2069B-ULN2071B I_F = 1 A I_F = 1.5 A			 1.75 2	 V V	7

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

TEST CIRCUITS

Figure 1.

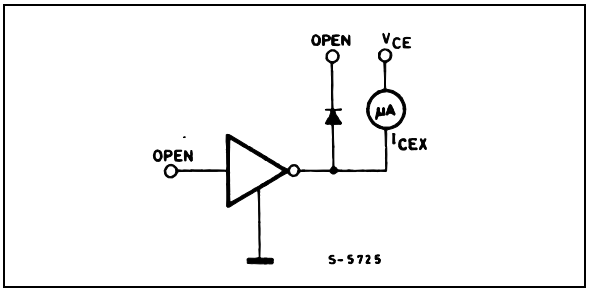


Figure 2.

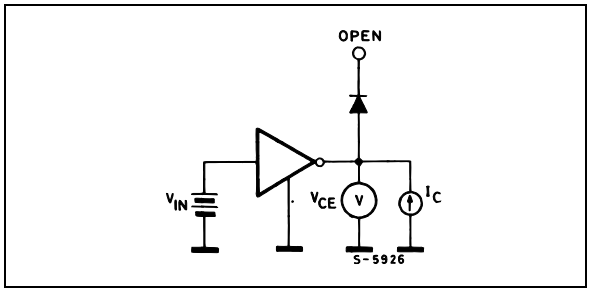


Figure 3.

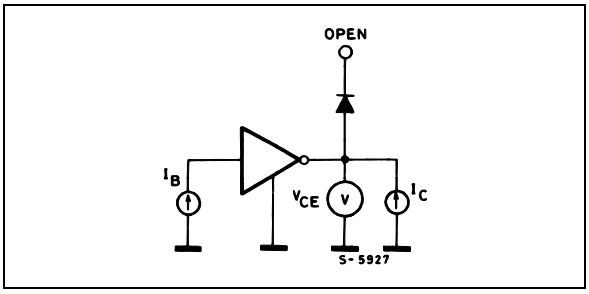


Figure 4.

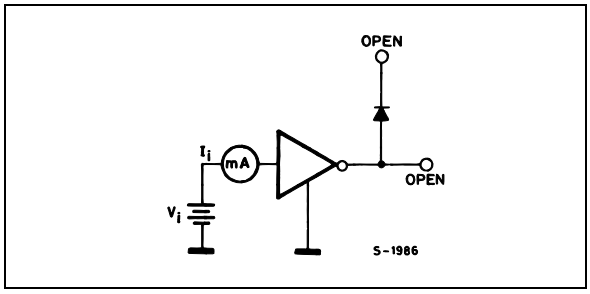


Figure 5.

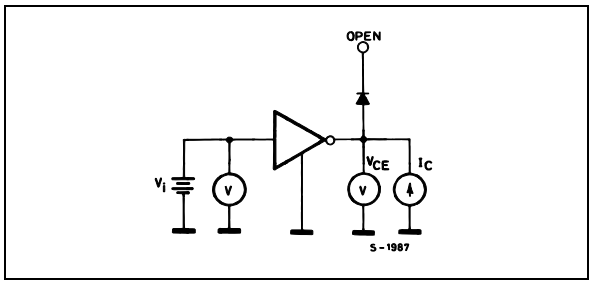


Figure 6.

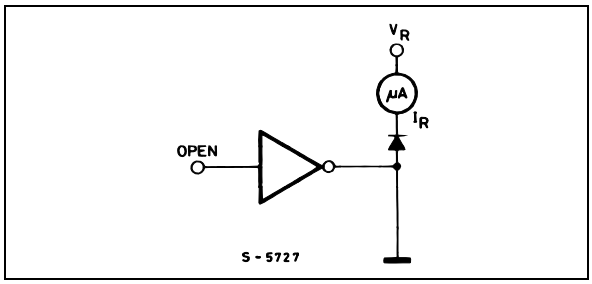


Figure 7.

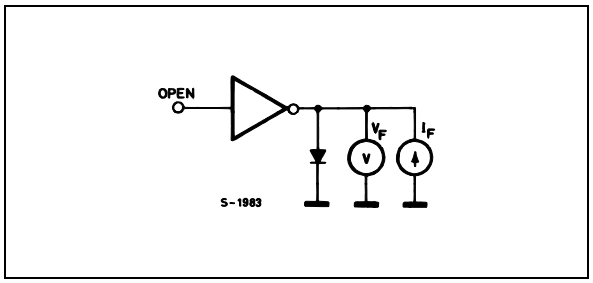


Figure 8.

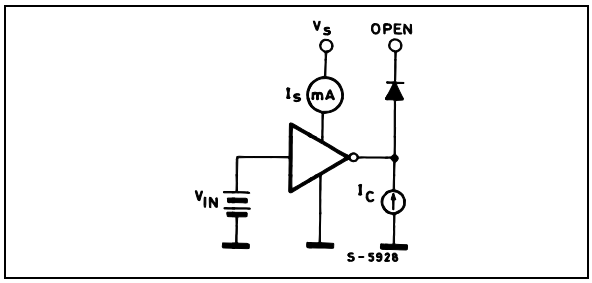


Figure 9 : Input Current as a Function of Input Voltage.

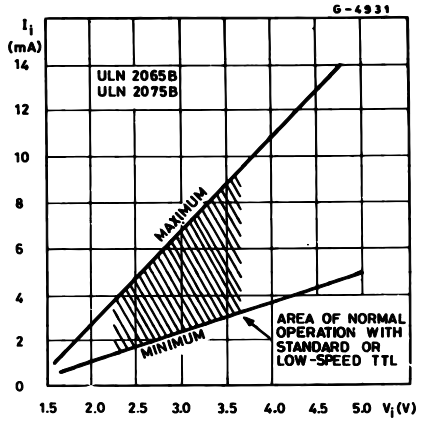


Figure 10 : Input Current as a Function of Input Voltage.

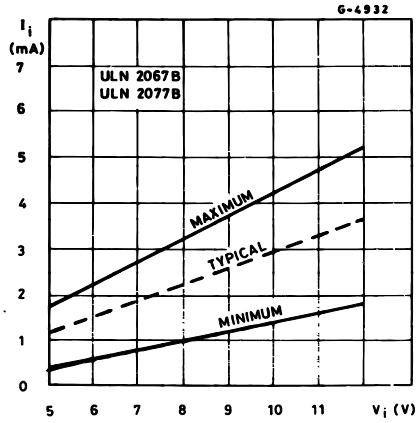
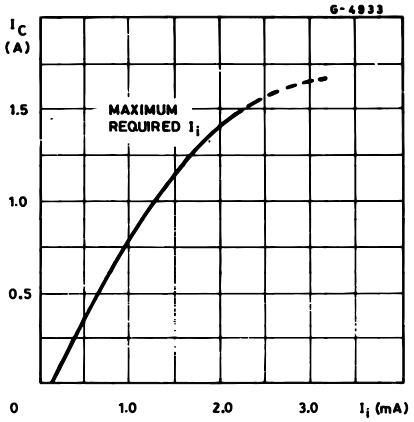


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "∝" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

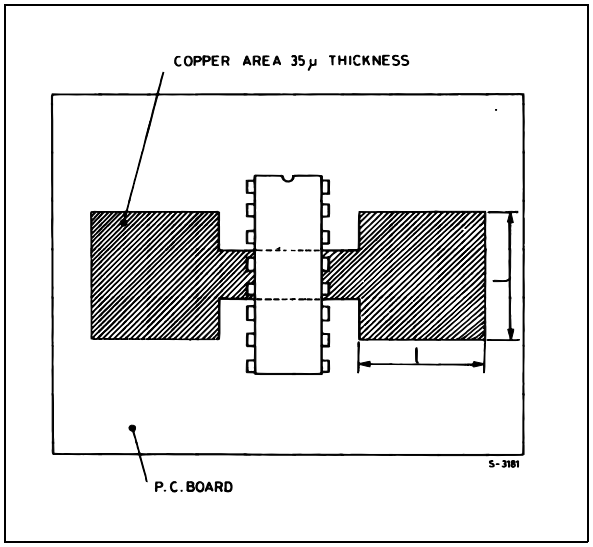


Figure 13 : External Heatsink Mounting Example.

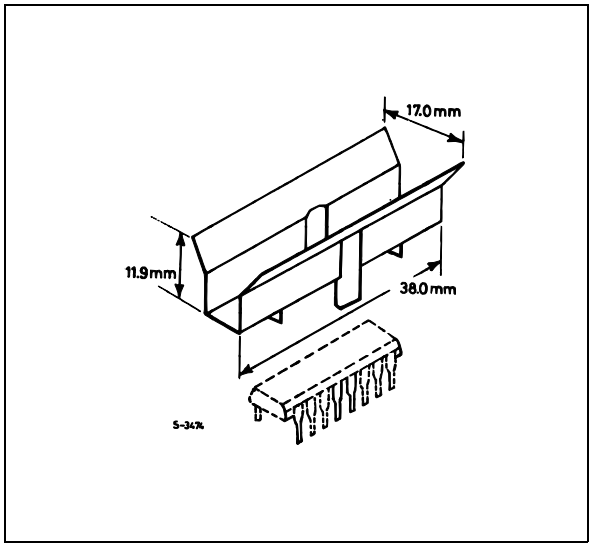


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

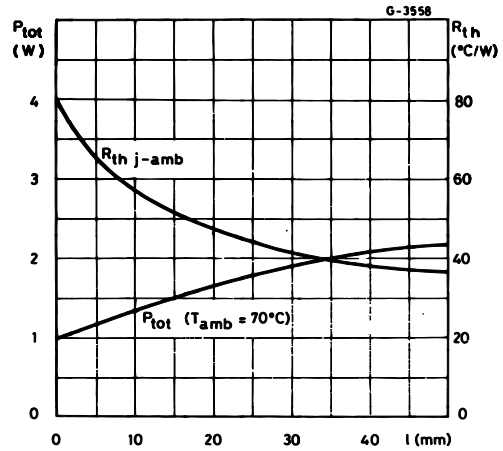
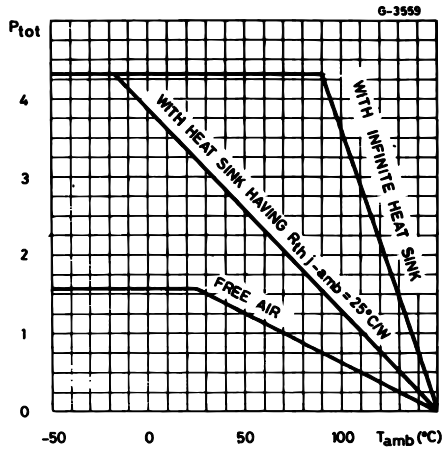
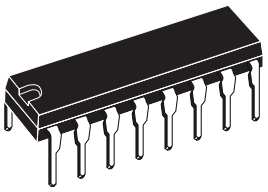


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



Powerdip 16