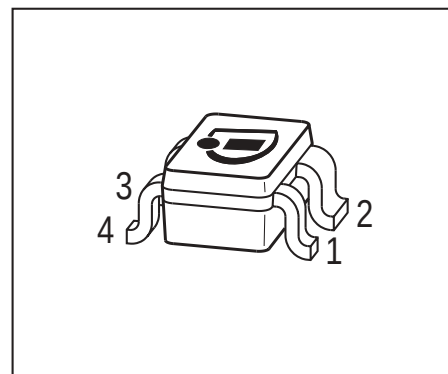


NPN Silicon RF Transistor

- For low current applications
- For oscillators up to 12 GHz
- Noise figure $F = 1.25$ dB at 1.8 GHz
outstanding $G_{ms} = 23$ dB at 1.8 GHz
- Transition frequency $f_T = 25$ GHz
- Gold metallization for high reliability
- SIEGET[®] 25 GHz f_T - Line
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Marking	Pin Configuration						Package
BFP405	ALs	1=B	2=E	3=C	4=E	-	-	SOT343

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}		V
$T_A > 0$ °C		4.5	
$T_A \leq 0$ °C		4.1	
Collector-emitter voltage	V_{CES}	15	
Collector-base voltage	V_{CBO}	15	
Emitter-base voltage	V_{EBO}	1.5	
Collector current	I_C	12	mA
Base current	I_B	1	
Total power dissipation ²⁾	P_{tot}	55	mW
$T_S \leq 120$ °C			
Junction temperature	T_j	150	°C
Ambient temperature	T_A	-65 ... 150	
Storage temperature	T_{stg}	-65 ... 150	

¹⁾Pb-containing package may be available upon special request

²⁾ T_S is measured on the collector lead at the soldering point to the pcb

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	≤ 520	K/W

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Collector-emitter breakdown voltage $I_C = 1\text{ mA}, I_B = 0$	$V_{(BR)CEO}$	4.5	5	-	V
Collector-emitter cutoff current $V_{CE} = 15\text{ V}, V_{BE} = 0$	I_{CES}	-	-	10	μA
Collector-base cutoff current $V_{CB} = 5\text{ V}, I_E = 0$	I_{CBO}	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 0.5\text{ V}, I_C = 0$	I_{EBO}	-	-	1	μA
DC current gain $I_C = 5\text{ mA}, V_{CE} = 4\text{ V}, \text{pulse measured}$	h_{FE}	60	95	130	-

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Transition frequency $I_C = 10\text{ mA}$, $V_{CE} = 3\text{ V}$, $f = 2\text{ GHz}$	f_T	18	25	-	GHz
Collector-base capacitance $V_{CB} = 2\text{ V}$, $f = 1\text{ MHz}$, $V_{BE} = 0$, emitter grounded	C_{cb}	-	0.05	0.1	pF
Collector emitter capacitance $V_{CE} = 2\text{ V}$, $f = 1\text{ MHz}$, $V_{BE} = 0$, base grounded	C_{ce}	-	0.24	-	
Emitter-base capacitance $V_{EB} = 0.5\text{ V}$, $f = 1\text{ MHz}$, $V_{CB} = 0$, collector grounded	C_{eb}	-	0.29	-	
Noise figure $I_C = 2\text{ mA}$, $V_{CE} = 2\text{ V}$, $f = 1.8\text{ GHz}$, $Z_S = Z_{Sopt}$	F	-	1.25	-	dB
Power gain, maximum stable ¹⁾ $I_C = 5\text{ mA}$, $V_{CE} = 2\text{ V}$, $Z_S = Z_{Sopt}$, $Z_L = Z_{Lopt}$, $f = 1.8\text{ GHz}$	G_{ms}	-	23	-	dB
Insertion power gain $V_{CE} = 2\text{ V}$, $I_C = 5\text{ mA}$, $f = 1.8\text{ GHz}$, $Z_S = Z_L = 50\ \Omega$	$ S_{21} ^2$	14	18.5	-	
Third order intercept point at output ²⁾ $V_{CE} = 2\text{ V}$, $I_C = 5\text{ mA}$, $f = 1.8\text{ GHz}$, $Z_S = Z_L = 50\ \Omega$	IP_3	-	15	-	dBm
1dB Compression point at output $I_C = 5\text{ mA}$, $V_{CE} = 2\text{ V}$, $Z_S = Z_L = 50\ \Omega$, $f = 1.8\text{ GHz}$	P_{-1dB}	-	5	-	

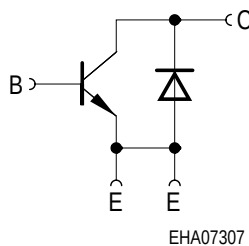
¹⁾ $G_{ms} = |S_{21}| / |S_{12}|$
²⁾ IP_3 value depends on termination of all intermodulation frequency components.
Termination used for this measurement is $50\ \Omega$ from 0.1 MHz to 6 GHz

For non-linear simulation:

- Use transistor chip parameters in Berkeley SPICE 2G.6 syntax for all simulators.
- If you need simulation of the reverse characteristics, add the diode with the C'-E'- diode data between collector and emitter.
- Simulation of package is not necessary for frequencies < 100MHz.
For higher frequencies add the wiring of package equivalent circuit around the non-linear transistor and diode model.

Note:

- This transistor is constructed in a common emitter configuration. This feature causes an additional reverse biased diode between emitter and collector, which does not effect normal operation.



Transistor Schematic Diagram

The common emitter configuration shows the following advantages:

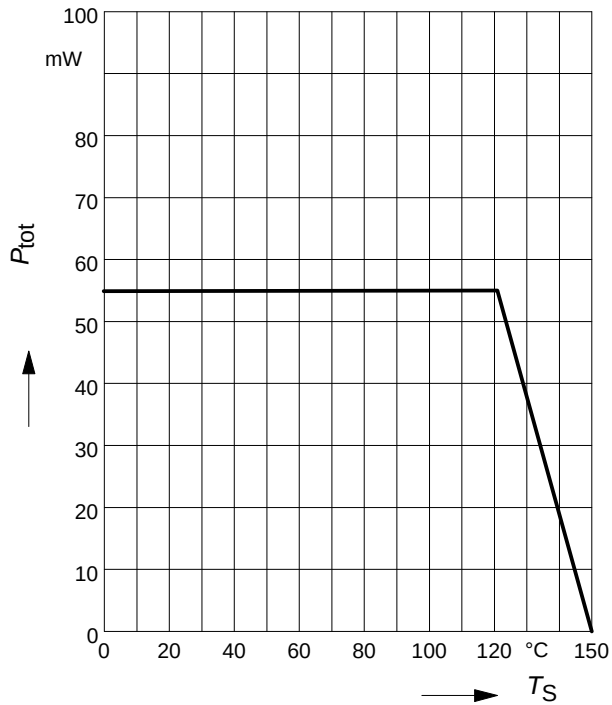
- Higher gain because of lower emitter inductance.
- Power is dissipated via the grounded emitter leads, because the chip is mounted on copper emitter leadframe.

Please note, that the broadest lead is the emitter lead.

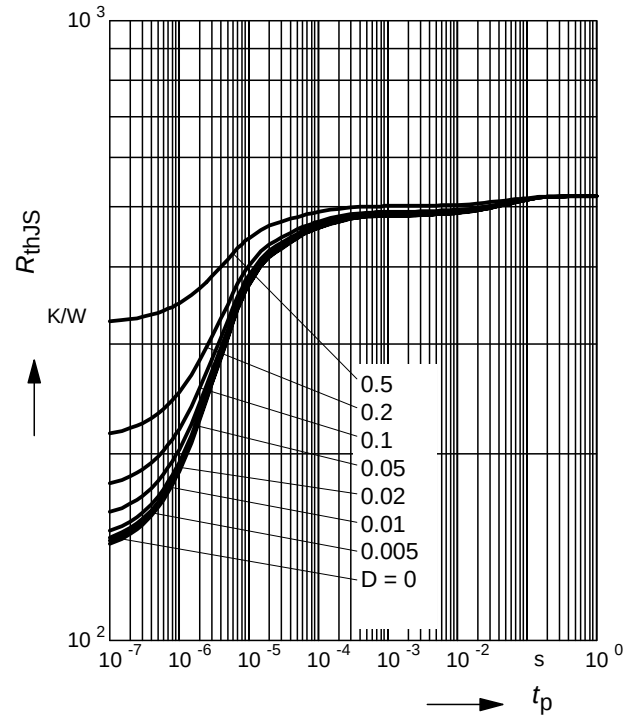
Common Emitter S- and Noise-parameter

For detailed S- and Noise-parameters please contact your local Infineon Technologies distributor or sales office to obtain a Infineon Technologies Application Notes CD-ROM or see Internet: <http://www.infineon.com/silicondiscretes>

Total power dissipation $P_{\text{tot}} = f(T_S)$

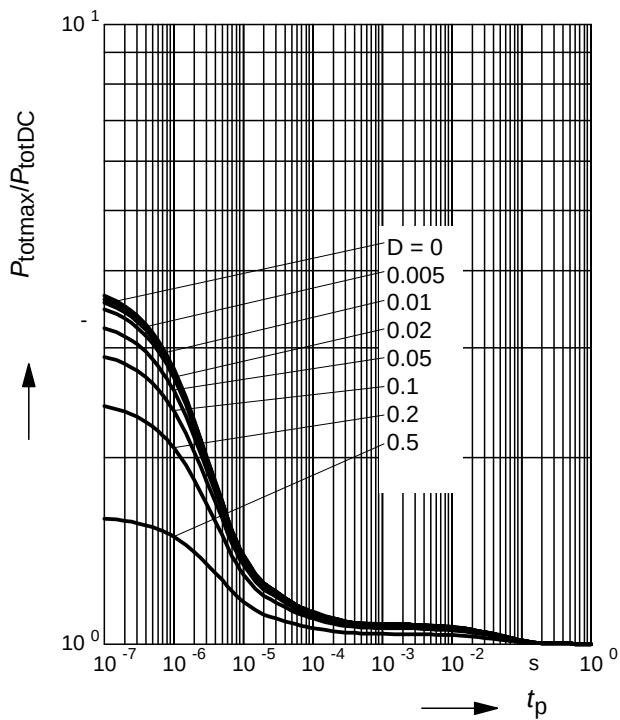


Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$



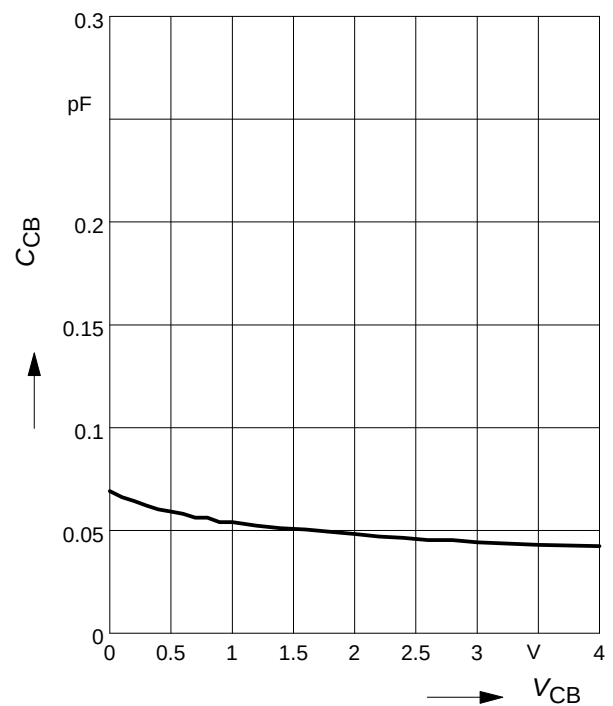
Permissible Pulse Load

$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$



Collector-base capacitance $C_{\text{cb}} = f(V_{\text{CB}})$

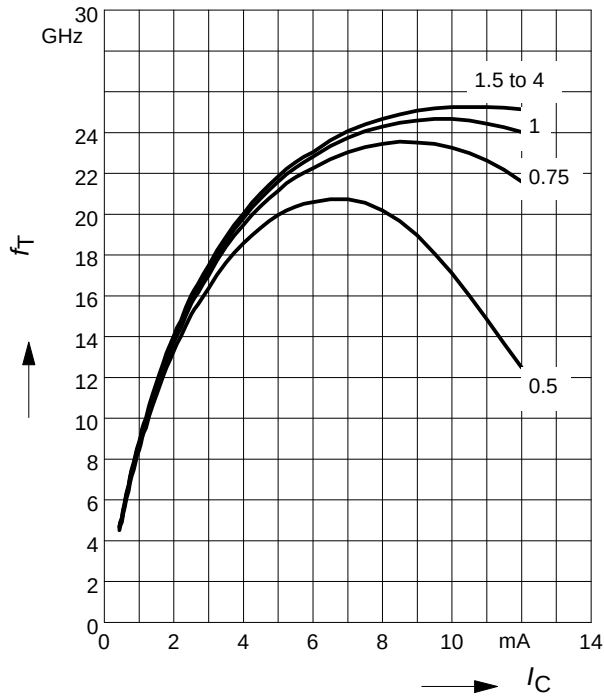
$f = 1\text{MHz}$



Transition frequency $f_T = f(I_C)$

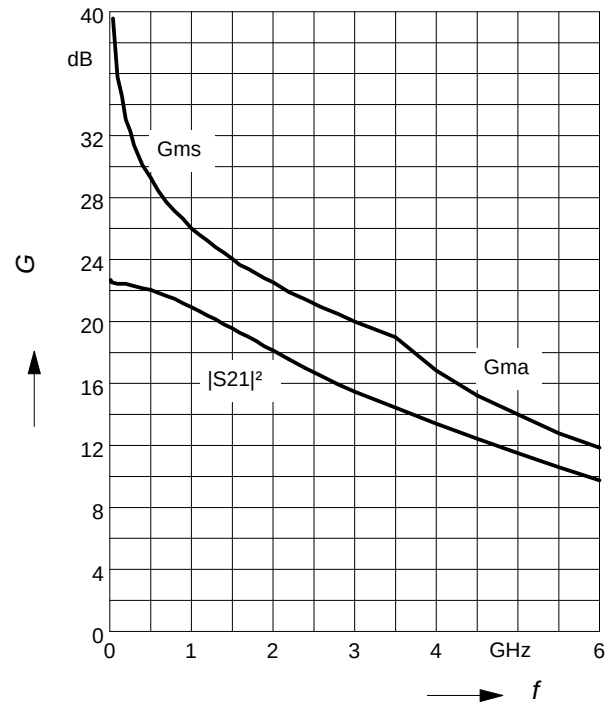
$f = 2 \text{ GHz}$

$V_{CE} = \text{parameter in V}$



Power gain $G_{ma}, G_{ms}, |S_{21}|^2 = f(f)$

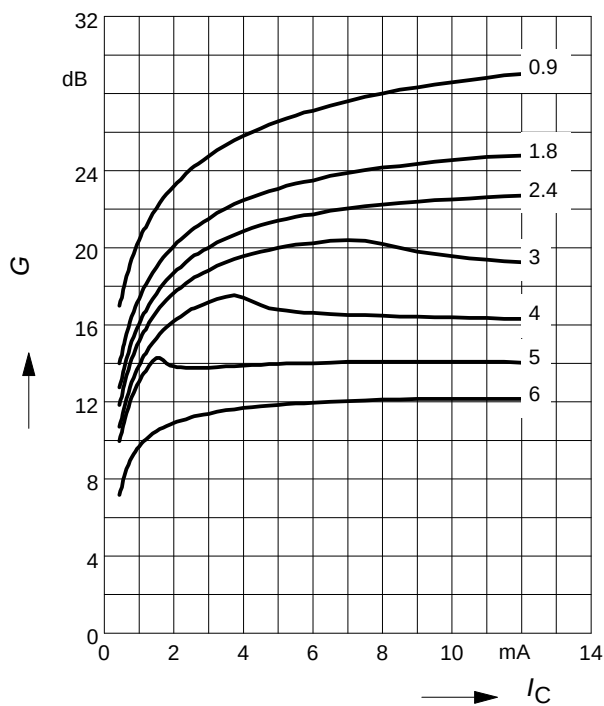
$V_{CE} = 2 \text{ V}, I_C = 5 \text{ mA}$



Power gain $G_{ma}, G_{ms} = f(I_C)$

$V_{CE} = 2 \text{ V}$

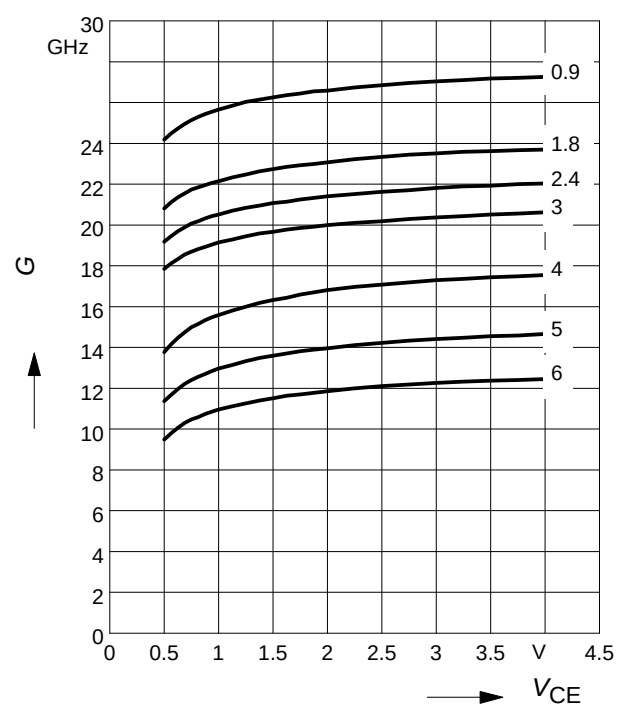
$f = \text{parameter in GHz}$



Power gain $G_{ma}, G_{ms} = f(V_{CE})$

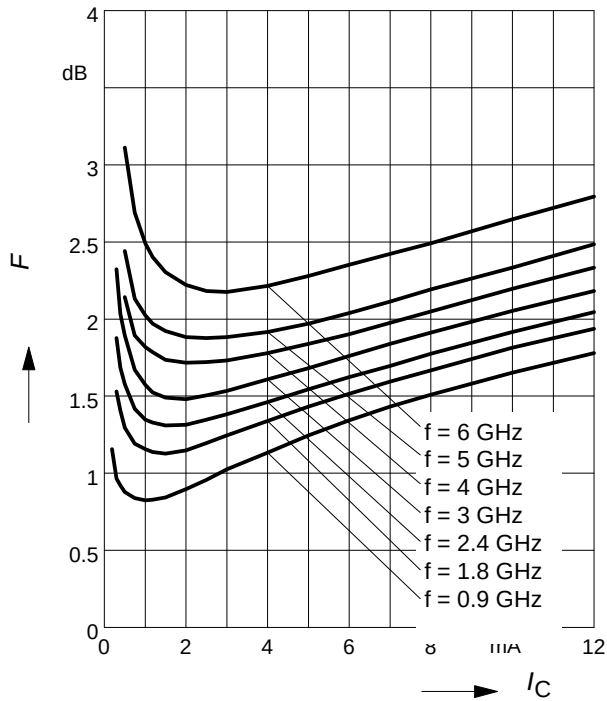
$I_C = 5 \text{ mA}$

$f = \text{parameter in GHz}$



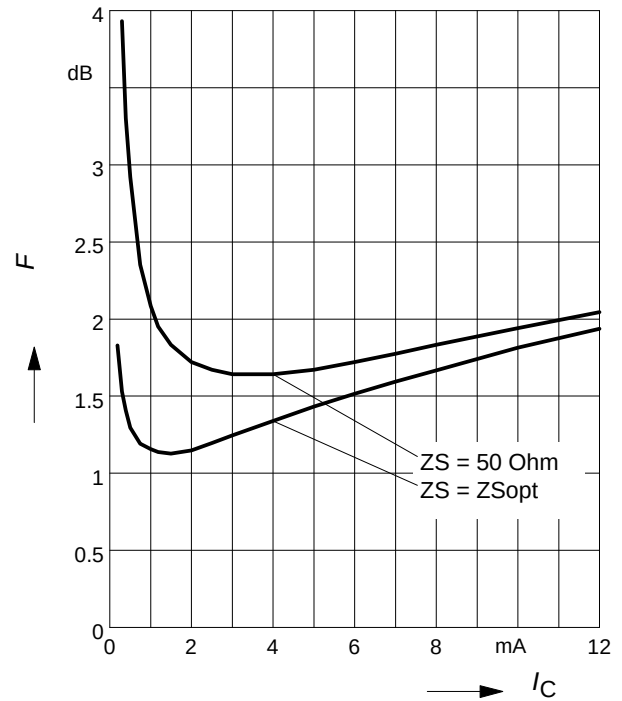
Noise figure $F = f(I_C)$

$V_{CE} = 2 \text{ V}$, $Z_S = Z_{Sopt}$



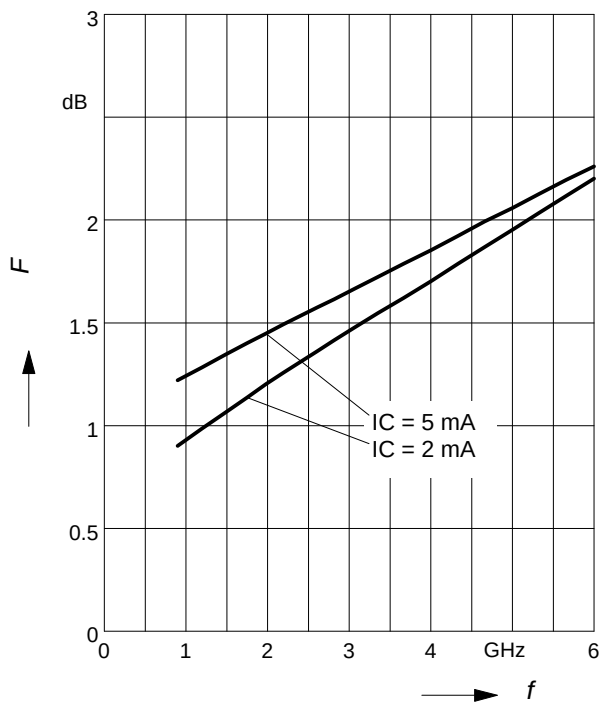
Noise figure $F = f(I_C)$

$V_{CE} = 2 \text{ V}$, $f = 1.8 \text{ GHz}$



Noise figure $F = f(f)$

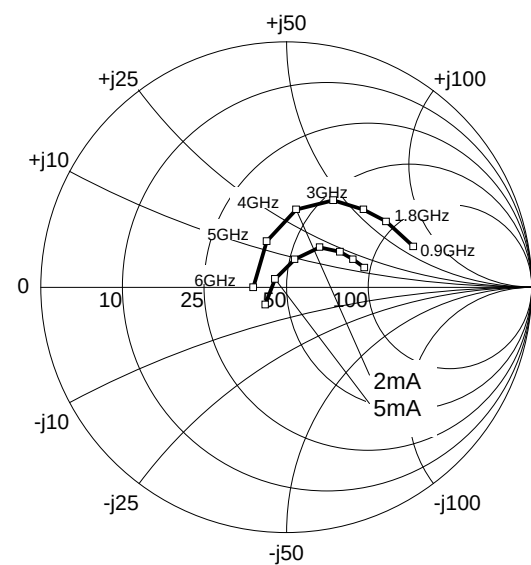
$V_{CE} = 1 \text{ V}$, $Z_S = Z_{Sopt}$



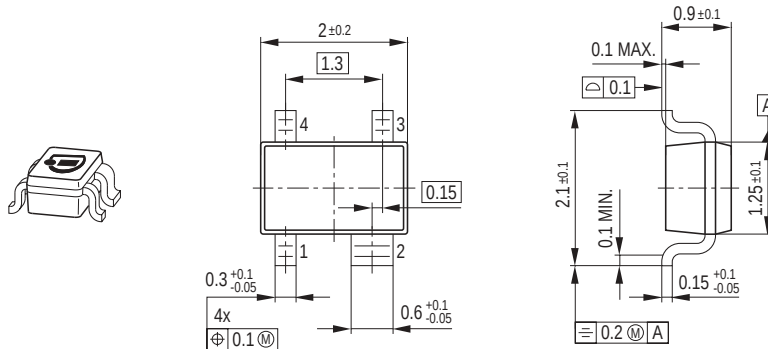
Source impedance for min.

noise figure vs. frequency

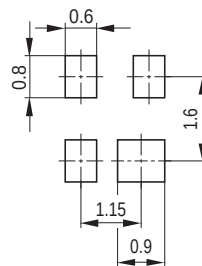
$V_{CE} = 3 \text{ V}$, $I_C = 2 \text{ mA} / 5 \text{ mA}$



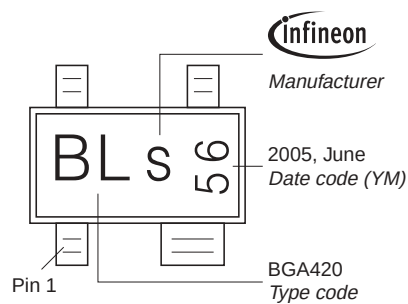
Package Outline



Foot Print

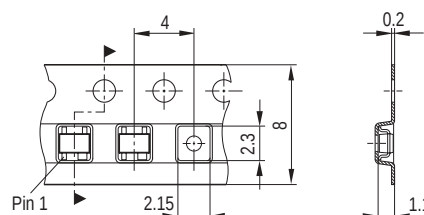


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



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