

EFM[®]32

... the world's most energy friendly microcontrollers

GECKO DATASHEET

EFM32G890F128/EFM32G890F64/EFM32G890F32

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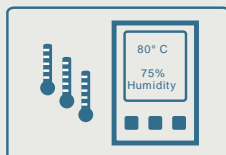
- **ARM Cortex-M3 CPU platform**
 - High Performance 32-bit processor @ up to 32 MHz
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 20 nA @ 3 V Shutoff Mode
 - 0.6 μ A @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 0.9 μ A @ 3 V Deep Sleep Mode, including Real Time Clock with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 45 μ A/MHz @ 3 V Sleep Mode
 - 180 μ A/MHz @ 3 V Run Mode, with code executed from flash
- **128/64/32 KB Flash**
- **16/16/8 KB RAM**
- **90 General Purpose I/O pins**
 - Configurable Push-pull, Open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 16 asynchronous external interrupts
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
 - 3x 16-bit Timer/Counter
 - 3x3 Compare/Capture/PWM channels
 - Dead-Time Insertion on TIMER0
 - 16-bit Low Energy Timer
 - 24-bit Real-Time Counter
 - 3x 8-bit Pulse Counter
 - Asynchronous pulse counting/quadrature decoding
 - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Integrated LCD Controller for up to 4x40 segments**
 - Voltage boost, adjustable contrast adjustment and autonomous animation feature
- **External Bus Interface for up to 64 MB of external memory mapped space**
- **Communication interfaces**
 - 3x Universal Synchronous/Asynchronous Receiver/Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA
 - Triple buffered full/half-duplex operation
 - 4-16 data bits
 - Universal Asynchronous Receiver/Transmitter
 - Triple buffered full/half-duplex operation
 - 8-9 data bits
 - 2x Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - I²C Interface with SMBus support
 - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
 - 12-bit 1 Msamples/s Analog to Digital Converter
 - 8 single ended channels/4 differential channels
 - On-chip temperature sensor
 - Conversion tailgating for predictable latency
 - 12-bit 500 ksamples/s Digital to Analog Converter
 - 2 single ended channels/1 differential channel
 - 2x Analog Comparator
 - Programmable speed/current
 - Capacitive sensing with up to 8 inputs
 - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
 - 1-pin Serial Wire Viewer
- **Temperature range -40 to 85 °C**
- **Single power supply 1.8 to 3.8 V**
- **BGA112 package**

EFM32G890 microcontrollers are suited for all battery operated applications

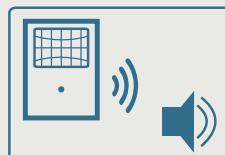
Energy Metering



Industrial/ Home Automation



Wireless Alarm/ Security



Medical Systems



1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32G890 devices.

Table 1.1. Ordering Information

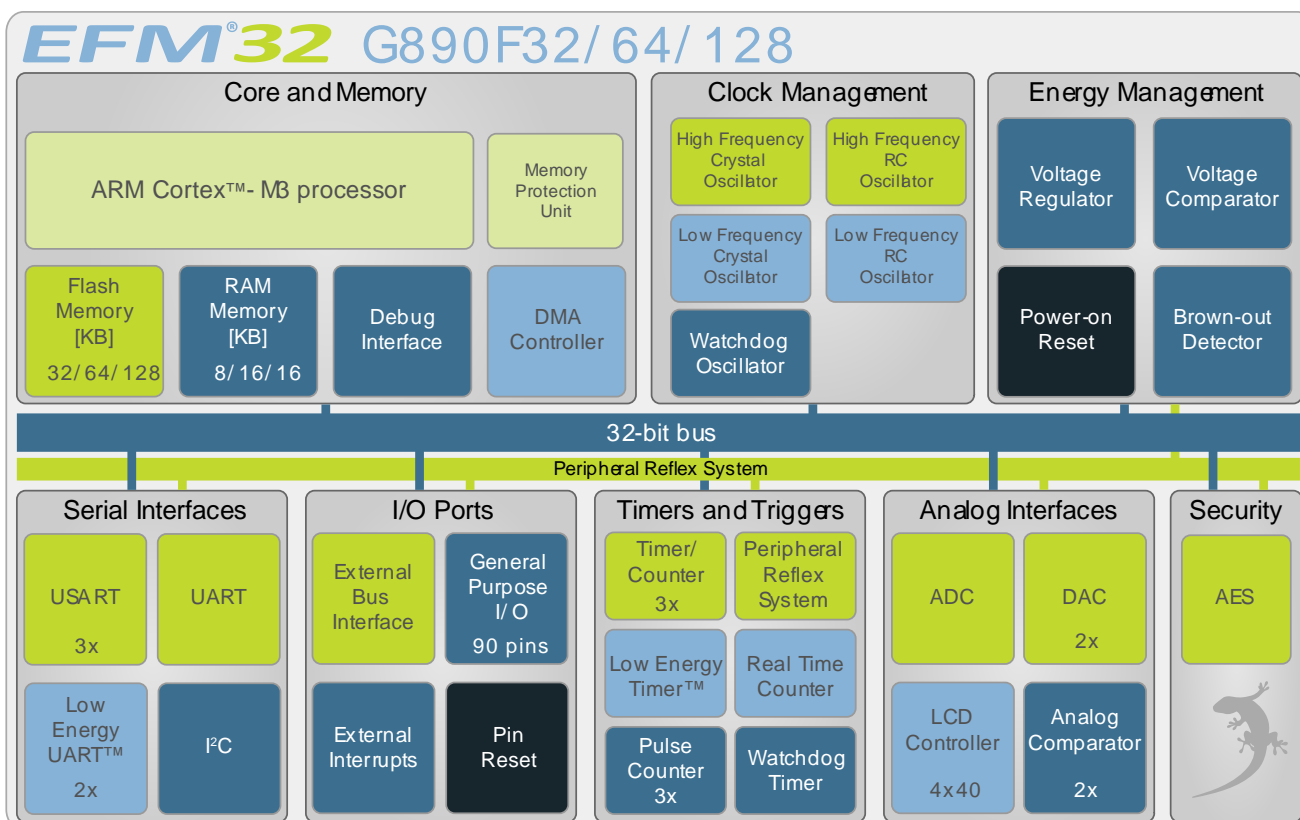
Ordering Code	Flash (KB)	RAM (KB)	Max Speed (MHz)	Supply Voltage	Temperature	Package
EFM32G890F32-BGA112	32	8	32	1.8 to 3.8V	-40 to 85 °C	BGA112
EFM32G890F64-BGA112	64	16	32	1.8 to 3.8V	-40 to 85 °C	BGA112
EFM32G890F128-BGA112	128	16	32	1.8 to 3.8V	-40 to 85 °C	BGA112

Visit www.energymicro.com for information on global distributors and representatives or contact sales@energymicro.com for additional information.

1.1 Block Diagram

A block diagram of the EFM32G890 is shown in Figure 1.1 (p. 2) .

Figure 1.1. Block Diagram



2 System Summary

2.1 System Introduction

The EFM32G family of MCUs is the world's most energy friendly microcontroller. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G890 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32G Reference Manual*.

2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32G Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to the DAC. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all

peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

2.1.11 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and IrDA devices.

2.1.13 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/

s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.17 Low Energy Timer (LETIMER)

The unique LETIMER[™], the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.18 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.19 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.21 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from >8 external pins and 6 internal signals.

2.1.22 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.23 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.24 General Purpose Input/Output (GPIO)

In the EFM32G890, there are 90 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.1.25 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 4x 40 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

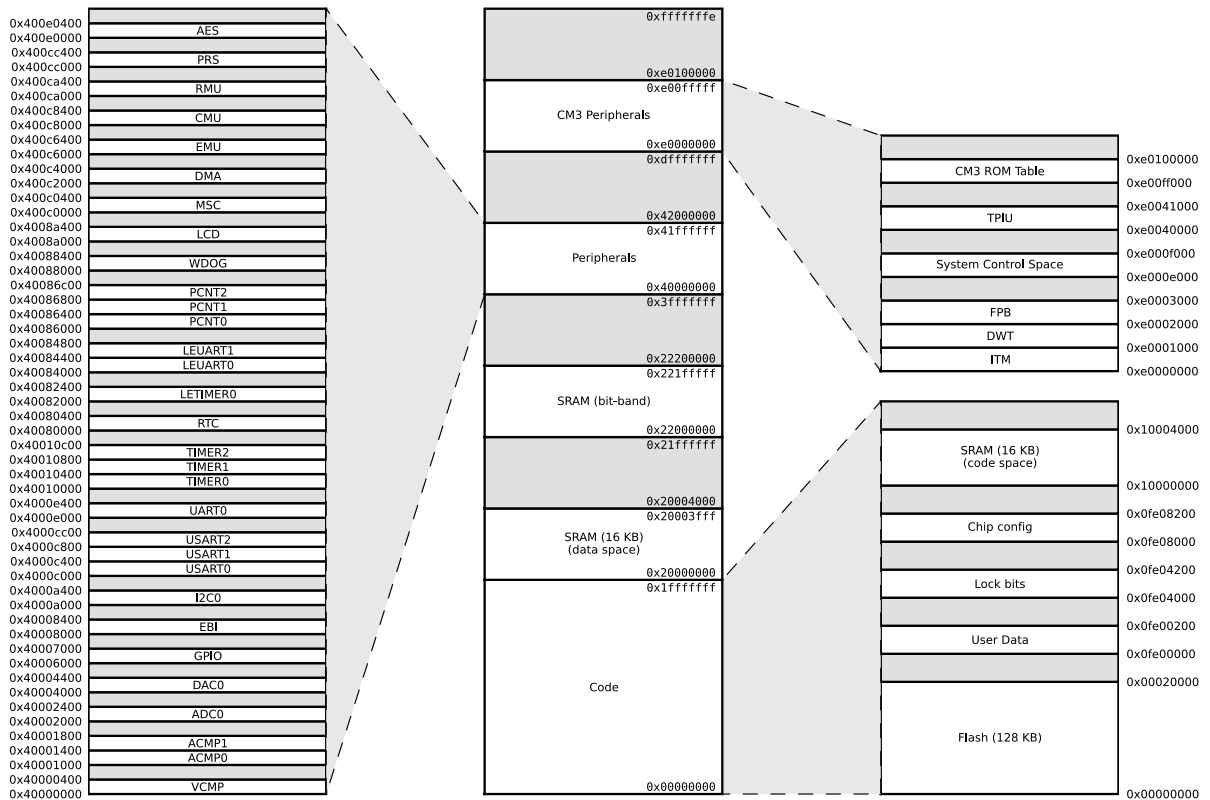
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	No IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	No IrDA	US2_TX, US2_RX, US2_CLK, US2_CS

Module	Configuration	Pin Connections
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	No DTI	TIM1_CC[2:0]
TIMER2	No DTI	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	8-bit count register	PCNT0_S[1:0]
PCNT1	8-bit count register	PCNT1_S[1:0]
PCNT2	8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 43)
LCD	Full configuration	LCD_SEG[39:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The *EFM32G890* memory map is shown in Figure 2.1 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.1. EFM32G890 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		85	$^{\circ}\text{C}$
T_J	Maximum junction temperature	JEDEC J-STD-020D			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40	25	85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.8	3.0	3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ESDHBM}	ESD (Human Body Model HBM)	T _{AMB} =25°C			2	kV
V _{ESDCDM}	ESD (Charged Device Model, CDM)	T _{AMB} =25°C			500	V
MSL	Moisture sensitivity level	JEDEC J-STD-20D. Level 3			168	hrs
LU	Latchup sensitivity	JESD78 Latchup test procedure. Class II level A.			85	°C

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		180		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		190	240	μA/ MHz
		1 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		220		μA/ MHz
I _{EM1}	EM1 current	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		45		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		47	57	μA/ MHz
		1 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V		103		μA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9		μA
		EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =85°C		3.0	6.0	μA
I _{EM3}	EM3 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.59		μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		2.75	5.8	μA
I _{EM4}	EM4 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.02		μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		0.25	0.7	μA

Figure 3.1. EM0 Current consumption vs supply voltage, executing prime number calculation code from flash with HFRCO running at 28MHz

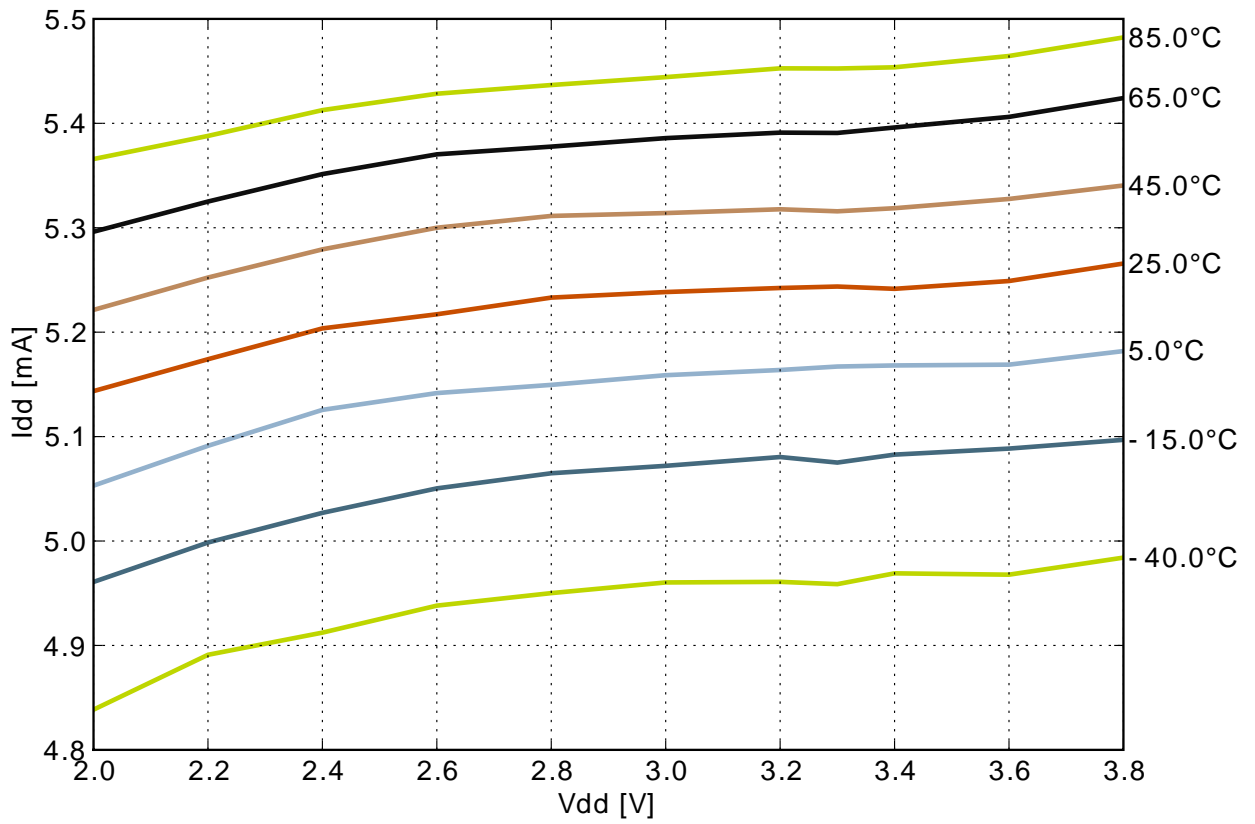


Figure 3.2. EM0 Current consumption vs temperature, executing prime number calculation code from flash with HFRCO running at 28MHz

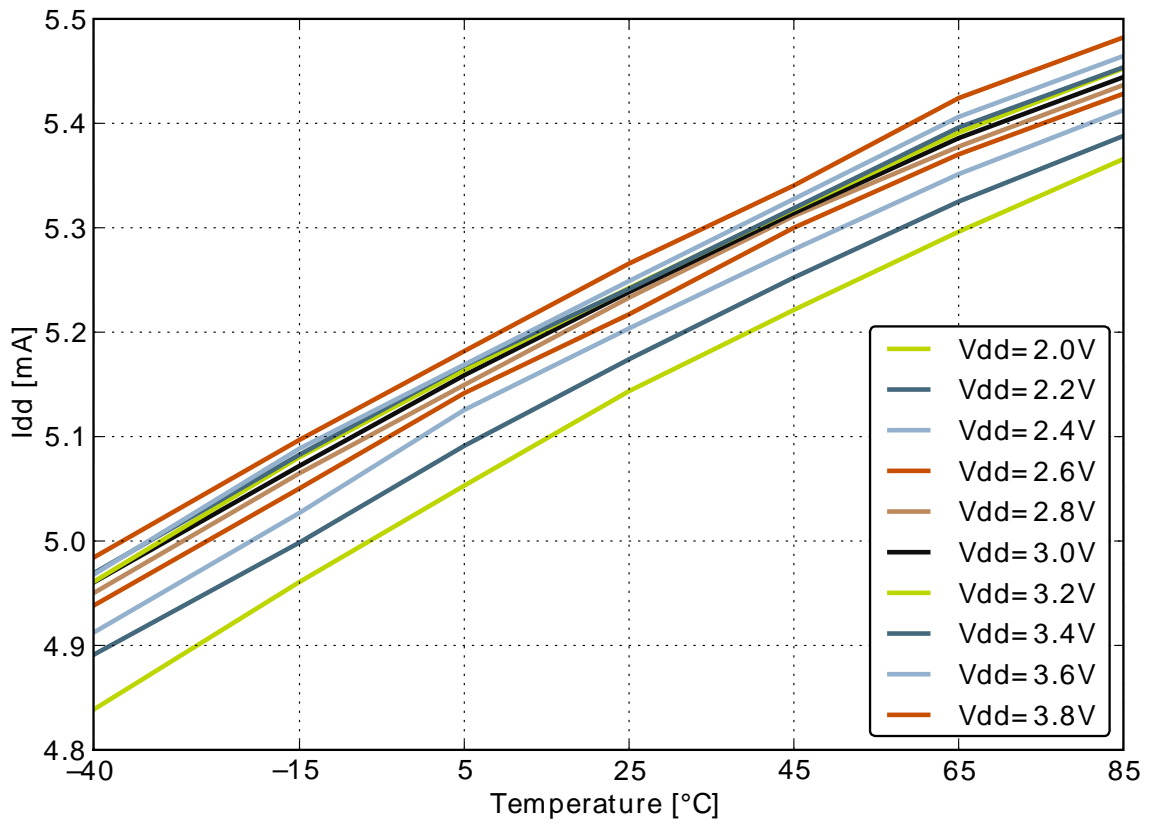


Figure 3.3. EM1 Current consumption vs supply voltage, all peripheral clocks disabled, HFRCO running at 28MHz

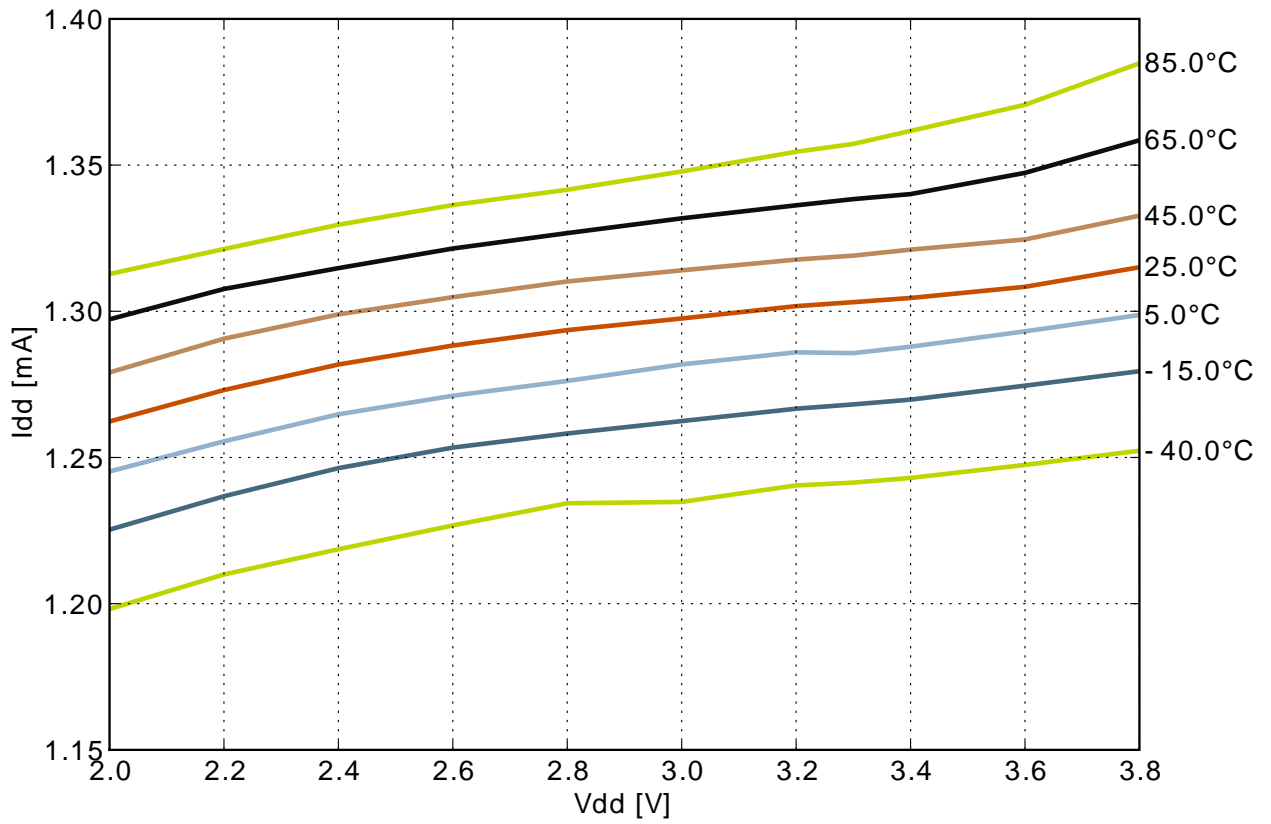


Figure 3.4. EM1 Current consumption vs temperature, all peripheral clocks disabled, HFRCO running at 28MHz

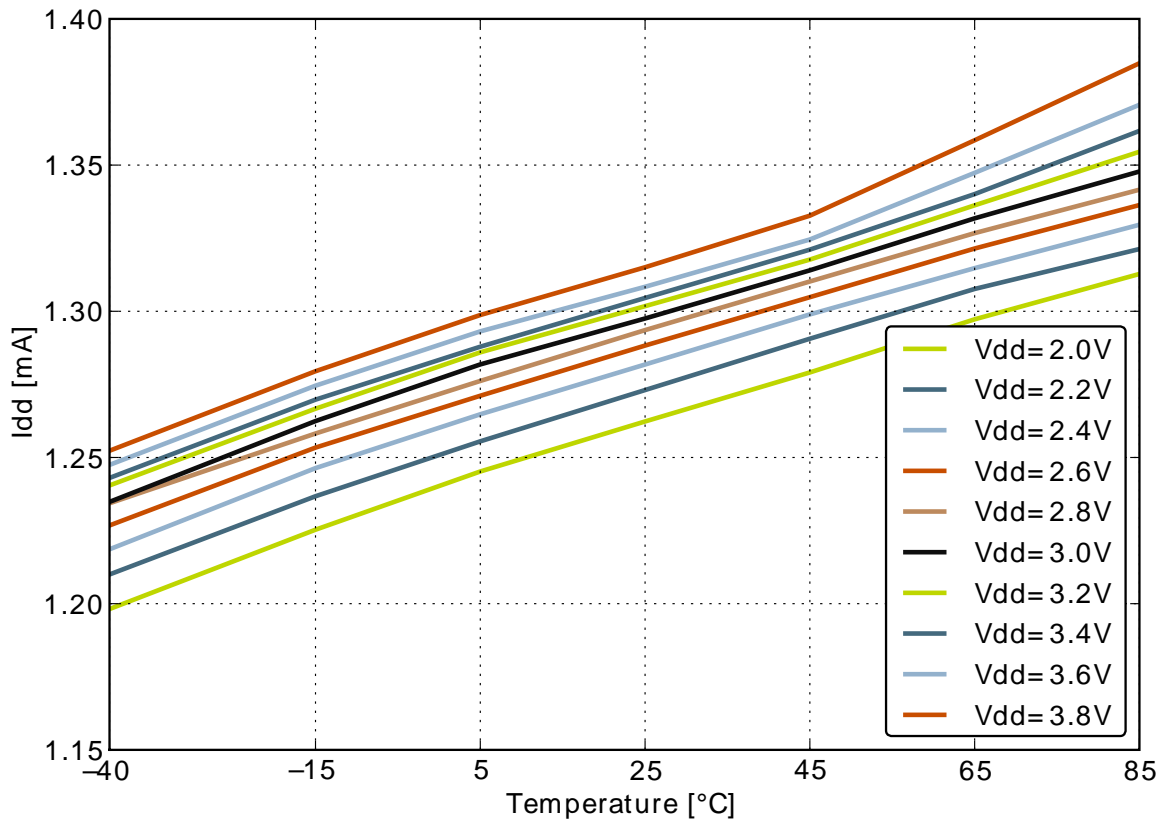


Figure 3.5. EM2 Current consumption vs supply voltage. RTC incremented each second, RTC prescaled to 1kHz, 32 kHz LFRCO.

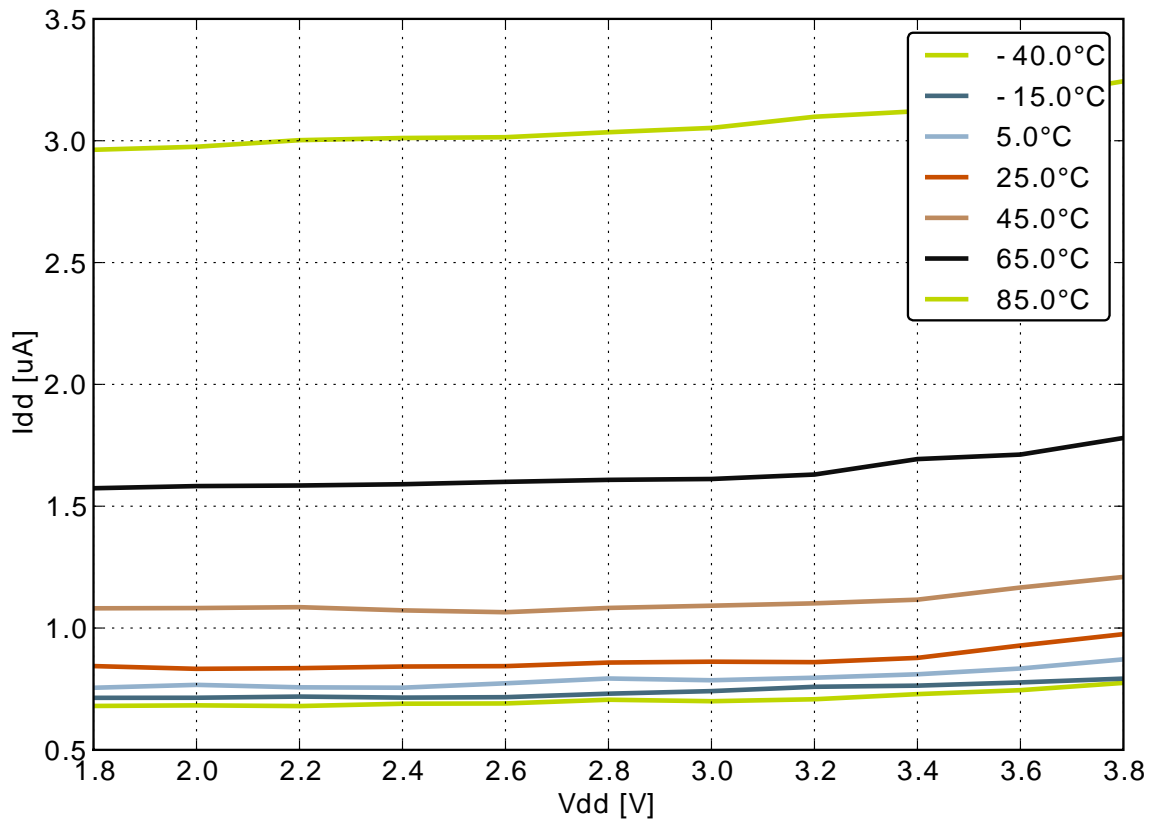


Figure 3.6. EM2 Current consumption vs temperature. RTC incremented each second, RTC prescaled to 1kHz, 32 kHz LFRCO.

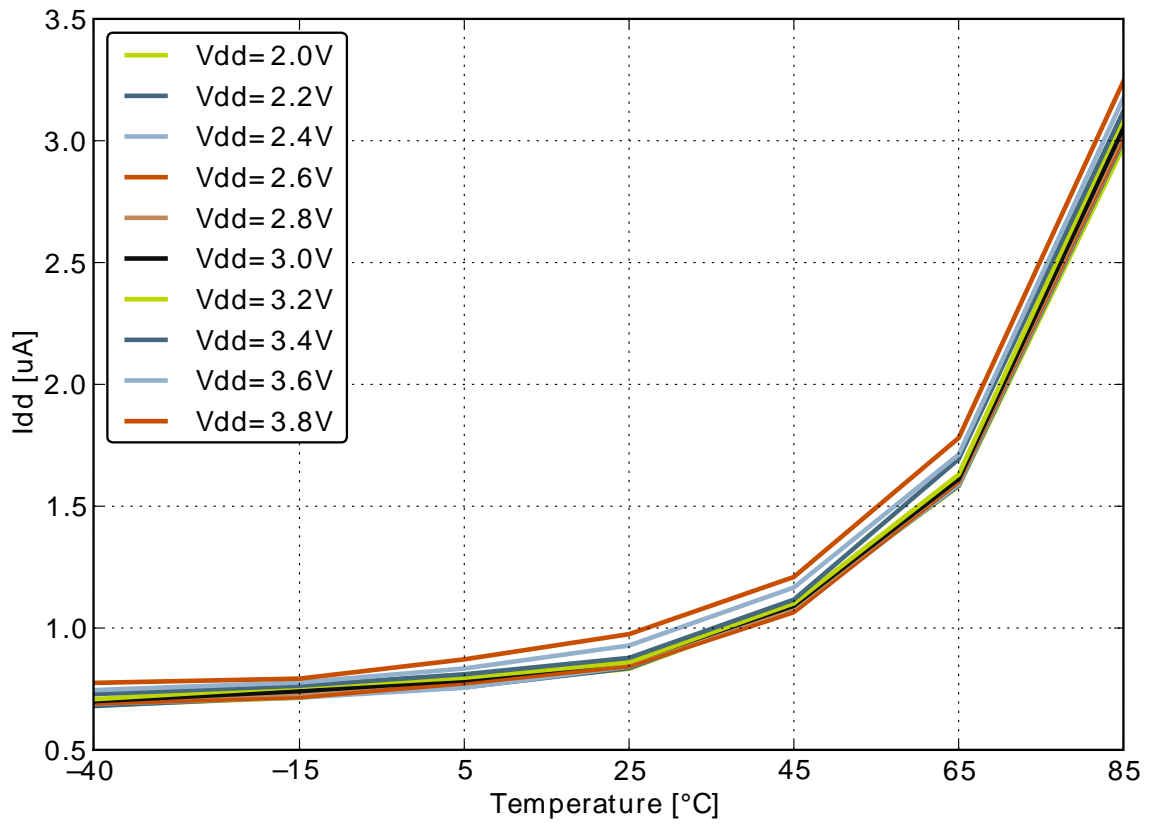


Figure 3.7. EM3 Current consumption vs supply voltage

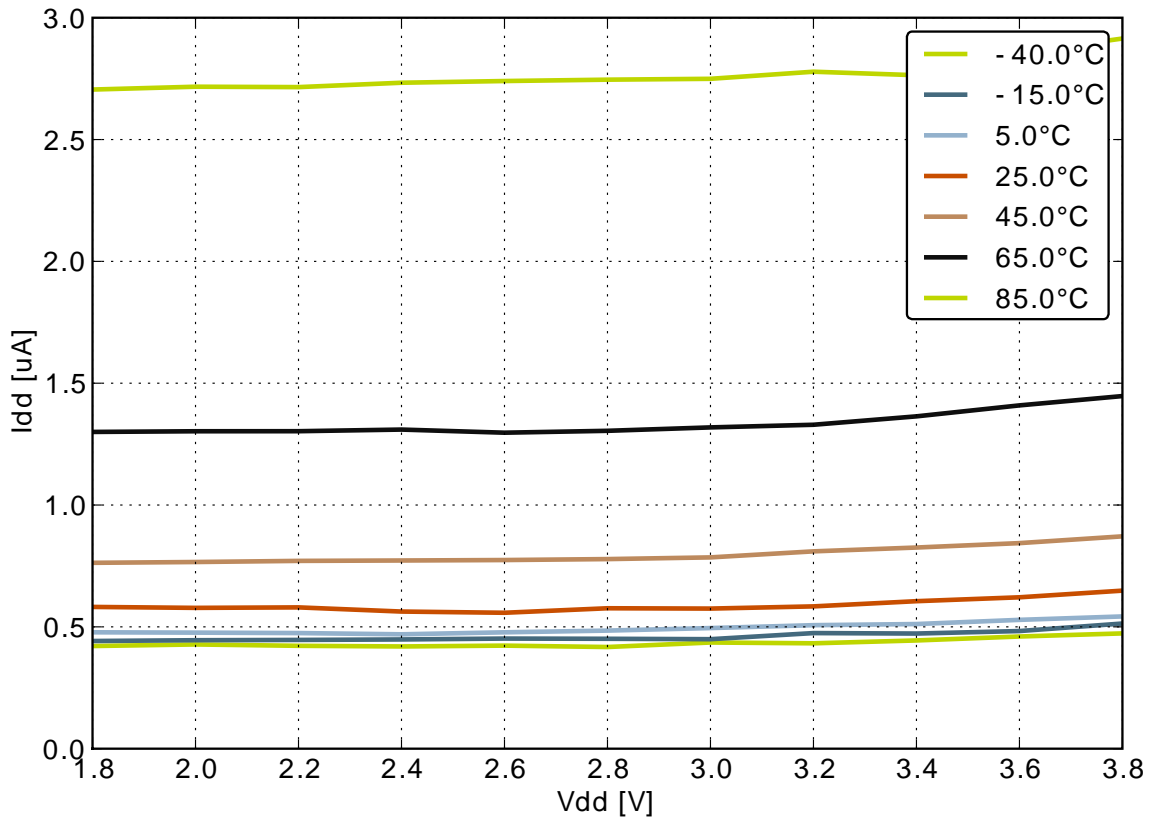


Figure 3.8. EM3 Current consumption vs temperature

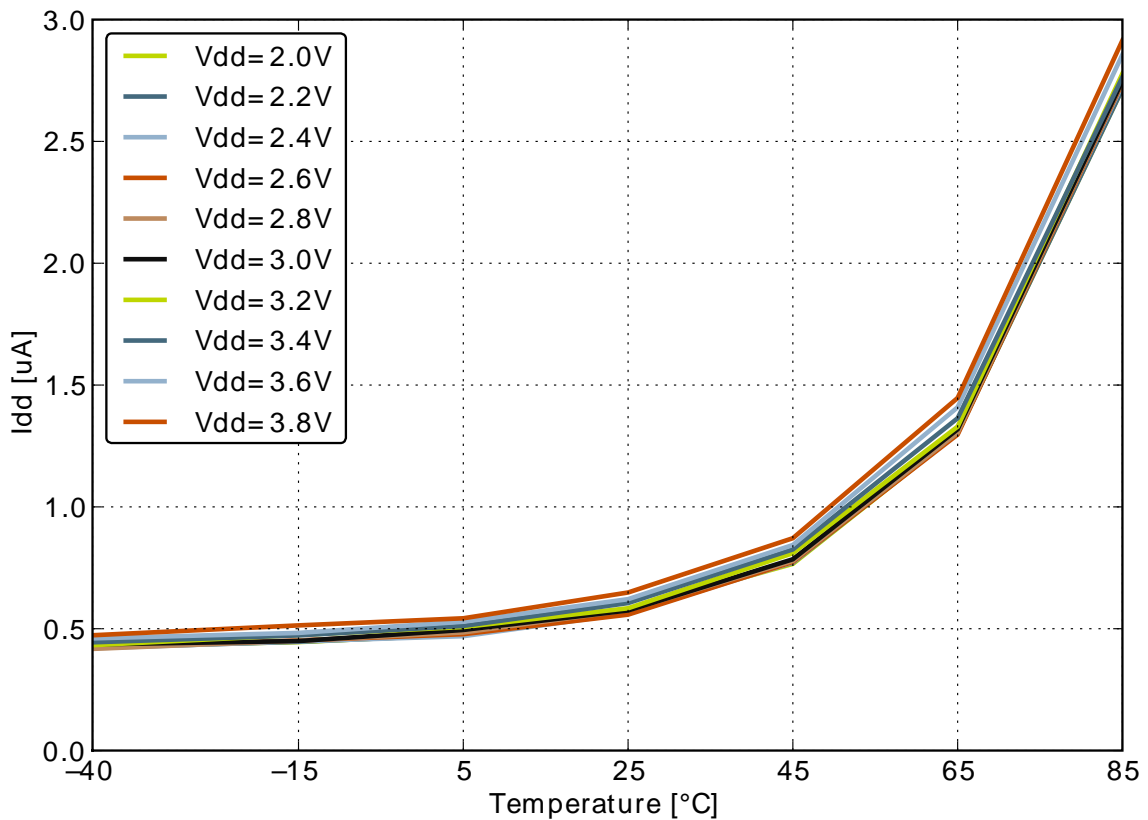


Figure 3.9. EM4 Current consumption vs supply voltage

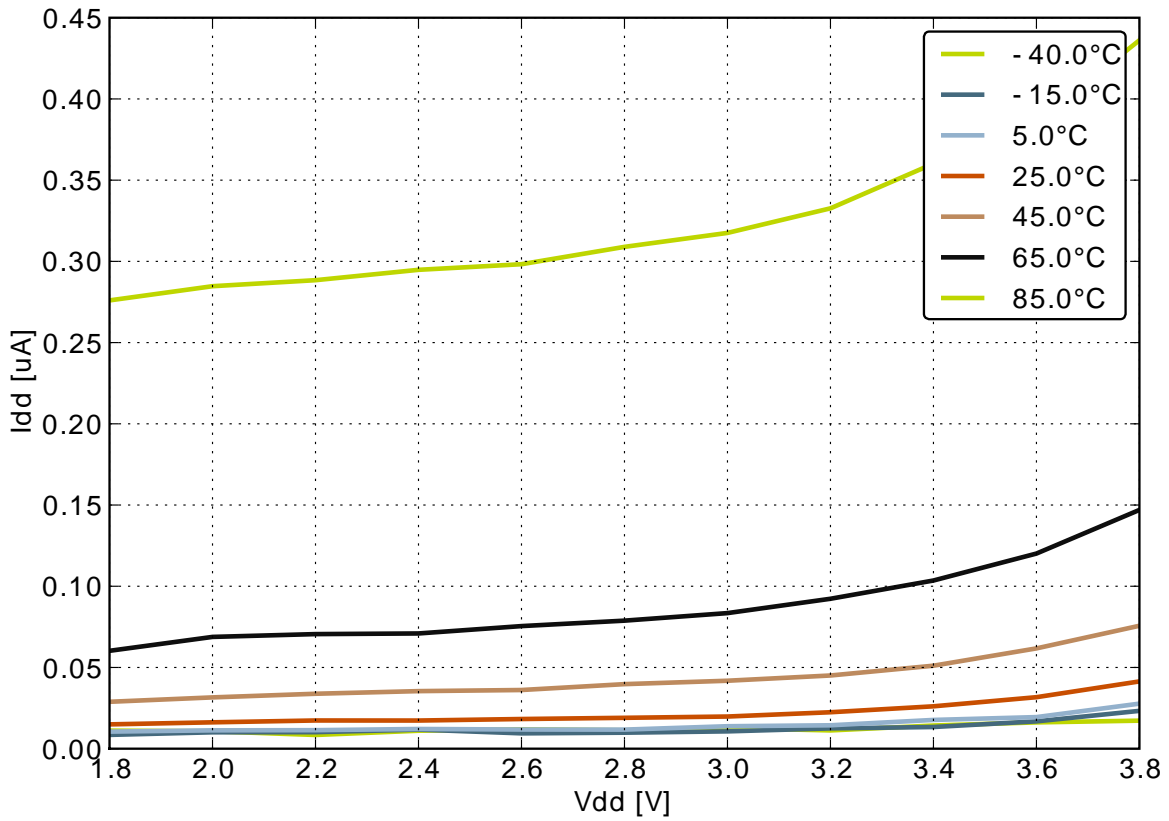
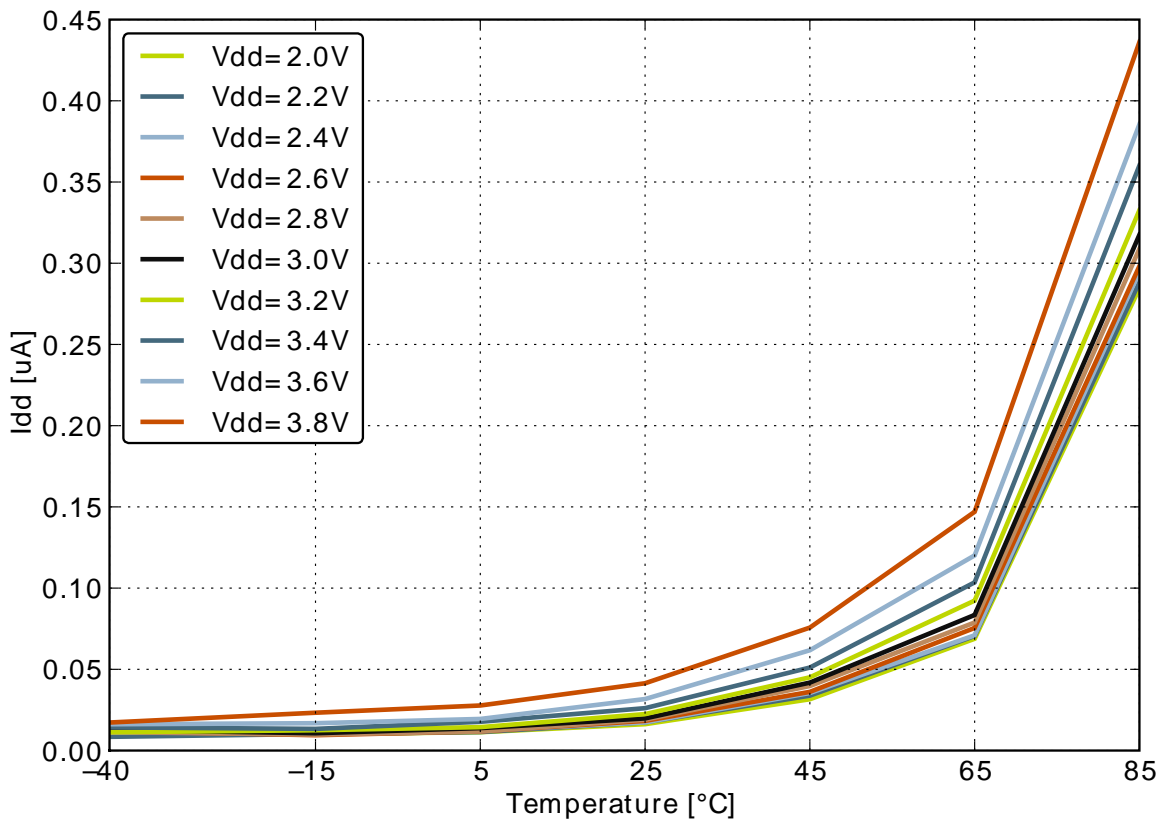


Figure 3.10. EM4 Current consumption vs temperature



3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0			0 ¹		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0			2		μ s
t_{EM30}	Transition time from EM3 to EM0			2		μ s
t_{EM40}	Transition time from EM4 to EM0			163		μ s

¹Core wakeup time only.

3.6 Power Management

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.77		1.80	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.65	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage	Uncalibrated		1.82		V
$V_{BODexthyst}$	BOD hysteresis on external supply voltage			150		mV
TC_{BGR}	Temperature coefficient of band-gap reference (BGR)	Relative voltage variation in EM0 based on the difference in V_{ref} between -40°C and 85°C.			0.55	%
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μ s
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μ F

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <85°C	10			years
t _{W_PROG}	Word (32-bit) programming time		20			µs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms

3.8 General Purpose Input Output

Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.3V _{DD}	V
V _{IOIH}	Input high voltage		0.7V _{DD}			V
V _{IOOH}	Output high voltage relative to V _{DD}	Sourcing 6 mA, V _{DD} =1.8V	75			%
		Sourcing 6 mA, V _{DD} =3.0V	95			%
		Sourcing 20 mA, V _{DD} =1.8V	70			%
		Sourcing 20 mA, V _{DD} =3.0V	90			%
V _{IOOL}	Output low voltage relative to V _{DD}	Sinking 6 mA, V _{DD} =1.8V			25	%
		Sinking 6 mA, V _{DD} =3.0V			5	%
		Sinking 20 mA, V _{DD} =1.8V			30	%
		Sinking 20 mA, V _{DD} =3.0V			10	%
R _{PU}	I/O pin pull-up resistor			40		kOhm
R _{PD}	I/O pin pull-down resistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t _{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C _L =12.5-25pF.	20+0.1C _L		250	ns
		2mA drive strength and load capacitance C _L =350-600pF	20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.8 - 3.8 V	0.1V _{DD}			V

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, $C_L=10$ pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start-up time.	ESR=30 kOhm, $C_L=10$ pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

3.9.2 HFXO

Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, $C_L=20$ pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μ A
		32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μ A
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μ s

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency			32		kHz
t_{LFRCO}	Startup time not including software calibration			150		μ s
I_{LFRCO}	Current consumption			190		nA
TUNESTEP _{L-FR} FRCO	Frequency step for LSB change in TUNING value			1.5		%

3.9.4 HFRCO

Table 3.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		7		MHz
		1 MHz frequency band		1		MHz
t_{HFRCO}	Start-up time not including software calibration	$f_{HFRCO} = 14$ MHz		0.6		μ s
I_{HFRCO}	Current consumption	$f_{HFRCO} = 28$ MHz		106		μ A
		$f_{HFRCO} = 21$ MHz		93		μ A
		$f_{HFRCO} = 14$ MHz		77		μ A
		$f_{HFRCO} = 11$ MHz		72		μ A
		$f_{HFRCO} = 7$ MHz		63		μ A
DC _{HFRCO}	Duty cycle	$f_{HFRCO} = 14$ MHz	48.5	50	51	%
TUNESTEP _{H-FR} FRCO	Frequency step for LSB change in TUNING value			0.3		%

3.9.5 ULFRCO

Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.8		1.5	kHz
TC _{ULFRCO}	Temperature coefficient			0.05		%/°C
VC _{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCCM}	Analog input common mode voltage range		0		V _{DD}	V
V _{ADCIN}	Input voltage range of external reference voltage, single ended and differential		1.25		V _{DD}	V
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		220		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		9		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		6		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		74		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		290		μA
		6 bit 10 kSamples/s, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		4		μA
I _{ADCREf}	Current consumption of internal voltage reference	Internal voltage reference		70		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
V _{ADCCMOUT}	Common mode output voltage range			1.65		V
f _{ADCCLK}	Frequency of ADC clock, max and min			13		MHz
t _{ADCCONV}	Conversion time			1		μs
t _{ADCACQ}	Acquisition time	Programmable		0.5		μs
t _{ADCACQVDD3}	Required sample time for VDD/3 reference			2		μs
t _{ADCSTART}	Startup time of reference generator in NORMAL mode and startup time ADC			5		μs
	Startup time of reference generator in KEEPAD-CWARM mode and startup time ADC			1		μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SNR _{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		1 MSamples/s, 12 bit, differential, 5V reference		73		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		100 kSamples/s, 12 bit, differential, 5V reference		73		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
		SNDR _{ADC}	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		68
1 MSamples/s, 12 bit, single ended, internal 2.5V reference				71		dB
1 MSamples/s, 12 bit, differential, internal 1.25V reference				69		dB
1 MSamples/s, 12 bit, differential, internal 2.5V reference				72		dB
1 MSamples/s, 12 bit, differential, 5V reference				72		dB
100 kSamples/s, 12 bit, single ended, internal 1.25V reference				68		dB
100 kSamples/s, 12 bit, single ended, internal 2.5V reference				71		dB
100 kSamples/s, 12 bit, differential, internal 1.25V reference				69		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, 5V reference		72		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		1 MSamples/s, 12 bit, differential, 5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, 5V reference		75		dB
V _{ADCOFFSET}	Offset voltage	Before calibration, single ended		10		mV
		After calibration, single ended		0.3		mV
		Before calibration, differential		10		mV
		After calibration, differential		0.3		mV
TGRAD _{ADCTH}	Thermometer output gradient			-1.85		mV/°C
				-6.1		ADC Codes/°C
DNL _{ADC}	Differential non-linearity (DNL)	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
		Internal 5V reference		1		LSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
INL _{ADC}	Integral non-linearity (INL), End point method	Internal 1.25V reference		2		LSB
		Internal 2.5V reference		2		LSB
		Internal 5V reference		2		LSB
MC _{ADC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 1.25V reference, differential		0		
		12 bit, internal 2.5V reference, single ended		0		
		12 bit, internal 2.5V reference, differential		0		
		12 bit, internal 5V reference, differential		0		

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.11 (p. 26) and Figure 3.12 (p. 27) , respectively.

Figure 3.11. Integral Non-Linearity (INL)

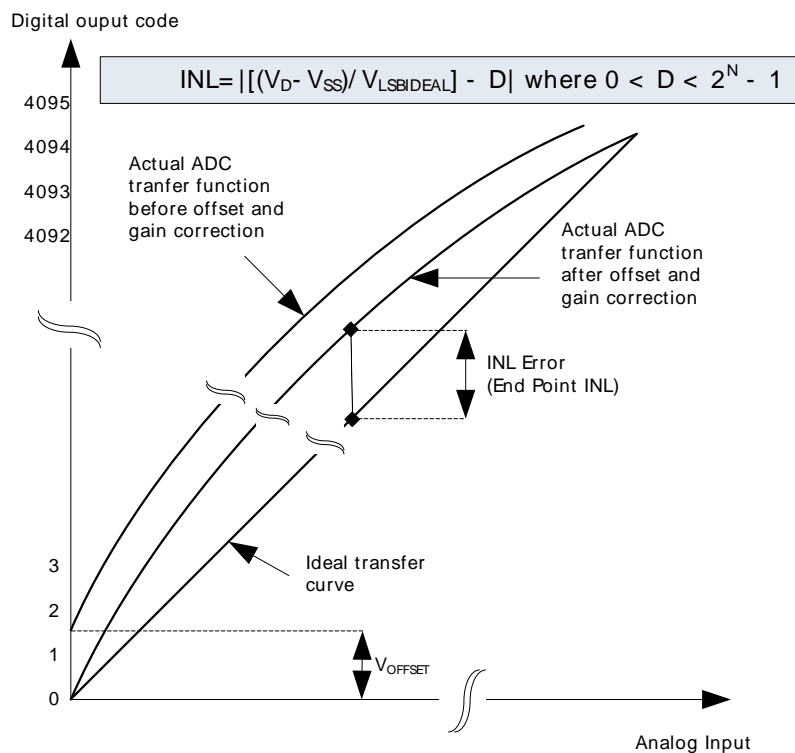
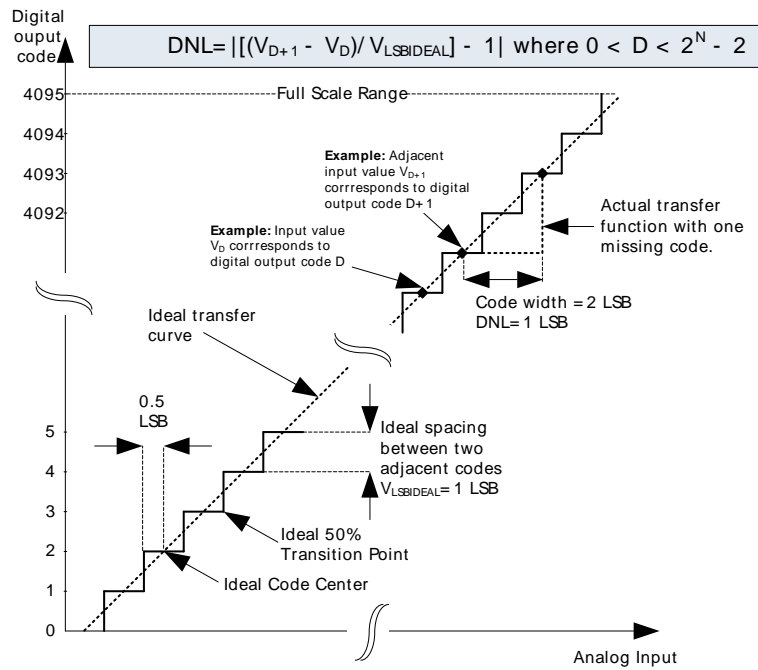


Figure 3.12. Differential Non-Linearity (DNL)



3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	External voltage reference, single ended	0		V_{DD}	V
		External voltage reference, differential	0		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400		μA
		100 kSamples/s, 12 bit		200		μA
		1 kSamples/s 12 bit NORMAL		38		μA
SR_{DAC}	DAC sample rate			500		ksamples/s
f_{DAC}	DAC clock frequency			1		MHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	DAC conversion time			2		μs
$t_{DACSETTLE}$	DAC settling time			5		μs
SNR_{DAC}	DAC Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		73		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		500 kSamples/s, 12 bit, differential, 5V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		73		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		100 kSamples/s, 12 bit, differential, 5V reference		73		dB
SNDR _{DAC}	DAC Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		70		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		69		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		72		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		71		dB
		500 kSamples/s, 12 bit, differential, 5V reference		71		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		72		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
100 kSamples/s, 12 bit, differential, 5V reference		72		dB		
SFDR _{DAC}	DAC Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		500 kSamples/s, 12 bit, differential, 5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, 5V reference		75		dB
V _{DACOFFSET}	Offset voltage	Before calibration, single ended		10		mV
		Before calibration, differential		10		mV
		After calibration, single ended		0.5		mV
		After calibration, differential		0.5		mV
DNL _{DAC}	Differential non-linearity	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
		5V reference		1		LSB
INL _{DAC}	Integral non-linearity	Internal 1.25V reference		2		LSB
		Internal 2.5V reference		2		LSB
		5V reference		2		LSB
MC _{DAC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 1.25V reference, differential		0		
		12 bit, internal 2.5V reference, single ended		0		
		12 bit, internal 2.5V reference, differential		0		
		12 bit, internal 5V reference, differential		0		

3.12 Analog Comparator (ACMP)

Table 3.16. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ACMPIN}	Input voltage range		0		V _{DD}	V
V _{ACMPCM}	ACMP Common Mode voltage range		0		V _{DD}	V
I _{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1		μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87		μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		μA
I _{ACMPREF}	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
V _{ACMPOFFSET}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{ACMPHYST}	ACMP hysteresis	Programmable		17		mV
R _{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 30) . I_{ACMPREF} is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \tag{3.1}$$

3.13 Voltage Comparator (VCMP)

Table 3.17. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMP_{CM}}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register		2.7		μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMP_{OFFSET}}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{VCMP_{HYST}}	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD \text{ Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.14 LCD

Table 3.18. LCD

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{LCDFR}	Frame rate		30		200	Hz
NUM _{SEG}	Number of segments supported			4x40		seg
V _{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I _{LCD}	Steady state current consumption.	Display disconnected, static mode, framerate 32 Hz, all segments on.		250		nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
I _{LCDBOOST}	Steady state Current contribution of internal boost.	Internal voltage boost off		0		μA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		μA
V _{BOOST}	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL0		3.0		V
		VBLEV of LCD_DISPCTRL register to LEVEL1		3.08		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.17		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.26		V
		VBLEV of LCD_DISPCTRL register to LEVEL4		3.34		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.43		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.52		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.6		V

The total LCD current is given by Equation 3.3 (p. 32) . I_{LCDBOOST} is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST} \tag{3.3}$$

3.15 Digital Peripherals

Table 3.19. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		7.5		μA/MHz
I _{UART}	UART current	UART idle current, clock enabled		5.63		μA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.25		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		μA/ MHz
I _{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		150		nA
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I _{LCD}	LCD current	LCD idle current, clock enabled		100		nA
I _{AES}	AES current	AES idle current, clock enabled		2.5		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		μA/ MHz
I _{EBI}	EBI current	EBI idle current, clock enabled		1.56		μA/ MHz
I _{PRS}	PRS current	PRS idle current		2,81		μA/ MHz
I _{DMA}	DMA current	Clock enable		8.12		μA/ MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32G Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32G890.

4.1 Pinout

The EFM32G890 pinout is shown in Figure 4.1 (p. 34) and Table 4.1 (p. 34). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32G890 Pinout (top view, not to scale)

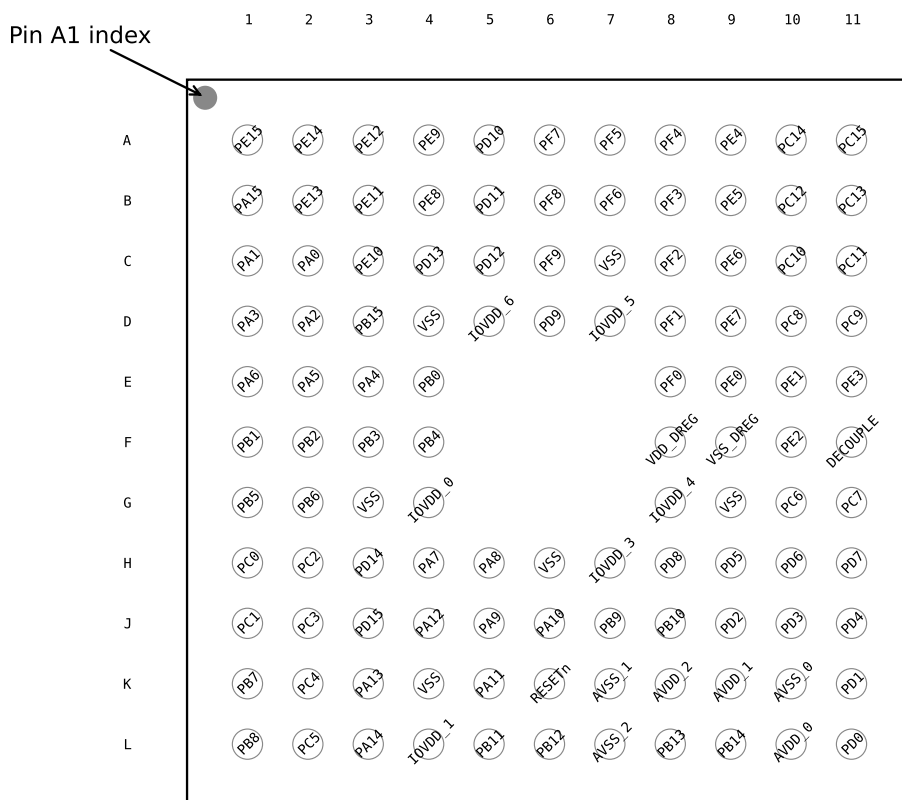


Table 4.1. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication	Other	
A1	PE15	LCD_SEG11	-	EBI_AD7	-	-	-	LEU0_RX #2	-	-
A2	PE14	LCD_SEG10	-	EBI_AD6	-	-	-	LEU0_TX #2	-	-
A3	PE12	LCD_SEG8	-	EBI_AD4	TIM1_CC2 #1	-	-	US0_CLK #0	-	-

BGA112 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
A4	PE9	LCD_SEG5	-	EBI_AD1	PCNT2_S1IN #1	-	-	-	-	-
A5	PD10	LCD_SEG29	-	EBI_CS1	-	-	-	-	-	-
A6	PF7	LCD_SEG25	-	-	TIM0_CC1 #2	-	-	U0_RX #0	-	-
A7	PF5	LCD_SEG3	-	EBI_REn	TIM0_CDTI2 #2	-	-	-	-	-
A8	PF4	LCD_SEG2	-	EBI_WEn	TIM0_CDTI1 #2	-	-	-	-	-
A9	PE4	LCD_COM0	-	-	-	-	-	US0_CS #1	-	-
A10	PC14	ACMP1_CH6	-	-	TIM0_CDTI1 #1/3	TIM1_CC1 #0	PCNT0_S1IN #0	U0_TX #3	-	-
A11	PC15	ACMP1_CH7	DBG_SWO #1	-	TIM0_CDTI2 #1/3	TIM1_CC2 #0	-	U0_RX #3	-	-
B1	PA15	LCD_SEG12	-	EBI_AD8	-	-	-	-	-	-
B2	PE13	LCD_SEG9	-	EBI_AD5	-	-	-	US0_CS #0	-	ACMP0_O #0
B3	PE11	LCD_SEG7	-	EBI_AD3	TIM1_CC1 #1	-	-	US0_RX #0	-	-
B4	PE8	LCD_SEG4	-	EBI_AD0	PCNT2_S0IN #1	-	-	-	-	-
B5	PD11	LCD_SEG30	-	EBI_CS2	-	-	-	-	-	-
B6	PF8	LCD_SEG26	-	-	TIM0_CC2 #2	-	-	-	-	-
B7	PF6	LCD_SEG24	-	-	TIM0_CC0 #2	-	-	U0_TX #0	-	-
B8	PF3	LCD_SEG1	-	EBI_ALE	TIM0_CDTI0 #2	-	-	-	-	-
B9	PE5	LCD_COM1	-	-	-	-	-	US0_CLK #1	-	-
B10	PC12	ACMP1_CH4	-	-	-	-	-	-	-	CMU_OUT0 #1
B11	PC13	ACMP1_CH5	-	-	TIM0_CDTI0 #1/3	TIM1_CC0 #0	PCNT0_S0IN #0	-	-	-
C1	PA1	LCD_SEG14	-	EBI_AD10	TIM0_CC1 #0/1	-	-	I2C0_SCL #0	-	CMU_OUT1 #0
C2	PA0	LCD_SEG13	-	EBI_AD9	TIM0_CC0 #0/1	-	-	I2C0_SDA #0	-	-
C3	PE10	LCD_SEG6	-	EBI_AD2	TIM1_CC0 #1	-	-	US0_TX #0	-	-
C4	PD13	-	-	-	-	-	-	-	-	-
C5	PD12	LCD_SEG31	-	EBI_CS3	-	-	-	-	-	-
C6	PF9	LCD_SEG27	-	-	-	-	-	-	-	-
C7	VSS	Ground								
C8	PF2	LCD_SEG0	DBG_SWO #0	EBI_ARDY	-	-	-	-	-	ACMP1_O #0
C9	PE6	LCD_COM2	-	-	-	-	-	US0_RX #1	-	-

BGA112 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
C10	PC10	ACMP1_CH2	-	-	TIM2_CC2 #2	-	-	US0_RX #2	-	-
C11	PC11	ACMP1_CH3	-	-	-	-	-	US0_TX #2	-	-
D1	PA3	LCD_SEG16	-	EBI_AD12	TIM0_CDTI0 #0	-	-	U0_TX #2	-	-
D2	PA2	LCD_SEG15	-	EBI_AD11	TIM0_CC2 #0/1	-	-	-	-	CMU_OUT0 #0
D3	PB15	-	-	-	-	-	-	-	-	-
D4	VSS	Ground								
D5	IOVDD_6	Digital IO power supply 6.								
D6	PD9	LCD_SEG28	-	EBI_CS0	-	-	-	-	-	-
D7	IOVDD_5	Digital IO power supply 5.								
D8	PF1	-	DBG_SWDIO #0/1	-	LETIM0_OUT1 #2	-	-	-	-	-
D9	PE7	LCD_COM3	-	-	-	-	-	US0_TX #1	-	-
D10	PC8	ACMP1_CH0	-	-	TIM2_CC0 #2	-	-	US0_CS #2	-	-
D11	PC9	ACMP1_CH1	-	-	TIM2_CC1 #2	-	-	US0_CLK #2	-	-
E1	PA6	LCD_SEG19	-	EBI_AD15	-	-	-	LEU1_RX #1	-	-
E2	PA5	LCD_SEG18	-	EBI_AD14	TIM0_CDTI2 #0	-	-	LEU1_TX #1	-	-
E3	PA4	LCD_SEG17	-	EBI_AD13	TIM0_CDTI1 #0	-	-	U0_RX #2	-	-
E4	PB0	LCD_SEG32	-	-	TIM1_CC0 #2	-	-	-	-	-
E8	PF0	-	DBG_SWCLK #0/1	-	LETIM0_OUT0 #2	-	-	-	-	-
E9	PE0	-	-	-	PCNT0_S0IN #1	-	-	U0_TX #1	-	-
E10	PE1	-	-	-	PCNT0_S1IN #1	-	-	U0_RX #1	-	-
E11	PE3	-	-	-	-	-	-	-	-	ACMP1_O #1
F1	PB1	LCD_SEG33	-	-	TIM1_CC1 #2	-	-	-	-	-
F2	PB2	LCD_SEG34	-	-	TIM1_CC2 #2	-	-	-	-	-
F3	PB3	LCD_SEG20	-	-	PCNT1_S0IN #1	-	-	US2_TX #1	-	-
F4	PB4	LCD_SEG21	-	-	PCNT1_S1IN #1	-	-	US2_RX #1	-	-
F8	VDD_DREG	Power supply for on-chip voltage regulator.								
F9	VSS_DREG	Ground for on-chip voltage regulator.								
F10	PE2	-	-	-	-	-	-	-	-	ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator, nominally at 1.8 V. An external capacitance of size C _{DECOUPLE} is required at this pin.								

BGA112 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
G1	PB5	LCD_SEG22	-	-	-	-	-	US2_CLK #1	-	-
G2	PB6	LCD_SEG23	-	-	-	-	-	US2_CS #1	-	-
G3	VSS	Ground								
G4	IOVDD_0	Digital IO power supply 0.								
G8	IOVDD_4	Digital IO power supply 4.								
G9	VSS	Ground								
G10	PC6	ACMP0_CH6	-	-	-	-	-	LEU1_TX #0	I2C0_SDA #2	-
G11	PC7	ACMP0_CH7	-	-	-	-	-	LEU1_RX #0	I2C0_SCL #2	-
H1	PC0	ACMP0_CH0	-	-	PCNT0_S0IN #2	-	-	US1_TX #0	-	-
H2	PC2	ACMP0_CH2	-	-	-	-	-	US2_TX #0	-	-
H3	PD14	-	-	-	-	-	-	I2C0_SDA #3	-	-
H4	PA7	LCD_SEG35	-	-	-	-	-	-	-	-
H5	PA8	LCD_SEG36	-	-	TIM2_CC0 #0	-	-	-	-	-
H6	VSS	Ground								
H7	IOVDD_3	Digital IO power supply 3.								
H8	PD8	-	-	-	-	-	-	-	-	CMU_OUT1 #1
H9	PD5	ADC0_CH5	-	-	-	-	-	LEU0_RX #0	-	-
H10	PD6	ADC0_CH6	-	-	LETIM0_OUT0 #0	-	-	I2C0_SDA #1	-	-
H11	PD7	ADC0_CH7	-	-	LETIM0_OUT1 #0	-	-	I2C0_SCL #1	-	-
J1	PC1	ACMP0_CH1	-	-	PCNT0_S1IN #2	-	-	US1_RX #0	-	-
J2	PC3	ACMP0_CH3	-	-	-	-	-	US2_RX #0	-	-
J3	PD15	-	-	-	-	-	-	I2C0_SCL #3	-	-
J4	PA12	LCD_BCAP_P	-	-	TIM2_CC0 #1	-	-	-	-	-
J5	PA9	LCD_SEG37	-	-	TIM2_CC1 #0	-	-	-	-	-
J6	PA10	LCD_SEG38	-	-	TIM2_CC2 #0	-	-	-	-	-
J7	PB9	-	-	-	-	-	-	-	-	-
J8	PB10	-	-	-	-	-	-	-	-	-
J9	PD2	ADC0_CH2	-	-	TIM0_CC1 #3	-	-	US1_CLK #1	-	-
J10	PD3	ADC0_CH3	-	-	TIM0_CC2 #3	-	-	US1_CS #1	-	-

BGA112 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
J11	PD4	ADC0_CH4	-	-	-	-	-	LEU0_TX #0	-	-
K1	PB7	LFXTAL_P	-	-	-	-	-	US1_CLK #0	-	-
K2	PC4	ACMP0_CH4	-	-	LETIM0_OUT0 #3	PCNT1_S0IN #0	-	US2_CLK #0	-	-
K3	PA13	LCD_BCAP_N	-	-	TIM2_CC1 #1	-	-	-	-	-
K4	VSS	Ground								
K5	PA11	LCD_SEG39	-	-	-	-	-	-	-	-
K6	RESETn	Reset input. Active low, with internal pull-up.								
K7	AVSS_1	Analog ground 1.								
K8	AVDD_2	Analog power supply 2.								
K9	AVDD_1	Analog power supply 1.								
K10	AVSS_0	Analog ground 0.								
K11	PD1	ADC0_CH1	-	-	TIM0_CC0 #3	PCNT2_S1IN #0	-	US1_RX #1	-	-
L1	PB8	LFXTAL_N	-	-	-	-	-	US1_CS #0	-	-
L2	PC5	ACMP0_CH5	-	-	LETIM0_OUT1 #3	PCNT1_S1IN #0	-	US2_CS #0	-	-
L3	PA14	LCD_BEXT	-	-	TIM2_CC2 #1	-	-	-	-	-
L4	IOVDD_1	Digital IO power supply 1.								
L5	PB11	DAC0_OUT0	-	-	LETIM0_OUT0 #1	-	-	-	-	-
L6	PB12	DAC0_OUT1	-	-	LETIM0_OUT1 #1	-	-	-	-	-
L7	AVSS_2	Analog ground 2.								
L8	PB13	HFXTAL_P	-	-	-	-	-	LEU0_TX #1	-	-
L9	PB14	HFXTAL_N	-	-	-	-	-	LEU0_RX #1	-	-
L10	AVDD_0	Analog power supply 0.								
L11	PD0	ADC0_CH0	-	-	PCNT2_S0IN #0	-	-	US1_TX #1	-	-

4.2 Alternate functionality pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 39). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate Functionality	LOCATION				Description
	0	1	2	3	
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
CMU_OUT0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_OUT1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD0	PE8				External Bus Interface (EBI) address and data input / output pin 0.
EBI_AD1	PE9				External Bus Interface (EBI) address and data input / output pin 1.
EBI_AD2	PE10				External Bus Interface (EBI) address and data input / output pin 2.
EBI_AD3	PE11				External Bus Interface (EBI) address and data input / output pin 3.

Alternate	LOCATION				Description
	0	1	2	3	
EBI_AD4	PE12				External Bus Interface (EBI) address and data input / output pin 4.
EBI_AD5	PE13				External Bus Interface (EBI) address and data input / output pin 5.
EBI_AD6	PE14				External Bus Interface (EBI) address and data input / output pin 6.
EBI_AD7	PE15				External Bus Interface (EBI) address and data input / output pin 7.
EBI_AD8	PA15				External Bus Interface (EBI) address and data input / output pin 8.
EBI_AD9	PA0				External Bus Interface (EBI) address and data input / output pin 9.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal (4 - 32 MHz) negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal (4 - 32 MHz) positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD driver segment line number 0.
LCD_SEG1	PF3				LCD driver segment line number 1.
LCD_SEG2	PF4				LCD driver segment line number 2.
LCD_SEG3	PF5				LCD driver segment line number 3.
LCD_SEG4	PE8				LCD driver segment line number 4.

Alternate Functionality	LOCATION				Description
	0	1	2	3	
LCD_SEG5	PE9				LCD driver segment line number 5.
LCD_SEG6	PE10				LCD driver segment line number 6.
LCD_SEG7	PE11				LCD driver segment line number 7.
LCD_SEG8	PE12				LCD driver segment line number 8.
LCD_SEG9	PE13				LCD driver segment line number 9.
LCD_SEG10	PE14				LCD driver segment line number 10.
LCD_SEG11	PE15				LCD driver segment line number 11.
LCD_SEG12	PA15				LCD driver segment line number 12.
LCD_SEG13	PA0				LCD driver segment line number 13.
LCD_SEG14	PA1				LCD driver segment line number 14.
LCD_SEG15	PA2				LCD driver segment line number 15.
LCD_SEG16	PA3				LCD driver segment line number 16.
LCD_SEG17	PA4				LCD driver segment line number 17.
LCD_SEG18	PA5				LCD driver segment line number 18.
LCD_SEG19	PA6				LCD driver segment line number 19.
LCD_SEG20	PB3				LCD driver segment line number 20.
LCD_SEG21	PB4				LCD driver segment line number 21.
LCD_SEG22	PB5				LCD driver segment line number 22.
LCD_SEG23	PB6				LCD driver segment line number 23.
LCD_SEG24	PF6				LCD driver segment line number 24.
LCD_SEG25	PF7				LCD driver segment line number 25.
LCD_SEG26	PF8				LCD driver segment line number 26.
LCD_SEG27	PF9				LCD driver segment line number 27.
LCD_SEG28	PD9				LCD driver segment line number 28.
LCD_SEG29	PD10				LCD driver segment line number 29.
LCD_SEG30	PD11				LCD driver segment line number 30.
LCD_SEG31	PD12				LCD driver segment line number 31.
LCD_SEG32	PB0				LCD driver segment line number 32.
LCD_SEG33	PB1				LCD driver segment line number 33.
LCD_SEG34	PB2				LCD driver segment line number 34.
LCD_SEG35	PA7				LCD driver segment line number 35.
LCD_SEG36	PA8				LCD driver segment line number 36.
LCD_SEG37	PA9				LCD driver segment line number 37.
LCD_SEG38	PA10				LCD driver segment line number 38.
LCD_SEG39	PA11				LCD driver segment line number 39.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.

Alternate	LOCATION				Description
	0	1	2	3	
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION				Description
	0	1	2	3	
US2_TX	PC2	PB3			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO pinout overview

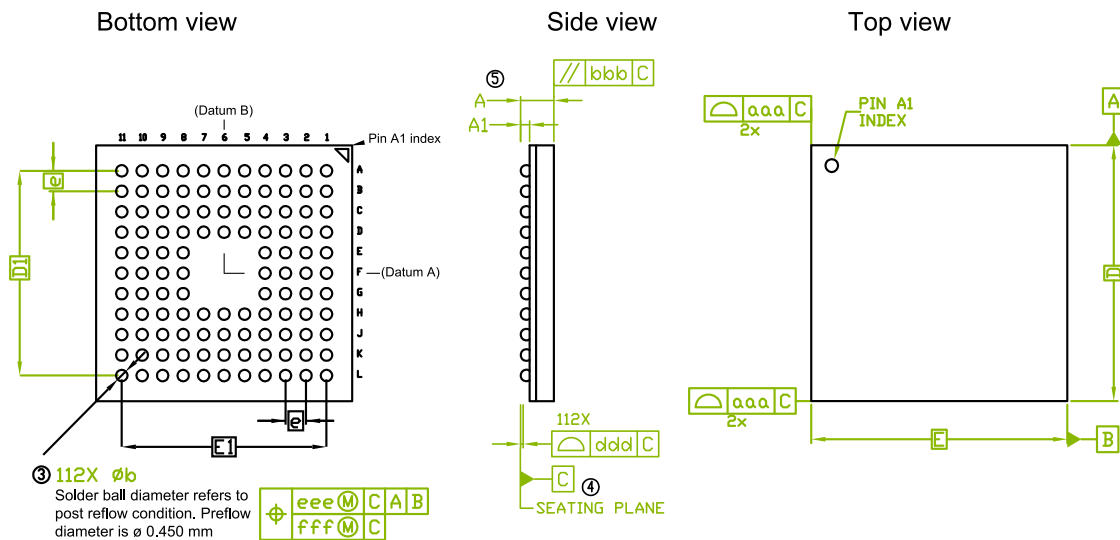
The specific GPIO pins available in *EFM32G890* is shown in Table 4.3 (p. 43). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 BGA112 Package

Figure 4.2. BGA112



Rev: P-5134-10.0x10.0-112(T)-A1-r0_05Aug09

1. All dimensions are in millimeters.
2. 'e' represents the basic solder ball grid pitch.
3. Dimension 'b' is measurable at the maximum ball diameter, parallel to primary datum 'C'.
4. Primary datum 'C' and seating plane are defined by the spherical crowns of the contact balls.
5. Dimension 'A' includes standoff height 'A1', package body thickness and lip height, but does not include attach features.
6. Package dimensions take reference to JEDEC MO-275 rev. A.

Table 4.4. BGA112 (Dimensions in mm)

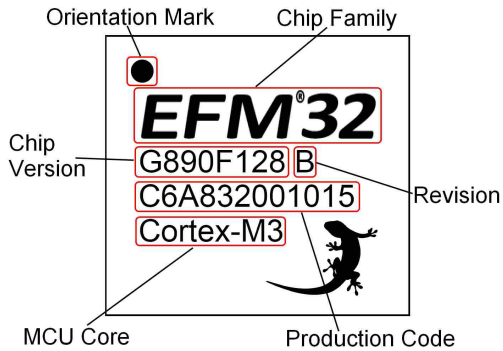
Symbol	A	A1	b	D	E	D1	E1	e	aaa	bbb	ddd	eee	fff
Min	1.22	0.30	0.42	10.00	10.00	8.00	8.00	0.80	0.15	0.20	0.12	0.15	0.08
Nom	1.30	0.35	0.47										
Max	1.38	0.40	0.52										

5 Chip Marking, Revision and Errata

5.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 5.1. BGA112 Chip Marking



5.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 5.1 (p. 45). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as specified in the reference manual.

5.3 Errata

Please see the [dxxxx_EFM32G890_errata.pdf](#) for description and resolution of device erratas.

6 Revision History

6.1 Revision 1.00

April 23rd, 2010

ADC_VCM line removed.

Added pinout illustration and additional pinout table.

Changed "Errata" chapter. Errata description moved to separate document.

Document changed status from "Preliminary".

Updated "Electrical Characteristics" chapter.

6.2 Revision 0.85

February 19th, 2010

Renamed DBG_SWV pin to DBG_SWO.

6.3 Revision 0.83

January 25th, 2010

Updated errata section.

Specified flash word width in Section 3.7 (p. 20)

Added Capacitive Sense Internal Resistor values in Section 3.12 (p. 30) .

6.4 Revision 0.82

December 9th, 2009

Updated contact information.

ADC current consumption numbers updated in Section 3.10 (p. 23)

Updated LCD supply voltage range in Section 3.14 (p. 32)

6.5 Revision 0.81

November 20th, 2009

Section 3.1 (p. 9) updated.

Storage temperature in Section 3.2 (p. 9) updated.

Temperature coefficient of band-gap reference in Section 3.6 (p. 19) added.

Erase times in Section 3.7 (p. 20) updated.

Definitions of DNL and INL added in Figure 3.11 (p. 26) and Figure 3.12 (p. 27) .

Section 3.14 (p. 32) added.

Current consumption of digital peripherals added in Section 3.15 (p. 32) .

Pinout information in Table 4.1 (p. 34) corrected.

Updated errata section.

6.6 Revision 0.80

Initial preliminary revision, October 19th, 2009

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Table of Contents

1. Ordering Information	2
1.1. Block Diagram	2
2. System Summary	3
2.1. System Introduction	3
2.2. Configuration Summary	6
2.3. Memory Map	7
3. Electrical Characteristics	9
3.1. Test Conditions	9
3.2. Absolute Maximum Ratings	9
3.3. General Operating Conditions	9
3.4. Current Consumption	10
3.5. Transition between Energy Modes	19
3.6. Power Management	19
3.7. Flash	20
3.8. General Purpose Input Output	20
3.9. Oscillators	21
3.10. Analog Digital Converter (ADC)	23
3.11. Digital Analog Converter (DAC)	27
3.12. Analog Comparator (ACMP)	30
3.13. Voltage Comparator (VCMP)	31
3.14. LCD	32
3.15. Digital Peripherals	32
4. Pinout and Package	34
4.1. Pinout	34
4.2. Alternate functionality pinout	38
4.3. GPIO pinout overview	43
4.4. BGA112 Package	43
5. Chip Marking, Revision and Errata	45
5.1. Chip Marking	45
5.2. Revision	45
5.3. Errata	45
6. Revision History	46
6.1. Revision 1.00	46
6.2. Revision 0.85	46
6.3. Revision 0.83	46
6.4. Revision 0.82	46
6.5. Revision 0.81	46
6.6. Revision 0.80	47
A. Disclaimer and Trademarks	48
A.1. Disclaimer	48
A.2. Trademark Information	48
B. Contact Information	49
B.1. Energy Micro Corporate Headquarters	49
B.2. Global Contacts	49

List of Figures

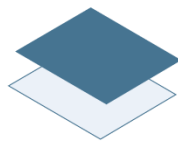
1.1. Block Diagram	2
2.1. <i>EFM32G890</i> Memory Map with largest RAM and Flash sizes	8
3.1. EM0 Current consumption vs supply voltage, executing prime number calculation code from flash with HFRCO running at 28MHz	11
3.2. EM0 Current consumption vs temperature, executing prime number calculation code from flash with HFRCO running at 28MHz	12
3.3. EM1 Current consumption vs supply voltage, all peripheral clocks disabled, HFRCO running at 28MHz	13
3.4. EM1 Current consumption vs temperature, all peripheral clocks disabled, HFRCO running at 28MHz	14
3.5. EM2 Current consumption vs supply voltage. RTC incremented each second, RTC prescaled to 1kHz, 32 kHz LFRCO.	15
3.6. EM2 Current consumption vs temperature. RTC incremented each second, RTC prescaled to 1kHz, 32 kHz LFRCO.	16
3.7. EM3 Current consumption vs supply voltage	17
3.8. EM3 Current consumption vs temperature	17
3.9. EM4 Current consumption vs supply voltage	18
3.10. EM4 Current consumption vs temperature	18
3.11. Integral Non-Linearity (INL)	26
3.12. Differential Non-Linearity (DNL)	27
4.1. <i>EFM32G890</i> Pinout (top view, not to scale)	34
4.2. BGA112	43
5.1. BGA112 Chip Marking	45

List of Tables

1.1. Ordering Information	2
2.1. Configuration Summary	6
3.1. Absolute Maximum Ratings	9
3.2. General Operating Conditions	9
3.3. Environmental	10
3.4. Current Consumption	10
3.5. Energy Modes Transitions	19
3.6. Power Management	19
3.7. Flash	20
3.8. GPIO	20
3.9. LFXO	21
3.10. HFXO	21
3.11. LFRCO	22
3.12. HFRCO	22
3.13. ULFRCO	22
3.14. ADC	23
3.15. DAC	27
3.16. ACMP	30
3.17. VCMP	31
3.18. LCD	32
3.19. Digital Peripherals	32
4.1. Device Pinout	34
4.2. Alternate functionality overview	39
4.3. GPIO Pinout	43
4.4. BGA112 (Dimensions in mm)	44

List of Equations

3.1. Total ACMP Active Current	30
3.2. VCMP Trigger Level as a Function of Level Setting	31
3.3. Total LCD Current Based on Operational Mode and Internal Boost	32



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