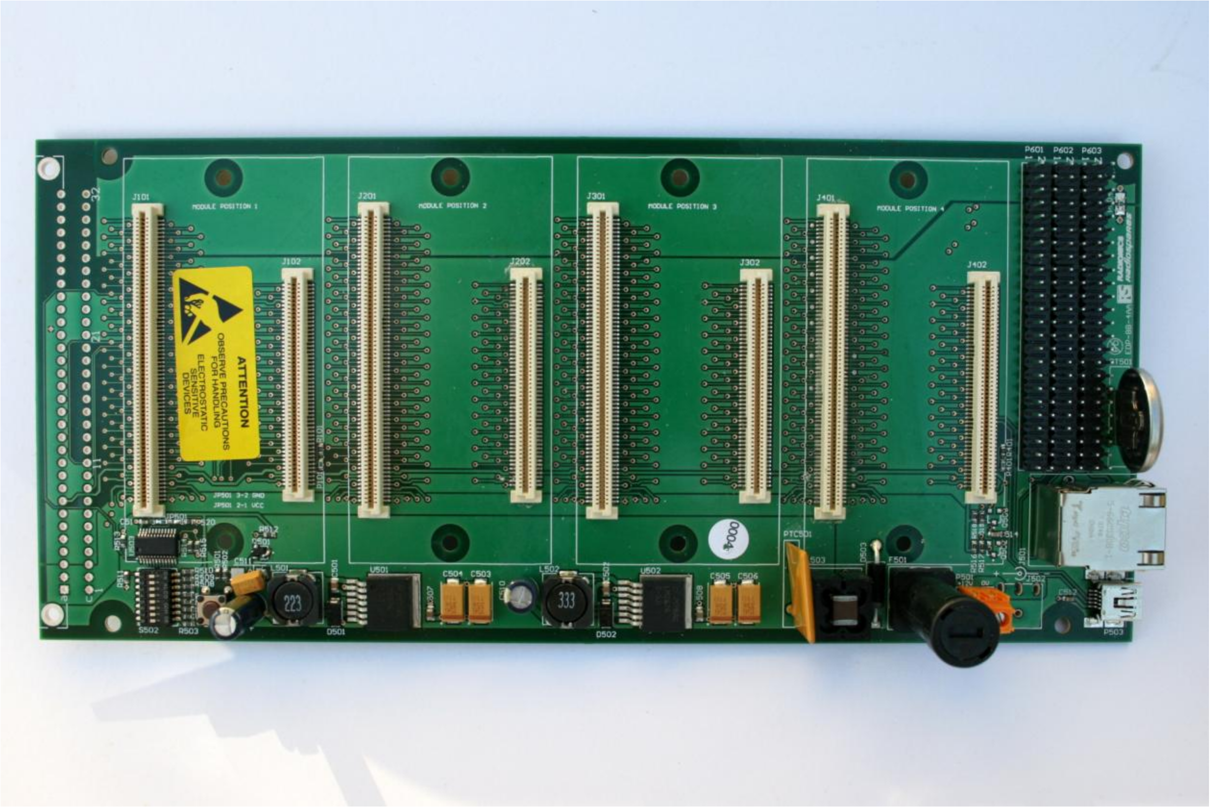


Embedded Development Platform

EDP Baseboard EDP-BB-4A User Manual

Contents

1. The EDP System

1.1 Introduction

1.1.1 EDP Baseboard

The EDP Baseboard (or “motherboard”) consists of 4 ‘stations’ with the minimum configuration of the motherboard with a single plug-in processor module. All 4 stations are identical, and there are many permutations of CPU modules and Application modules possible. Even with just the minimum configuration of Motherboard and CPU module for example, you can easily run a web-server through the standard onboard Ethernet connection. There are various application modules; we have introduced an initial starter range consisting of basic digital and analogue I/O, a motor control module and a communications module. The more advanced user will discover that it is possible to run more than one processor module on the motherboard in a Master and Slave configuration.

The motherboard is an Extended Euro card size (220 x 100 mm) fitted with rubber feet to lay flat on the bench, but able to be used in a standard rack system. Add a 64-way DIN (RS 381-8696) connector and you can plug the EDP into a backplane. Connectors for four module stations are supplied, arranged to ensure correct module fitting. There are also fitted +3.3V and +5V voltage regulators, a back-up battery, an RJ45 Ethernet connector, a mini-USB connector, +12 volt power-supply jack, I/O breakout header and eight DIP switches ported onto the system I^2C bus.

The DIP switches allow the user software running on a processor module to read a configuration setting, enabling I/O ports to be set up correctly, for example, or for CAN or TCP/IP addresses to be set. Depending on the capability of the particular processor module in use, up to three I^2C buses and two CAN networks are available. Many of the application modules use an I^2C bus for primary communication with the processor providing maximum flexibility. Some processor chips will require +5 volts, others +3.3 volts. A factory link on the module selects the correct supply from the connector. This supply is linked to a further connector pin on all the other module stations providing a correct voltage reference or bus pull-up for the application modules.

1.1.2 Reusable Components

The EDP baseboard is designed to be used and reused with new CPU and application modules being introduced on a regular basis. Its robust design has been rigorously tested, and every effort has been made at the design stage to protect the EDP from the most common human errors: the motherboard will have a significantly longer life than the average development board and is suitable for use in specialist one-off and low-volume products. Typical applications might be industrial controllers, scientific instrument controllers, data-logging and remote monitoring. For these reasons the EDP will prove attractive to all design engineers looking for a cost effective solution which allows them to significantly improve their development process and thus deliver products in reduced time. Design engineers, consultants, educators and trainers will quickly realise the benefits and recognise the potential of the development platform modules system as an effective solution.

1.1.3 Bread-Boarding Platform

With the difficulty in applying traditional “bread-boarding” techniques to today’s tiny SMT components, evaluating new active devices has become major problem. There is usually no alternative to creating a special “try-out” PCB using rapid PCB production houses just to get a new device up and running.

The EDP has been designed to host such experimental and trial designs, providing “clean” +5 and +3V3 supplies and instant access to a range of standard microcontrollers and I/O blocks and devices. The design information necessary to allow you to create your own module for experimenting with new devices is available free of charge but in many cases, RS will already have such a module available to save you the effort.

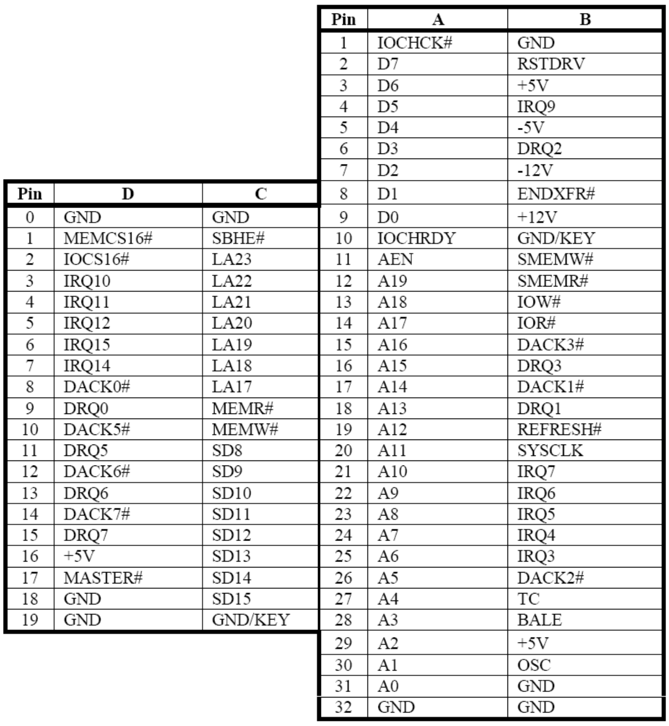
The EDP represents the start of a continuous launch process which will see the introduction of new processor and application modules on a monthly basis.

1.2 EDP Modules Available Now

Processor Module: ST Microelectronics STR912
Processor Module: Infineon XC167
Application Module: Analogue Input
Application Module: Digital Input/Output
Application Module: Brushed DC Motor Control
Application Module: Basic Communications

1.3 Basic EDP Concepts

The EDP allows microcontrollers and I/O devices to communicate through a standardised interface. To some extent this interface is analogous to PC104 or STE busses where a connector pin-out is defined that allows the interconnection of address and data-bus connected devices. Such busses tend to include only power line, data and address busses plus control signals such as chip selects and interrupt request lines.



Pin	D	C
0	GND	GND
1	MEMCS16#	SBHE#
2	IOCS16#	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	DACK0#	LA17
9	DRQ0	MEMR#
10	DACK5#	MEMW#
11	DRQ5	SD8
12	DACK6#	SD9
13	DRQ6	SD10
14	DACK7#	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER#	SD14
18	GND	SD15
19	GND	GND/KEY

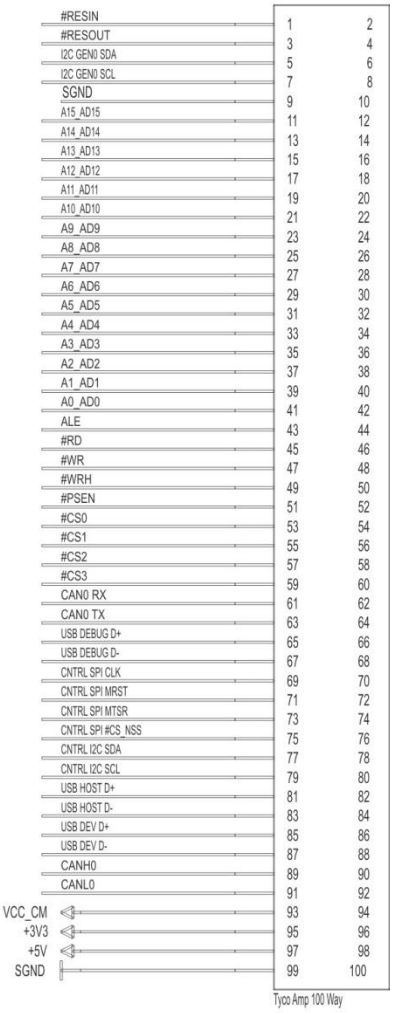
Pin	A	B
1	IOCHCK#	GND
2	D7	RSTDRV
3	D6	+5V
4	D5	IRQ9
5	D4	-5V
6	D3	DRQ2
7	D2	-12V
8	D1	ENDXFR#
9	D0	+12V
10	IOCHRDY	GND/KEY
11	AEN	SMEMW#
12	A19	SMEMR#
13	A18	IOW#
14	A17	IOR#
15	A16	DACK3#
16	A15	DRQ3
17	A14	DACK1#
18	A13	DRQ1
19	A12	REFRESH#
20	A11	SYSCLK
21	A10	IRQ7
22	A9	IRQ6
23	A8	IRQ5
24	A7	IRQ4
25	A6	IRQ3
26	A5	DACK2#
27	A4	TC
28	A3	BALE
29	A2	+5V
30	A1	OSC
31	A0	GND
32	GND	GND

For microcontroller systems, such a collection of signals is of very limited use, especially for single-chip CPUs that use no external bus. It also takes no account of the specialist pin functions available on microcontrollers such as CAN, I^2C, SPI, signal measurement and signal generation peripherals.

1.3.1 Standardised Signal Set for Embedded Microcontrollers

The EDPCON1 and 2 connectors thus defines a set of signals on a standardised format that are relevant to typical 8, 16 and 32-bit microcontrollers. In addition to address bus, data bus and chip select signals, they include three I^{2}C channels, two CAN channels, groups of pins able to create interrupts in response to external events, groups of pins able to create pulse-trains, others dedicated to motor control, I^{2}S, memory cards and many other common microcontroller I/O types.

All of these signals are contained within two 0.8mm dual-row connectors of 140 and 100 pins each.

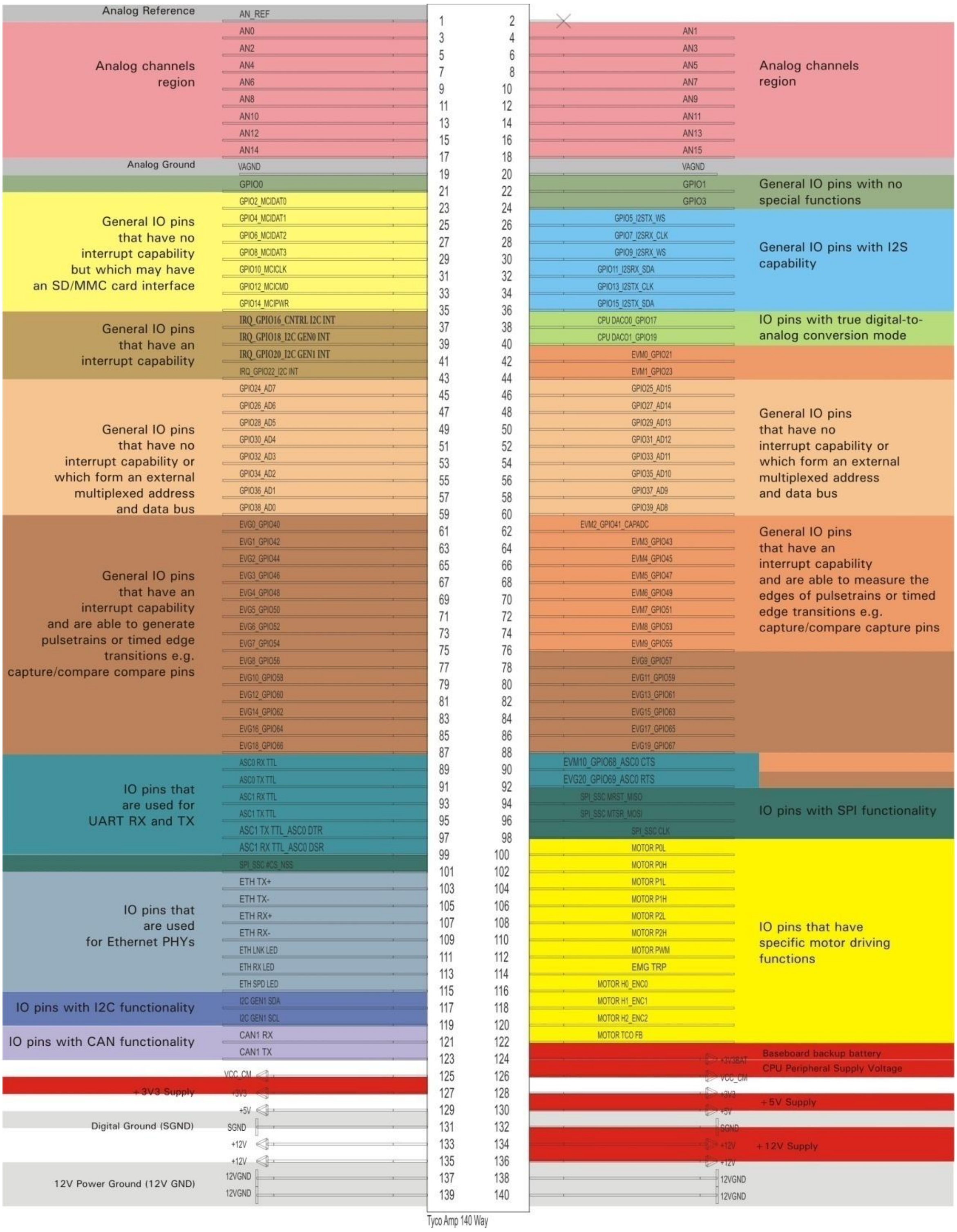


1.3.2 Grouping of Signals on the EDP Connectors

The EDPCON1 and 2 connector specification divide the total available 240 pins into groups or regions of similar characteristics, as shown below:

1.3.2.1 EDPCON1 Connector I/O Regions

EDPCON1 carries both analogue and digital signals. The analogue signals are grouped together in a “quiet zone”.

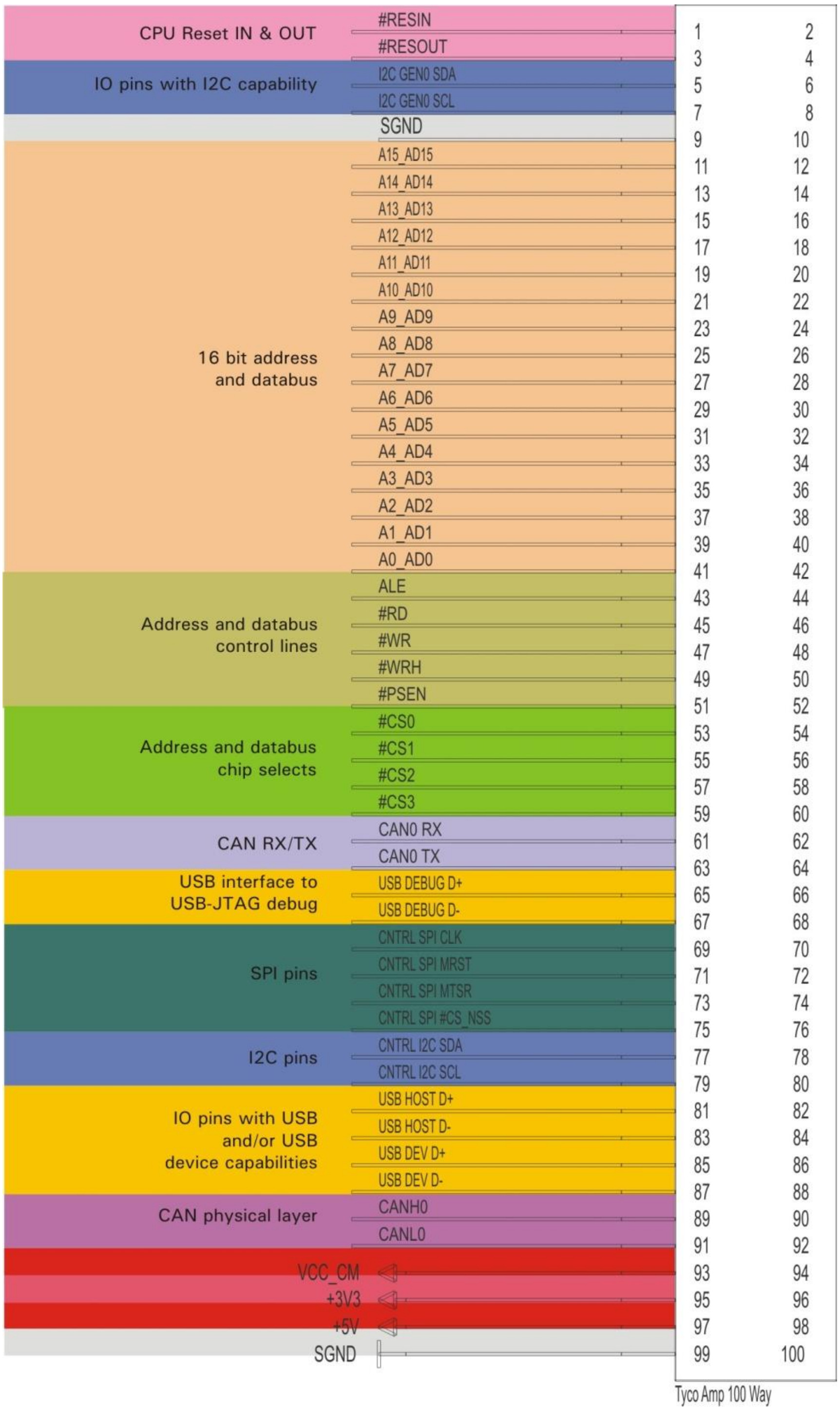


Region	Signal	Pin	Pin	Signal	Region
Analog Reference	AN_REF	1	2		
Analog channels region	AN0	3	4	AN1	Analog channels region
	AN2	5	6	AN3	
	AN4	7	8	AN5	
	AN6	9	10	AN7	
	AN8	11	12	AN9	
	AN10	13	14	AN11	
	AN12	15	16	AN13	
	AN14	17	18	AN15	
Analog Ground	VAGND	19	20	VAGND	
	GPIO0	21	22	GPIO1	General IO pins with no special functions
General IO pins that have no interrupt capability but which may have an SD/MMC card interface	GPIO2_MCIDAT0	23	24	GPIO3	
	GPIO4_MCIDAT1	25	26	GPIO5_I2STX_WS	General IO pins with I2S capability
	GPIO6_MCIDAT2	27	28	GPIO7_I2SRX_CLK	
	GPIO8_MCIDAT3	29	30	GPIO9_I2SRX_WS	
	GPIO10_MCICLK	31	32	GPIO11_I2SRX_SDA	
	GPIO12_MCICMD	33	34	GPIO13_I2STX_CLK	
	GPIO14_MCIPWR	35	36	GPIO15_I2STX_SDA	
General IO pins that have an interrupt capability	IRQ_GPIO16_CNTRL I2C INT	37	38	CPU DACO0_GPIO17	IO pins with true digital-to-analog conversion mode
	IRQ_GPIO18_I2C GEN0 INT	39	40	CPU DACO1_GPIO19	
	IRQ_GPIO20_I2C GEN1 INT	41	42	EVM0_GPIO21	
	IRQ_GPIO22_I2C INT	43	44	EVM1_GPIO23	
General IO pins that have no interrupt capability or which form an external multiplexed address and data bus	GPIO24_AD7	45	46	GPIO25_AD15	General IO pins that have no interrupt capability or which form an external multiplexed address and data bus
	GPIO26_AD6	47	48	GPIO27_AD14	
	GPIO28_AD5	49	50	GPIO29_AD13	
	GPIO30_AD4	51	52	GPIO31_AD12	
	GPIO32_AD3	53	54	GPIO33_AD11	
	GPIO34_AD2	55	56	GPIO35_AD10	
	GPIO36_AD1	57	58	GPIO37_AD9	
	GPIO38_AD0	59	60	GPIO39_AD8	
General IO pins that have an interrupt capability and are able to generate pulsetrains or timed edge transitions e.g. capture/compare compare pins	EVG0_GPIO40	61	62	EVM2_GPIO41_CAPADC	General IO pins that have an interrupt capability and are able to measure the edges of pulsetrains or timed edge transitions e.g. capture/compare capture pins
	EVG1_GPIO42	63	64	EVM3_GPIO43	
	EVG2_GPIO44	65	66	EVM4_GPIO45	
	EVG3_GPIO46	67	68	EVM5_GPIO47	
	EVG4_GPIO48	69	70	EVM6_GPIO49	
	EVG5_GPIO50	71	72	EVM7_GPIO51	
	EVG6_GPIO52	73	74	EVM8_GPIO53	
	EVG7_GPIO54	75	76	EVM9_GPIO55	
	EVG8_GPIO56	77	78	EVG9_GPIO57	
	EVG10_GPIO58	79	80	EVG11_GPIO59	
	EVG12_GPIO60	81	82	EVG13_GPIO61	
	EVG14_GPIO62	83	84	EVG15_GPIO63	
	EVG16_GPIO64	85	86	EVG17_GPIO65	
	EVG18_GPIO66	87	88	EVG19_GPIO67	
IO pins that are used for UART RX and TX	ASC0 RX TTL	89	90	EVM10_GPIO68_ASC0 CTS	
	ASC0 TX TTL	91	92	EVG20_GPIO69_ASC0 RTS	
	ASC1 RX TTL	93	94	SPI_SSC MRST_MISO	IO pins with SPI functionality
	ASC1 TX TTL	95	96	SPI_SSC MTSR_MOSI	
	ASC1 TX TTL_ASC0 DTR	97	98	SPI_SSC CLK	
	ASC1 RX TTL_ASC0 DSR	99	100	MOTOR P0L	IO pins that have specific motor driving functions
	SPI_SSC #CS_NSS	101	102	MOTOR P0H	
IO pins that are used for Ethernet PHYs	ETH TX+	103	104	MOTOR P1L	
	ETH TX-	105	106	MOTOR P1H	
	ETH RX+	107	108	MOTOR P2L	
	ETH RX-	109	110	MOTOR P2H	
	ETH LNK LED	111	112	MOTOR PWM	
	ETH RX LED	113	114	EMG TRP	
	ETH SPD LED	115	116	MOTOR H0_ENC0	
IO pins with I2C functionality	I2C GEN1 SDA	117	118	MOTOR H1_ENC1	
	I2C GEN1 SCL	119	120	MOTOR H2_ENC2	
IO pins with CAN functionality	CAN1 RX	121	122	MOTOR TCO FB	
	CAN1 TX	123	124	+3V3BAT	Baseboard backup battery
	VCC_CM	125	126	VCC_CM	CPU Peripheral Supply Voltage
+3V3 Supply	+3V3	127	128	+3V3	
	+5V	129	130	+5V	+5V Supply
Digital Ground (SGND)	SGND	131	132	SGND	
	+12V	133	134	+12V	+12V Supply
	+12V	135	136	+12V	
12V Power Ground (12V GND)	12VGND	137	138	12VGND	
	12VGND	139	140	12VGND	

Tyco Amp 140 Way

1.3.2.2 EDPCON2 Connector Regions

EDPCON2 carries mainly bus signals such as I^{2}C, SPI, CAN and the multiplexed 16-bit external bus from the CPU module.



1.3.3 EDP Signal Names

The generic signals present on the connectors have names which indicate their primary and secondary functions.

1.3.3.1 EDPCON1 Signal Description

ANx:	Analogue signals
VAGND:	Analogue ground, referenced to CPU and Analogue application analogue signal grounds
GPIOx:	Pins that can only be set to 1 or 0 by a CPU instruction. It has no special or alternate function.
GPIOx_MCIxxx:	Pins that have basic I/O function like “GPIOx” but which also form an SM/MMC card interface
GPIOx_I2S_XXX:	Pins that have basic I/O function like “GPIOx” but which also form an I2S interface.
IRQx_GPIOx_X_I2C_INT:	Pins that are used by the three I^{2}C busses to request a CPU interrupt. **Note:** IRQ_GPIO16_CNTRL_I2C_INT should always be reserved for use by the I^{2}C CNTRL I2C bus.
CPU_DACx_GPIOx:	Pins where CPUs with true digital to analogue converter outputs are always connected. Alternatively, PWM will be available if there is no DAC.
EVMx_GPIOx:	Pins which have basic I/O function but which also can measure timed events, pulse times and durations e.g. CAPCOM input.
GPIOx_ADx:	Pins with basic I/O function but which also can form a multiplexed address and data bus.
EVGx_GPIOx:	Pins which have basic I/O function but which also can generate events like timed pulses and transitions e.g. CAPCOM output.
EVM2_GPIO41_CAPADC:	Pins which have basic I/O function but which also can measure pulse times and durations e.g. CAPCOM input. If the CPU supports the triggering of ADC readings on an edge, the function will be on this pin.
ASC0_RX_TTL:	Logic level connection to CPU module’s serial port 0 receive pin.
ASC0_TX_TTL:	Logic level connection to CPU module’s serial port 0 transmit pin.
ASC1_RX_TTL:	Logic level connection to CPU module’s serial port 1 receive pin.
ASC1_TX_TTL:	Logic level connection to CPU module’s serial port 1 transmit pin.
ASC1_TX_TTL_ASC0_DTR:	If CPU supports DTR function on ASC0, the function is available here.
ASC1_RX_TTL_ASC0_DSR:	If CPU supports DSR function on ASC0, the function is available here.
EVM_GPIOx_ASC0_xTS:	Event measurement, general I/O and ASC0 RTS and CTS functions, where available.
SPI_XXXX:	Pins associated with SPI function, where supported by CPU module.
ETH_xxx:	Pins connected to an Ethernet PHY on CPU module, where available.
I2C_GEN1_SDA/SCL:	Pins connected to CPU’s I^{2}C channel 1
MOTOR_XXXX:	Pins required for driving three-phase AC and DC brushless motors, including inputs for Hall sensors and tachometers or other speed-related signals.
EMRG_TRP:	Emergency stop/trip function for motor control.
CAN1_RX/TX:	Logic level connection to CPU module’s second CAN module (where fitted).
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator
+12V:	Raw +12V from power input to baseboard
12VGND:	Ground connection to power supply.
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard

3V3 Vbatt:	Permanent +3V3 supply from Lithium cell on baseboard (where fitted)

1.3.3.2 EDPCON2 Signal Description

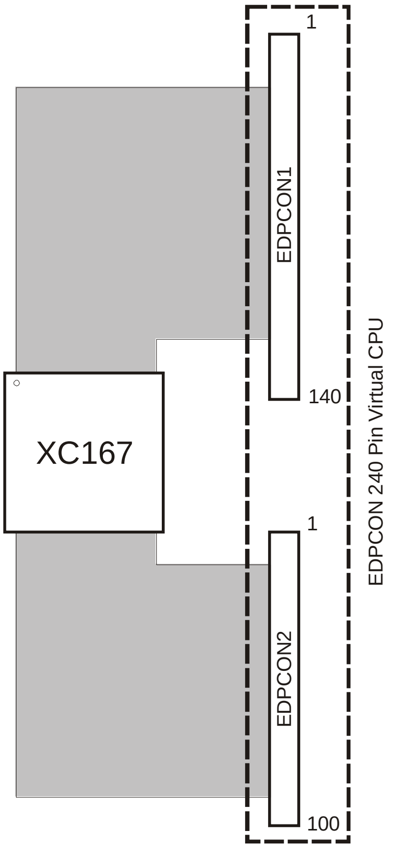
#RESIN:	Reset input to CPU module
#RESEOUT:	Reset out signal from CPU module (where available)
I2C_GEN0_SDA/SCL:	Secondary I^2C bus data and clock (where available)
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard
Axx_ADxx:	16-bit multiplexed address/data bus when enabled by jumpers on CPU module.
ALE:	CPU module’s address latch enable signal
#RD:	CPU module’s READ signal
#WR:	CPU module’s WRITE (or WRITELOW) signal
#WRH:	CPU module’s WRITE (or WRITEHIGH) signal
#PSEN_A16:	CPU module’s PSEN signal (8051) or A16, where available
#CS0:	CPU module’s first chip select signal
#CS1:	CPU module’s second chip select signal
#CS2:	CPU module’s third chip select signal
#CS3:	CPU module’s fourth chip select signal
CAN0_RX/TX:	Logic level connection to CPU module’s first CAN module (where fitted).
USB-DEBUG+/-	USB signals connected to FTDI USB-JTAG device on CPU module
CNTRL_SPI_XX:	Signals connected to CPU module’s first SPI peripheral
CNTRL_I2C_SDA/SCL:	Signals connected to CPU module’s first or primary I^2C channel. (This is the I^2C control backbone for the EDP baseboard).
CANH0/CANL0:	CPU module’s first CAN module via physical layer drivers.
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard

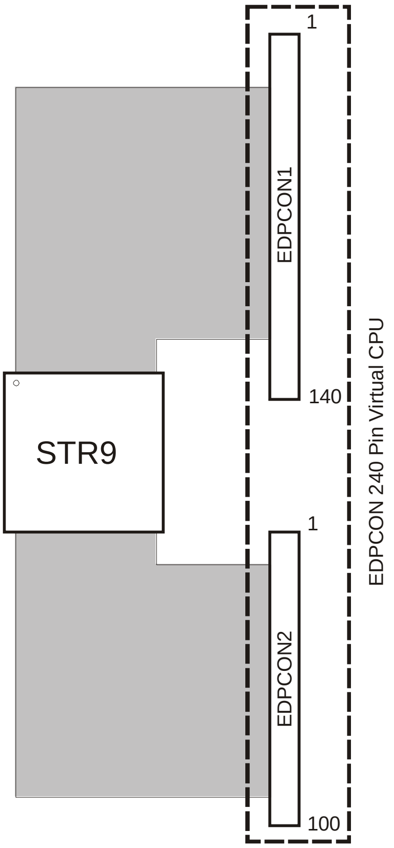
1.4 The EDP Virtual CPU Concept

A microcontroller that has its I/O pins mapped appropriately onto the EDPCON1 and EDPCON2 connectors appears to be a virtual CPU to other I/O devices fitted on the bus. Thus for example, a 14-bit ADC device on the EDPCON baseboard will see a CPU module also on the bus, as a virtual CPU whose pinout is defined by the EDP bus. Currently two popular microcontrollers (Infineon XC167 and ST STR9) have had their I/O pins mapped onto the EDPCON system. These two devices have some features in common -UARTs, capture and compare pins, ADC, CAN but the STR9 also has USB device. Thus the pin mapping to the EDPCON is not 100% in that on the XC167 version, the USB device pins are unused. Both devices have dedicated motor control peripherals which although they have different pin names, have virtually the same functionality.

Hence for example, a brushless DC motor control module with half-bridges can be designed to interface to the motor control region of the EDPCON bus without any regard for the CPU type to be ultimately used.
The net result is that subject some limitations, a range of modules bearing different CPUs can be freely connected to a range of I/O modules.

The EDPCON has been designed to accommodate all the common peripherals found on current microcontrollers, including advanced interfaces like SD/MMC and I^2S. Thus it is possible to map almost any microcontroller to this format.


1
EDPCON1
140
XC167
1
EDPCON2
100
EDPCON 240 Pin Virtual CPU

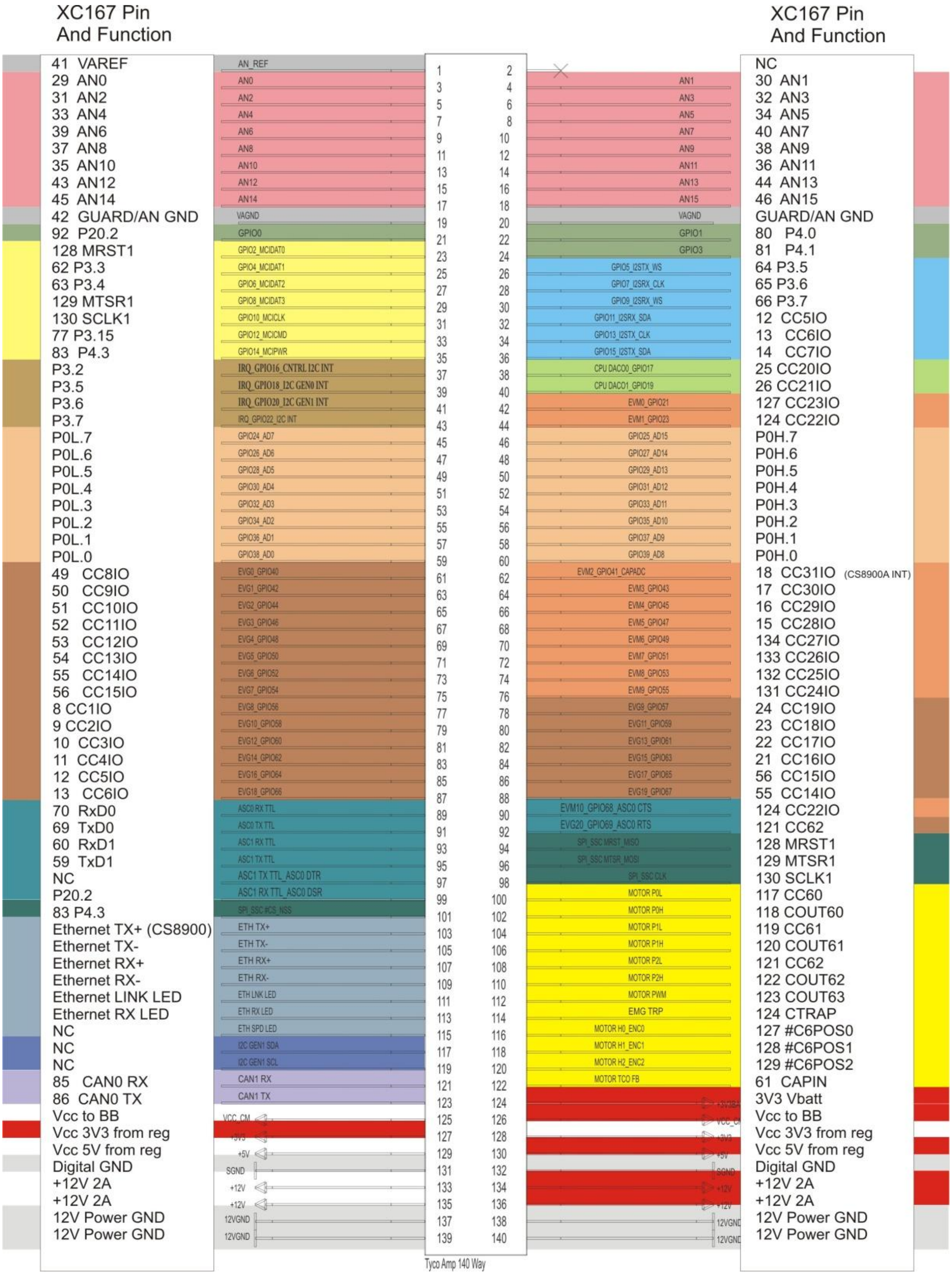

1
EDPCON1
140
STR9
1
EDPCON2
100
EDPCON 240 Pin Virtual CPU

1.4.1 Example of Real CPU to EDPCON Mapping

This is the mapping developed for the Infineon XC167 and used on the RS-EDP-CM-XC167 module.

1.4.1.1 Infineon XC167 – EDPCON1 Mapping

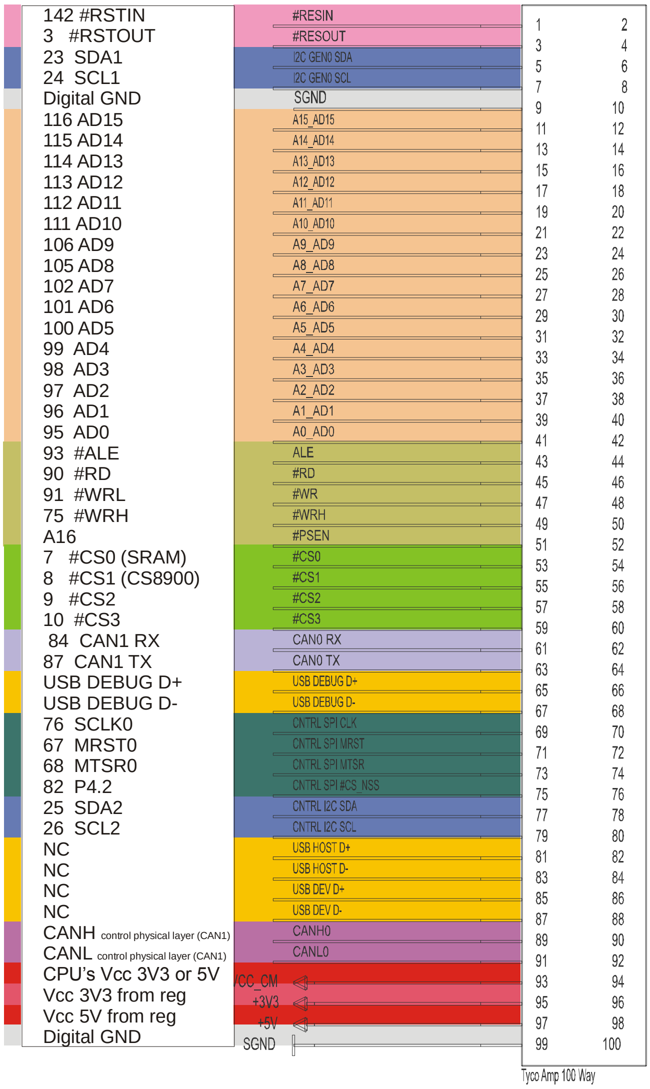
This mapping assigns the XC167 pins (and hence peripherals) into the appropriate regions on the EDPCON1 connector.



XC167 Pin And Function					XC167 Pin And Function
41 VAREF	AN_REF	1	2		NC
29 AN0	AN0	3	4	AN1	30 AN1
31 AN2	AN2	5	6	AN3	32 AN3
33 AN4	AN4	7	8	AN5	34 AN5
39 AN6	AN6	9	10	AN7	40 AN7
37 AN8	AN8	11	12	AN9	38 AN9
35 AN10	AN10	13	14	AN11	36 AN11
43 AN12	AN12	15	16	AN13	44 AN13
45 AN14	AN14	17	18	AN15	46 AN15
42 GUARD/AN GND	VAGND	19	20	VAGND	GUARD/AN GND
92 P20.2	GPIO0	21	22	GPIO1	80 P4.0
128 MRST1	GPIO2_MCIDAT0	23	24	GPIO3	81 P4.1
62 P3.3	GPIO4_MCIDAT1	25	26	GPIO5_I2STX_WS	64 P3.5
63 P3.4	GPIO6_MCIDAT2	27	28	GPIO7_I2SRX_CLK	65 P3.6
129 MTSR1	GPIO8_MCIDAT3	29	30	GPIO9_I2SRX_WS	66 P3.7
130 SCLK1	GPIO10_MCICLK	31	32	GPIO11_I2SRX_SDA	12 CC5IO
77 P3.15	GPIO12_MCICMD	33	34	GPIO13_I2STX_CLK	13 CC6IO
83 P4.3	GPIO14_MCIPWR	35	36	GPIO15_I2STX_SDA	14 CC7IO
P3.2	IRQ_GPIO16_CNTRL I2C INT	37	38	CPU DAC0_GPIO17	25 CC20IO
P3.5	IRQ_GPIO18_I2C GEN0 INT	39	40	CPU DAC1_GPIO19	26 CC21IO
P3.6	IRQ_GPIO20_I2C GEN1 INT	41	42	EVM0_GPIO21	127 CC23IO
P3.7	IRQ_GPIO22_I2C INT	43	44	EVM1_GPIO23	124 CC22IO
P0L.7	GPIO24_AD7	45	46	GPIO25_AD15	P0H.7
P0L.6	GPIO26_AD6	47	48	GPIO27_AD14	P0H.6
P0L.5	GPIO28_AD5	49	50	GPIO29_AD13	P0H.5
P0L.4	GPIO30_AD4	51	52	GPIO31_AD12	P0H.4
P0L.3	GPIO32_AD3	53	54	GPIO33_AD11	P0H.3
P0L.2	GPIO34_AD2	55	56	GPIO35_AD10	P0H.2
P0L.1	GPIO36_AD1	57	58	GPIO37_AD9	P0H.1
P0L.0	GPIO38_AD0	59	60	GPIO39_AD8	P0H.0
49 CC8IO	EVG0_GPIO40	61	62	EVM2_GPIO41_CAPADC	18 CC31IO (CS8900A INT)
50 CC9IO	EVG1_GPIO42	63	64	EVM3_GPIO43	17 CC30IO
51 CC10IO	EVG2_GPIO44	65	66	EVM4_GPIO45	16 CC29IO
52 CC11IO	EVG3_GPIO46	67	68	EVM5_GPIO47	15 CC28IO
53 CC12IO	EVG4_GPIO48	69	70	EVM6_GPIO49	134 CC27IO
54 CC13IO	EVG5_GPIO50	71	72	EVM7_GPIO51	133 CC26IO
55 CC14IO	EVG6_GPIO52	73	74	EVM8_GPIO53	132 CC25IO
56 CC15IO	EVG7_GPIO54	75	76	EVM9_GPIO55	131 CC24IO
8 CC1IO	EVG8_GPIO56	77	78	EVG9_GPIO57	24 CC19IO
9 CC2IO	EVG10_GPIO58	79	80	EVG11_GPIO59	23 CC18IO
10 CC3IO	EVG12_GPIO60	81	82	EVG13_GPIO61	22 CC17IO
11 CC4IO	EVG14_GPIO62	83	84	EVG15_GPIO63	21 CC16IO
12 CC5IO	EVG16_GPIO64	85	86	EVG17_GPIO65	56 CC15IO
13 CC6IO	EVG18_GPIO66	87	88	EVG19_GPIO67	55 CC14IO
70 RxD0	ASC0 RX TTL	89	90	EVM10_GPIO68_ASC0 CTS	124 CC22IO
69 TxD0	ASC0 TX TTL	91	92	EVG20_GPIO69_ASC0 RTS	121 CC62
60 RxD1	ASC1 RX TTL	93	94	SPI_SSC MRST_MISO	128 MRST1
59 TxD1	ASC1 TX TTL	95	96	SPI_SSC MTSR_MOSI	129 MTSR1
NC	ASC1 TX TTL_ASC0 DTR	97	98	SPI_SSC CLK	130 SCLK1
P20.2	ASC1 RX TTL_ASC0 DSR	99	100	MOTOR P0L	117 CC60
83 P4.3	SPI_SSC #CS_NSS	101	102	MOTOR P0H	118 COUT60
Ethernet TX+ (CS8900)	ETH TX+	103	104	MOTOR P1L	119 CC61
Ethernet TX-	ETH TX-	105	106	MOTOR P1H	120 COUT61
Ethernet RX+	ETH RX+	107	108	MOTOR P2L	121 CC62
Ethernet RX-	ETH RX-	109	110	MOTOR P2H	122 COUT62
Ethernet LINK LED	ETH LNK LED	111	112	MOTOR PWM	123 COUT63
Ethernet RX LED	ETH RX LED	113	114	EMG TRP	124 CTRAP
NC	ETH SPD LED	115	116	MOTOR H0_ENC0	127 #C6POS0
NC	I2C GEN1 SDA	117	118	MOTOR H1_ENC1	128 #C6POS1
NC	I2C GEN1 SCL	119	120	MOTOR H2_ENC2	129 #C6POS2
85 CAN0 RX	CAN1 RX	121	122	MOTOR TCO FB	61 CAPIN
86 CAN0 TX	CAN1 TX	123	124	+3V3BA	3V3 Vbatt
Vcc to BB	VCC_CM	125	126	VCC_C	Vcc to BB
Vcc 3V3 from reg	+3V3	127	128	+3V3	Vcc 3V3 from reg
Vcc 5V from reg	+5V	129	130	+5V	Vcc 5V from reg
Digital GND	SGND	131	132	SGND	Digital GND
+12V 2A	+12V	133	134	+12V	+12V 2A
+12V 2A	+12V	135	136	+12V	+12V 2A
12V Power GND	12VGND	137	138	12VGND	12V Power GND
12V Power GND	12VGND	139	140	12VGND	12V Power GND

Tyco Amp 140 Way

1.4.1.2 Infineon XC167 – EDPCON2 Mapping



142 #RSTIN	#RESIN	1	2
3 #RSTOUT	#RESOUT	3	4
23 SDA1	I2C GEN0 SDA	5	6
24 SCL1	I2C GEN0 SCL	7	8
Digital GND	SGND	9	10
116 AD15	A15_AD15	11	12
115 AD14	A14_AD14	13	14
114 AD13	A13_AD13	15	16
113 AD12	A12_AD12	17	18
112 AD11	A11_AD11	19	20
111 AD10	A10_AD10	21	22
106 AD9	A9_AD9	23	24
105 AD8	A8_AD8	25	26
102 AD7	A7_AD7	27	28
101 AD6	A6_AD6	29	30
100 AD5	A5_AD5	31	32
99 AD4	A4_AD4	33	34
98 AD3	A3_AD3	35	36
97 AD2	A2_AD2	37	38
96 AD1	A1_AD1	39	40
95 AD0	A0_AD0	41	42
93 #ALE	ALE	43	44
90 #RD	#RD	45	46
91 #WRL	#WR	47	48
75 #WRH	#WRH	49	50
A16	#PSEN	51	52
7 #CS0 (SRAM)	#CS0	53	54
8 #CS1 (CS8900)	#CS1	55	56
9 #CS2	#CS2	57	58
10 #CS3	#CS3	59	60
84 CAN1 RX	CAN0 RX	61	62
87 CAN1 TX	CAN0 TX	63	64
USB DEBUG D+	USB DEBUG D+	65	66
USB DEBUG D-	USB DEBUG D-	67	68
76 SCLK0	CNTRL SPI CLK	69	70
67 MRST0	CNTRL SPI MRST	71	72
68 MTSR0	CNTRL SPI MTSR	73	74
82 P4.2	CNTRL SPI #CS_NSS	75	76
25 SDA2	CNTRL I2C SDA	77	78
26 SCL2	CNTRL I2C SCL	79	80
NC	USB HOST D+	81	82
NC	USB HOST D-	83	84
NC	USB DEV D+	85	86
NC	USB DEV D-	87	88
CANH control physical layer (CAN1)	CANH0	89	90
CANL control physical layer (CAN1)	CANL0	91	92
CPU's Vcc 3V3 or 5V	VCC_CM	93	94
Vcc 3V3 from reg	+3V3	95	96
Vcc 5V from reg	+5V	97	98
Digital GND	SGND	99	100

Tyco Amp 100 Way

1.5 Inter-Module Communication

With up to four modules on the EDPCON bus, some form of inter-module communication is required. With a limited number of CPU pins available, it is necessary to use a serial communications protocol to, for example, take readings from a high-precision ADC at the same time as read a serial EEPROM on a further module. The I^{2}C protocol is used as the main communication channel for such actions, although provision is made for SPI or even a CAN physical layer.

Module	**I^{2}C Device**	**Possible Range**	**Actual 7-bit Address**	**I^{2}C channel**	**Actual 7-bit Address**	**I^{2}C channel**	**Comment**
			Module 1		**Module 2**		
Baseboard	PCF8575TS	0x20 - 0x27	0x20	CNTRL	XXXX	XXXX	DIP configuration switches
	24C32 (Rev B)	0x50 - 0x57	0x51	CNTRL	0x52	CNTRL	4 kbyte EEPROM
Analogue AM	MAX1138EEE	0x35	0x35	CNTRL	0x35	Gen0	12-channel 10-bit ADC
	AD5263BRU50	0x2C - 0x2F	0x2C	CNTRL	0x2C	Gen0	Digital Potentiometer
Comms AM	PCF8583	0x50 - 0x51	0x50	CNTRL	XXXX	XXXX	Real-Time Clock and RAM
Digital AM	PCF8575TS	0x20 - 0x27	0x22	CNTRL	0x24	CNTRL	16-channel digital input
	PCF8575TS	0x20 - 0x27	0x23	CNTRL	0x25	CNTRL	16-channel digital output

There are three possible I^{2}C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I^{2}C device do, where possible, allow the user to configure the I^{2}C addresses. This allows for example, up to three digital I/O modules to be fitted, with the GPIO devices on each module given an unique address. Where the address space of a particular I^{2}C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.

1.6 Inter-EDP System Communications

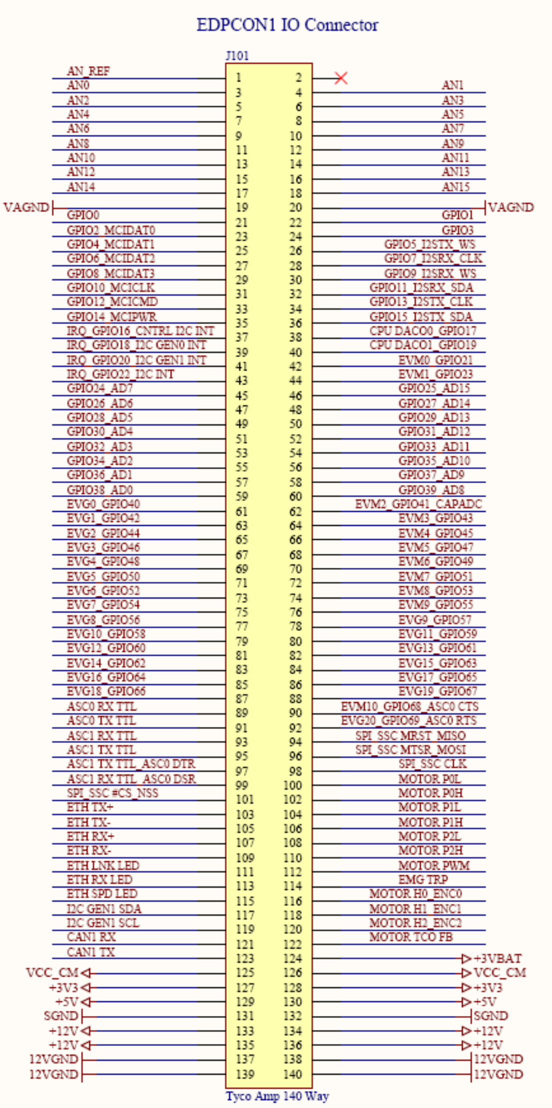
In a situation where there are multiple EDP baseboards, each with their own CPU modules in a complete system, an I^{2}C bus can still be used to allow the CPUs to communicate, but the use of a CAN bus is strongly recommended. EDP I/O signals that are intended to be taken off-board are brought out on a standard DIN41612 64-way connector.

2. Using the EDP Baseboard

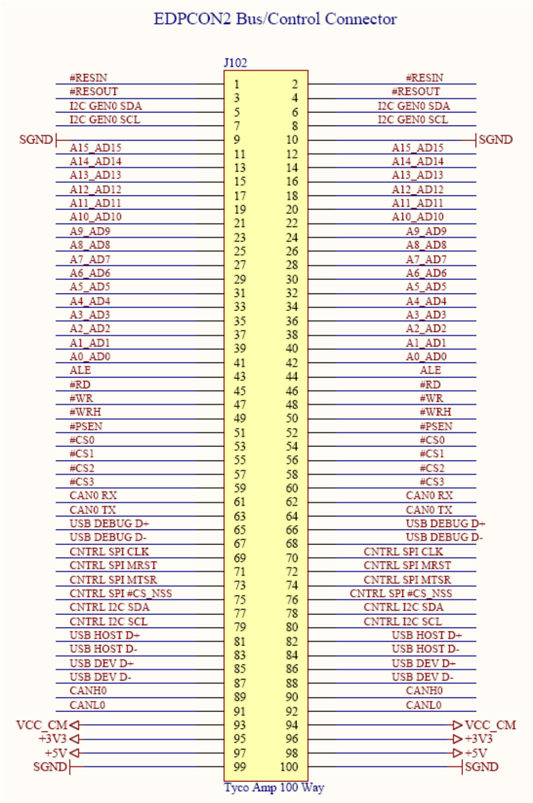
This section gives information on the features of the EDP baseboard, its connectors and the overall structure of the EDP system.

2.1 EDP Connectors

The EDP bus contained in the EDP baseboard is accessed through two Tyco-AMP 0.8mm pitch connectors. The signal names are intended to convey something of the capabilities of that signal. For example signal EVG0_GPIO40 is a pin that can generate timed events (i.e. pulses and pulse trains) as well as performing simple on/off pin control.



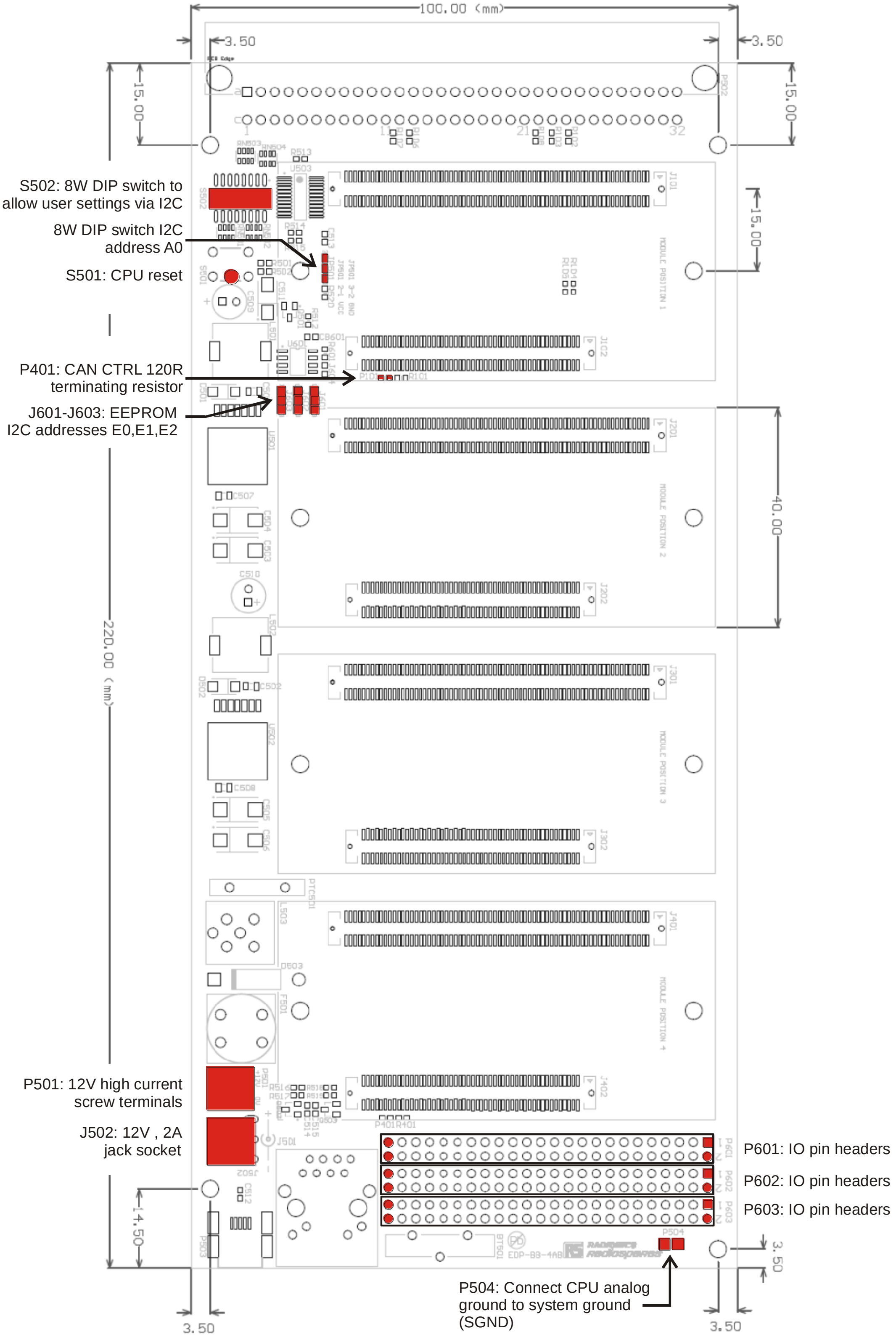
EDPCON1 Connector



EDPCON2 Connector

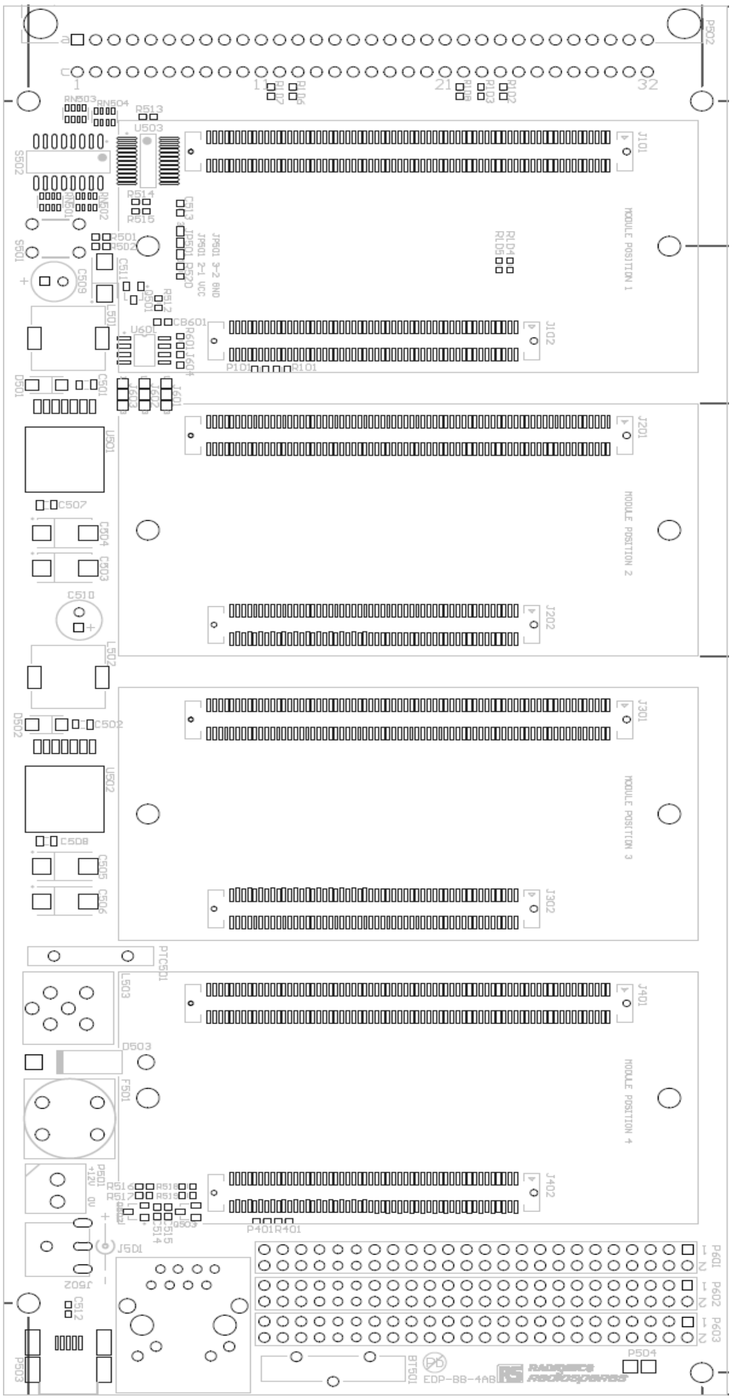
2.2 EDP Baseboard User Options Placement

There are a number of user-selectable functions on the baseboard, as shown below:



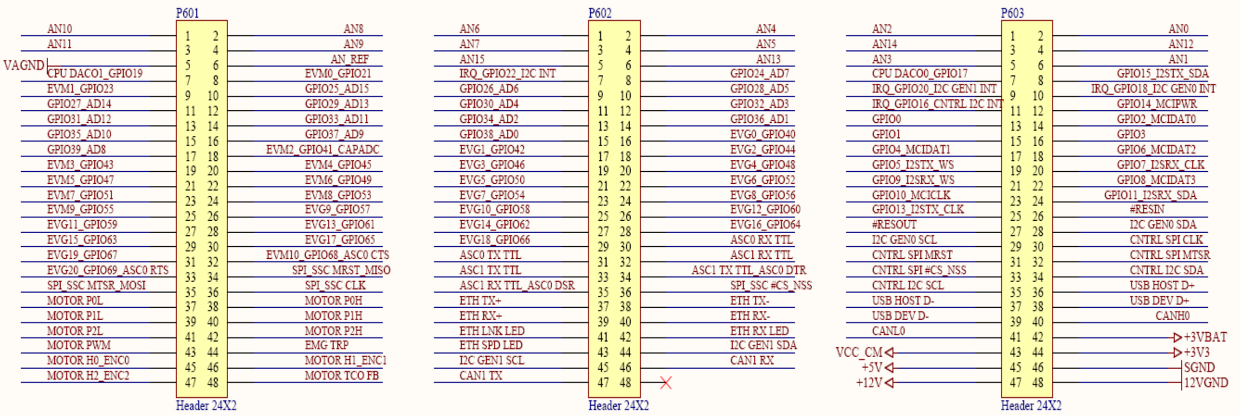
2.3 EDP Baseboard Component Placement

The location of the major items on the EDP baseboard is shown below.



2.4 EDP I/O Pin Headers

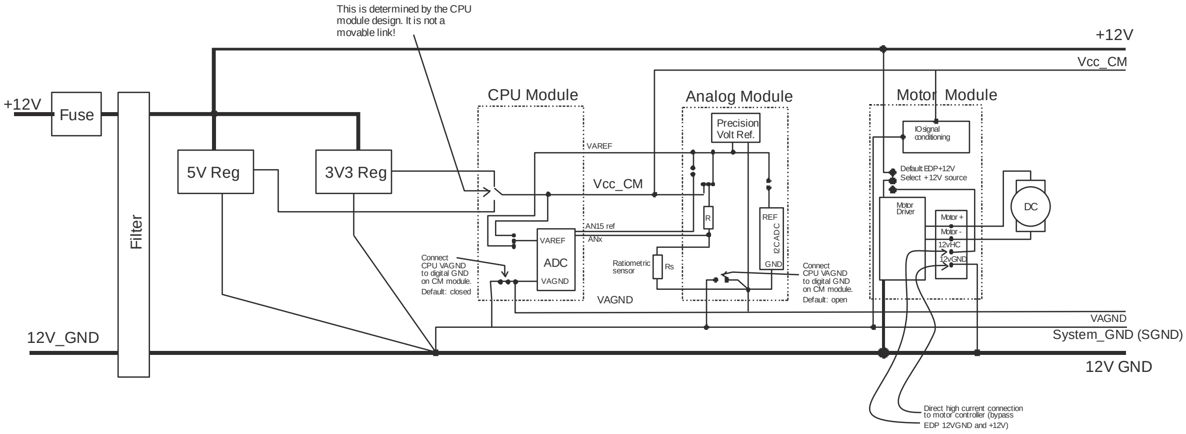
All the signals in the EDP backplane are available here on 0.1” pin headers for connection to test equipment, etc.



2.5 Grounding Arrangements

The system ground (SGND) and 12V ground (12V_GND) are connected together at a star point on the baseboard. The 12V GND is used for high current devices like the motor controller and the Darlington output drivers on the digital I/O module. System ground is used for all returns on logic devices on all modules. It can be used for analogue returns but there is a risk of noise (ground bounce).

Analogue ground (VAGnd) by default is an offshoot of the system ground which occurs only on the CM. It is routed to the VAGnd pins of the CPU and also acts as a return for filter circuits used for analogue inputs. It is optionally possible to connect the SGND to the Analogue ground on the analogue module, although this should not be necessary unless there are a large number of resistive sensors being used. In this case, the link connecting VAGnd and SGND on the CM must be opened to avoid ground loops.



2.6 Positive Supplies

The +12V line comes via the screw terminals on the baseboard or the mini-jack. It is fused and filtered before entering the EDP backplane. The +3V3 and +5V voltage regulators are driven from the +12V.

2.6.1 Logic Supplies

Both +3V3 and +5V are available on the EDPCON to support both +5V and +3V3 processors and devices. To allow the interfacing of I/O devices at the required voltage, the positive supply to the CPU I/O domain is routed into the EDPCON through Vcc_CM. It is intended to be used for pull-ups on I/O pins and powering small active components that connect directly to the CPU such as discrete logic, op-amps etc. Vcc_CM is limited to 500mA total current draw from other modules and the baseboard.

Vcc_CM is connected inside the CM to the voltage used by the CPU's I/O domain.

2.6.2 Analogue Supply

The Analogue supply to the CPU ADC may be derived from the local Vcc or from a precision reference located on the Analogue AM. Ideally the Analogue AM and CM should be in adjacent positions on the baseboard to keep the signal length to a minimum if the latter is chosen.
The I^2C ADC on the analogue module can use the Vcc_CM or the local precision voltage references, either +3V3 or +5V. The 5V reference is driven from the 12V to guarantee no drop-out problems.

As the anti-aliasing filters are run at +5V, the local ADC is not tied to the same voltage range as the CPU's ADC. It is the user's responsibility to make sure that the input does not exceed the permissible input voltage range of the CPU ADC. Protection resistors are provided to prevent damage.

2.7 Limits and Restrictions

Vcc CM max current	500mA
3V3 max current	2000mA
5V max current	2000mA
3V3 current + 5V current + Vcc_CM	2000mA
SGND max current	2000mA
12VGND max current	2000mA

Warning: Only attempt to fit two CPU modules to the baseboard at the same time when you are really certain you know what you're doing! If they have different peripheral supply voltages then damage is likely to occur.

2.8 EDP Control Busses

2.8.1 I^{2}C Busses

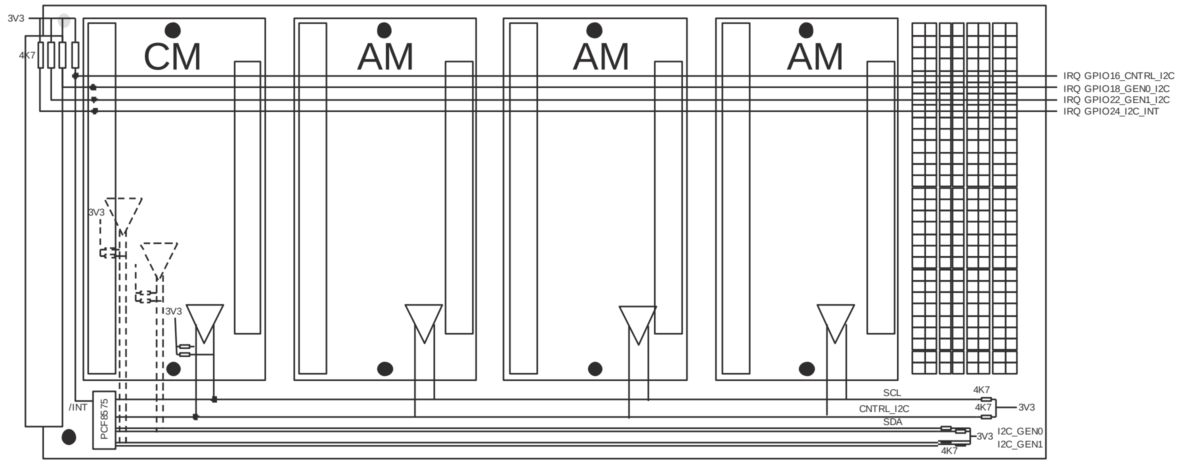
The EDP uses I^{2}C as the data and control backbone. Depending on the capabilities of the CM fitted, up to three independent I^{2}C busses are available. I^{2}C channel "CNTRL_I2C" is the primary I^{2}C device bus and is used by default to communicate with I^{2}C devices on the baseboard and application modules.

The I^{2}C address space is based on the 7-bit addressing scheme. I^{2}C devices that are able to generate an interrupt request by default use the IRQ_GPIO16_CNTRL_I2C_INT line, with the option of using up to another three interrupt-capable lines. A pull-up resistor is provided on IRQ_GPIO16_CNTRL_I2C_INT so that the open collector /INT outputs on I^{2}C devices can signal an interrupt by pulling this line down.

The I^{2}C bus runs at +3V3 so any +5V devices must be connected via a level shifting mechanism.

The I^{2}C bus devices require pull-up resistors on the SDA and SCL lines and these are incorporated on the baseboard.

There are three possible I^{2}C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I^{2}C device do, where possible, allow the user to configure the I^{2}C addresses. This allows for example, up to three digital I/O modules to be fitted, with the GPIO devices on each module given a unique address. Where the address space of a particular I^{2}C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.



Only CMs can optionally
have pull-ups to 3V3

2.8.1.1 Available I^{2}C Interrupt Request Lines

Each of the three potential I^{2}C channels has a dedicated interrupt request line into the CM. A spare interrupt line is provided that can be allocated to any channel, as defined by the user. However it is up to the user to make sure that the software is able to recognise the I^{2}C device that requested the interrupt.

I2C_CTRL	IRQ GPIO16_CNTRL_I2C	(integral pull-ups)
I2C_GEN0	IRQ GPIO18_GEN0_I2C	(integral pull-ups)
I2C_GEN1	IRQ GPIO22_GEN1_I2C	(integral pull-ups)
Uncommitted	IRQ GPIO24_I2C_INT	(integral pull-ups)

2.9 CAN Network

The on-board CAN network “CAN CNTRL” is intended to allow the interconnection of modules and other EDP systems via CAN. The first CAN module on any CPU is by default allocated to the CANH0 and CANL0 bus. This is the CAN physical layer (i.e. after the CAN transceivers) and can run at up 1MB/s. The 120R termination resistors at the ends of the network are located on the CM and at the end of the baseboard that carries the Ethernet and USB connectors. If the CAN CNTRL bus is taken off-board via the DIN41612 expansion connector then the 120R resistor on the baseboard must be disconnected by removing the P201 link.

The CAN CNTRL bus is available through a 9-way D-connector on the optional EDP-AM-CO1-A communications module.