



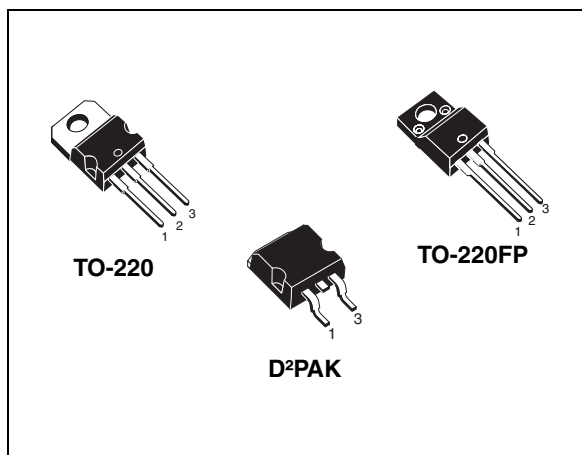
STB9NK60ZD STF9NK60ZD - STP9NK60ZD

N-channel 600 V - 0.85 Ω - 7 A - D²PAK, TO-220FP, TO-220
SuperFREDMesh™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _w
STB9NK60ZD	600 V	< 0.95 Ω	7 A	125 W
STF9NK60ZD	600 V	< 0.95 Ω	7 A	30 W
STP9NK60ZD	600 V	< 0.95 Ω	7 A	125 W

- Very high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Low intrinsic capacitances
- Fast internal recovery diode



Application

- Switching applications

Description

The SuperFREDMesh™ series associates all advantages of reduced on-resistance, zener gate protection and very high dv/dt capability with a Fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

Figure 1. Internal schematic diagram

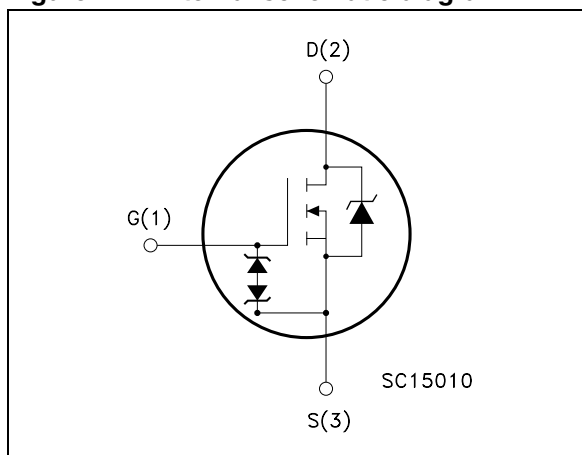


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB9NK60ZD	B9NK60ZD	D ² PAK	Tape and reel
STF9NK60ZD	F9NK60ZD	TO-220FP	Tube
STP9NK60ZD	P9NK60ZD	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK/TO-220	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	7	7 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	4.3	4.3 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	28	28 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	125	30	W
	Derating factor	1	0.24	W/ $^{\circ}\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 k Ω)	4000		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^{\circ}\text{C}$)	--	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		$^{\circ}\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 500\text{ A}/\mu\text{s}$, $V_{DD} = 80\%V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK/TO-220	TO-220FP	
$R_{thj-pcb}$	Thermal resistance junction-pcb Max (when mounted on minimum footprint)	30	--	$^{\circ}\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case Max	1	4.16	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5		$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	235	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125 \text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$, $I_D = 3.5 \text{ A}$		0.85	0.95	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 3.5 \text{ A}$		5.3		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		1110 135 30		pF pF pF
$C_{OSS \text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0 \text{ to } 480 \text{ V}$		72		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}$, $I_D = 7 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 17)		41 8.7 21	53	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2. $C_{OSS \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		11.4		ns
t_r	Rise time			13.6		ns
$t_{d(off)}$	Turn-off-delay time			23.1		ns
t_f	Fall time			15		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		11		ns
t_f	Fall time			8		ns
t_c	Cross-over time			20		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ (see Figure 21)		130		ns
Q_{rr}	Reverse recovery charge			550		nC
I_{RRM}	Reverse recovery current			8.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 21)		176		ns
Q_{rr}	Reverse recovery charge			880		nC
I_{RRM}	Reverse recovery current			10		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / D²PAK

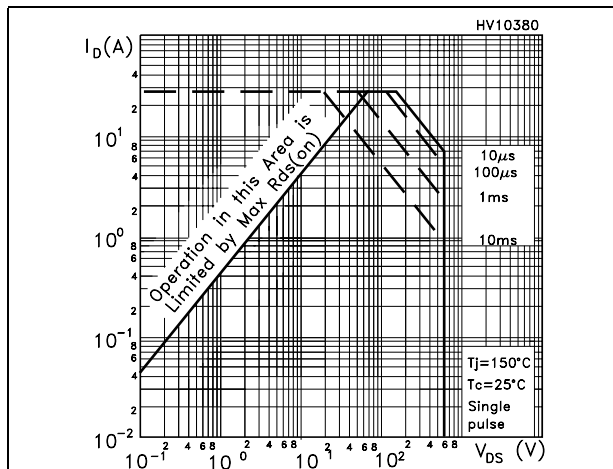


Figure 3. Thermal impedance for TO-220 / D²PAK

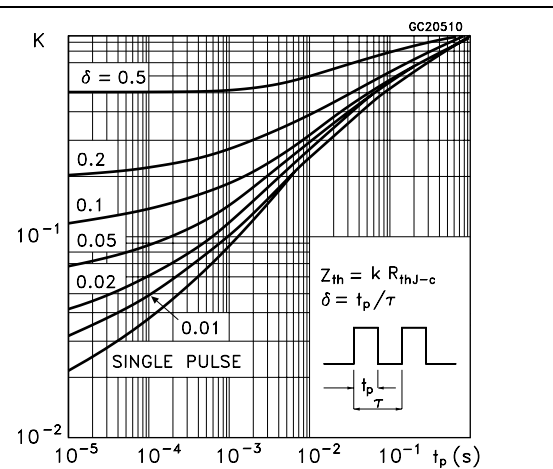


Figure 4. Safe operating area for TO-220FP

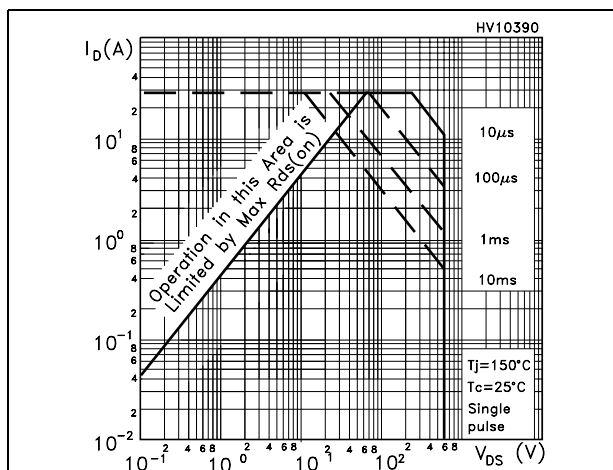


Figure 5. Thermal impedance for TO-220FP

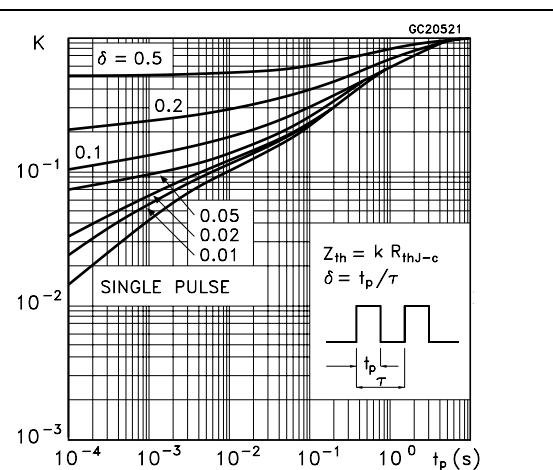


Figure 6. Output characteristics

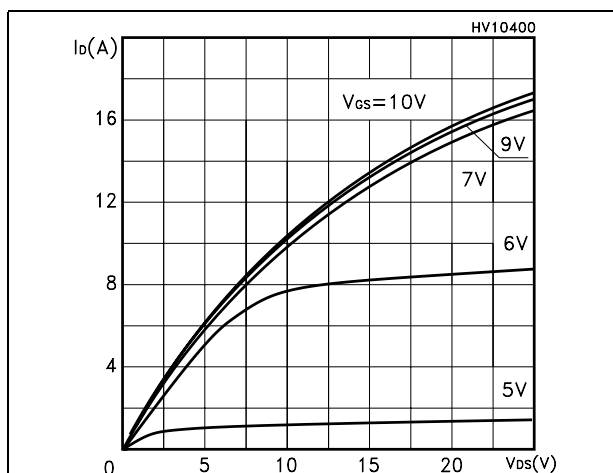


Figure 7. Transfer characteristics

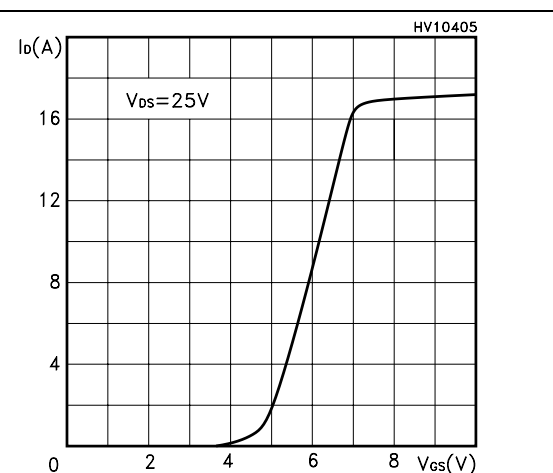


Figure 8. Normalized $B_{V_{DS}}$ vs temperature

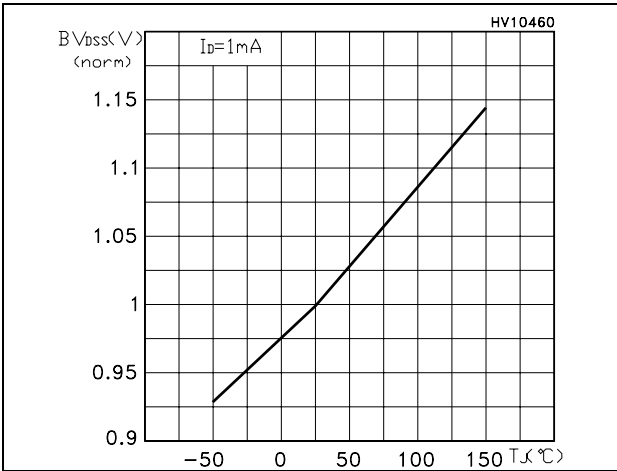


Figure 9. Static drain-source on resistance

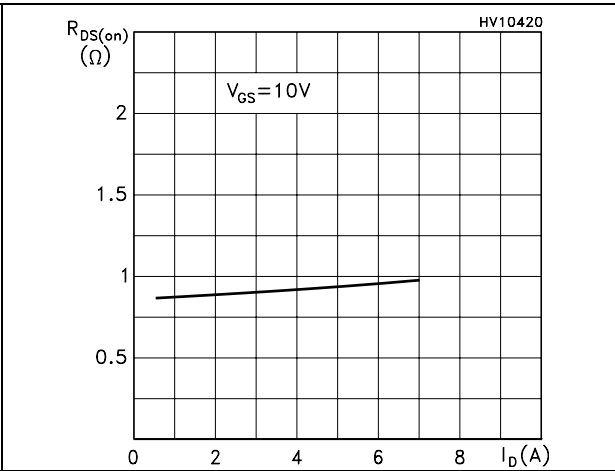


Figure 10. Gate charge vs gate-source voltage

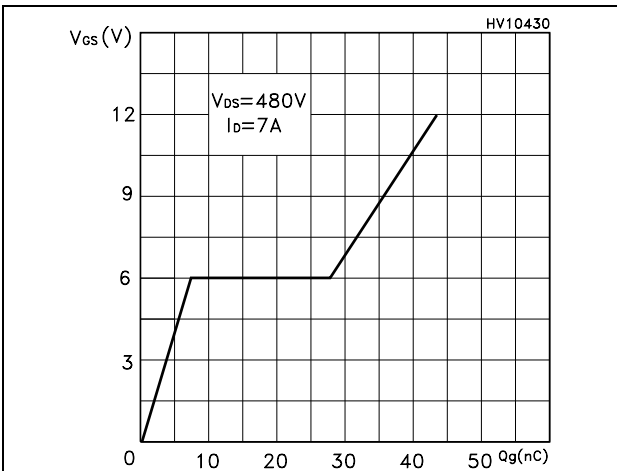


Figure 11. Capacitance variations

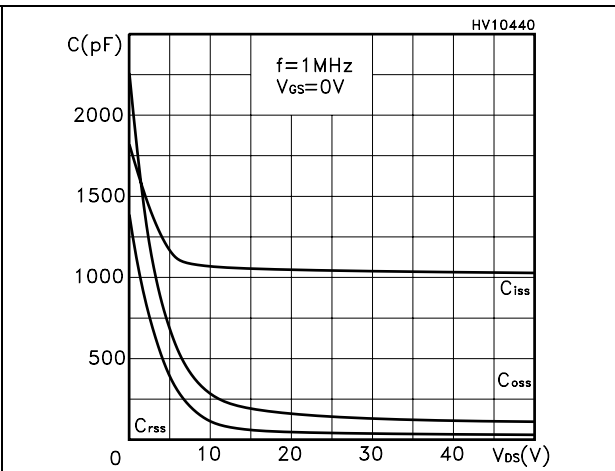


Figure 12. Normalized gate threshold voltage vs temperature

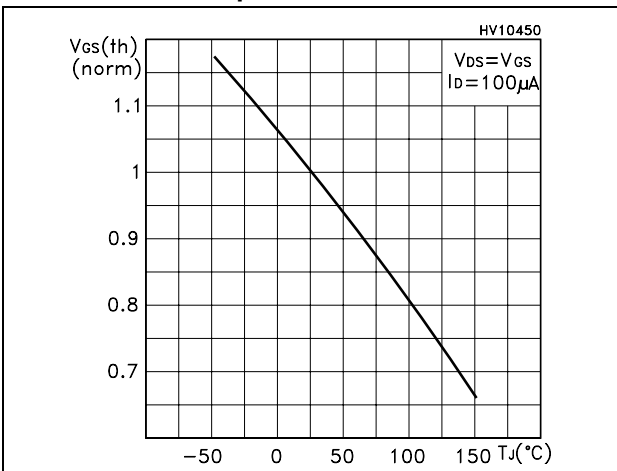


Figure 13. Normalized on resistance vs temperature

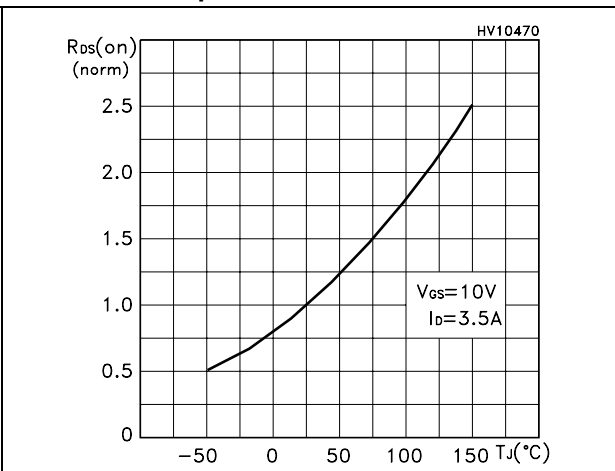


Figure 14. Source-drain diode forward characteristics

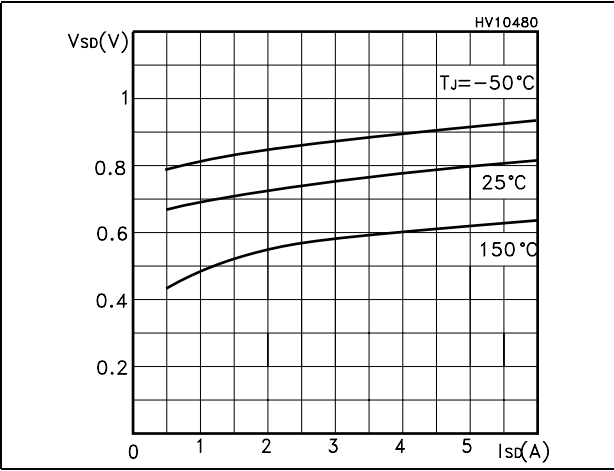
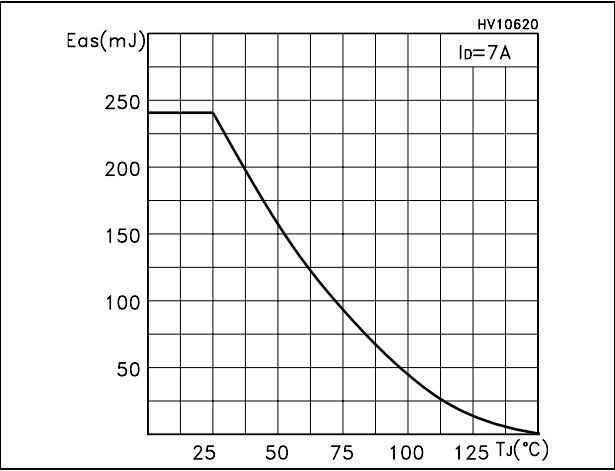


Figure 15. Maximum avalanche energy vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

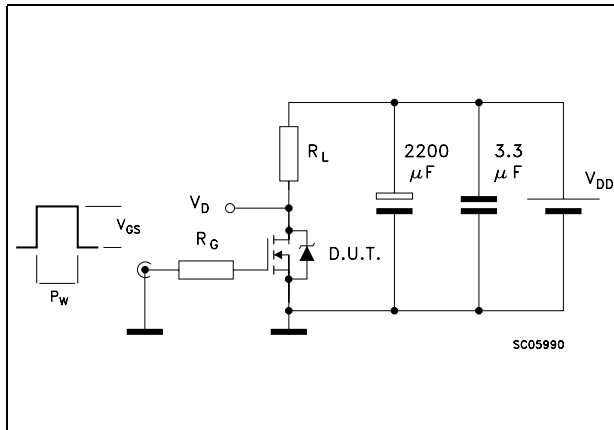


Figure 17. Gate charge test circuit

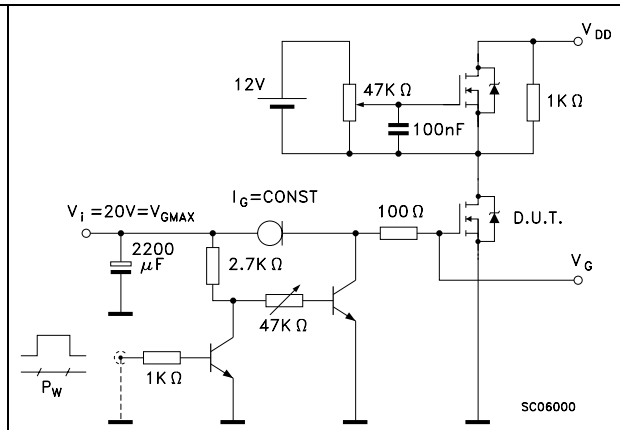


Figure 18. Test circuit for inductive load switching and diode recovery times

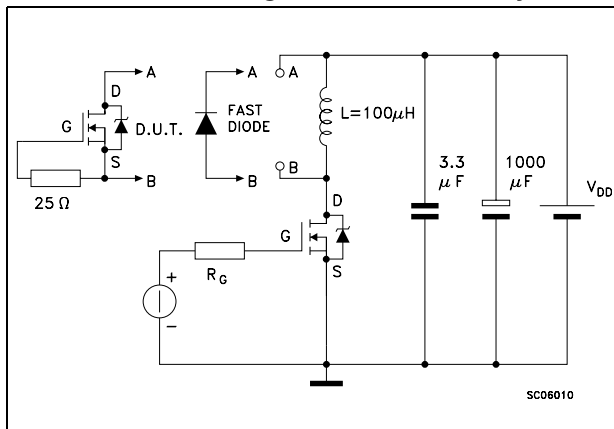


Figure 19. Unclamped inductive load test circuit

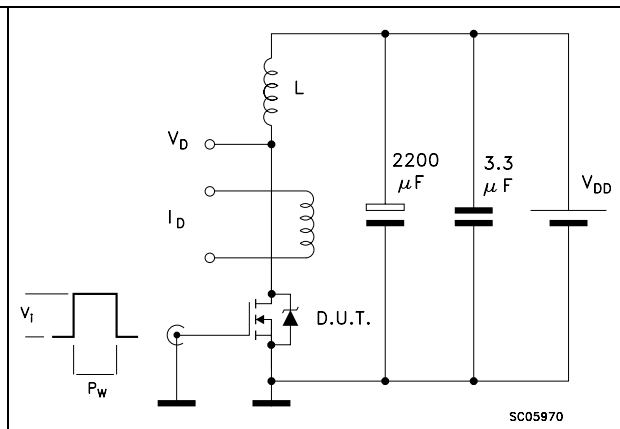


Figure 20. Unclamped inductive waveform

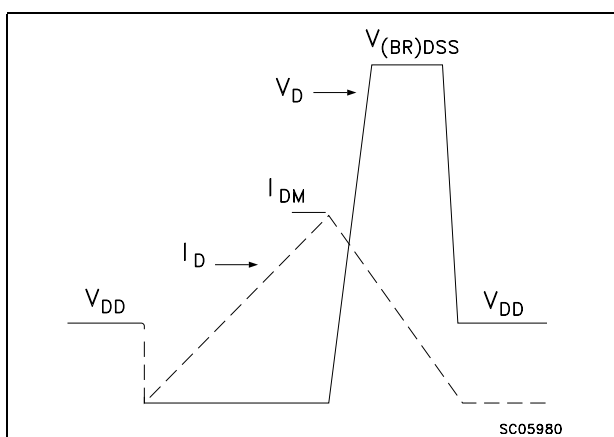
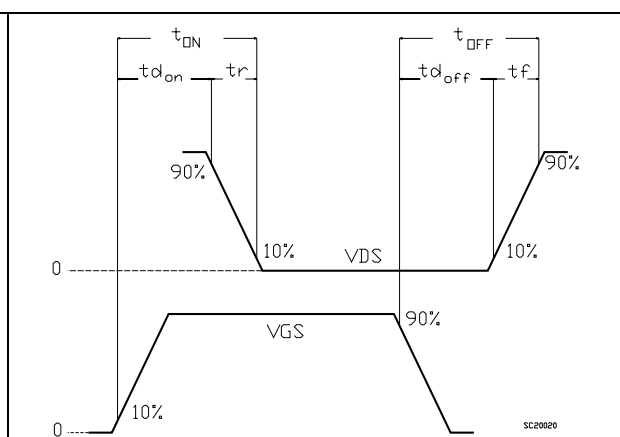


Figure 21. Switching time waveform

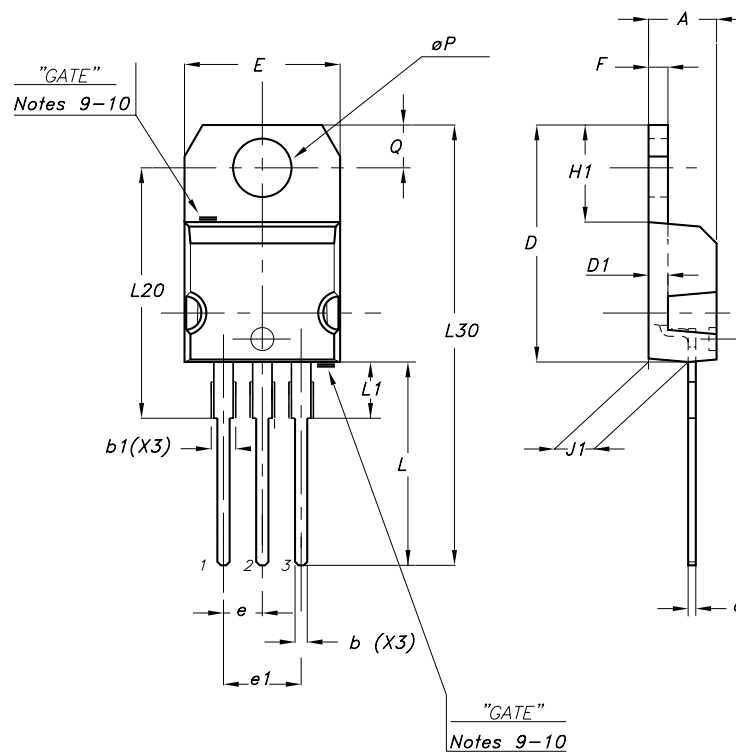


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 mechanical data

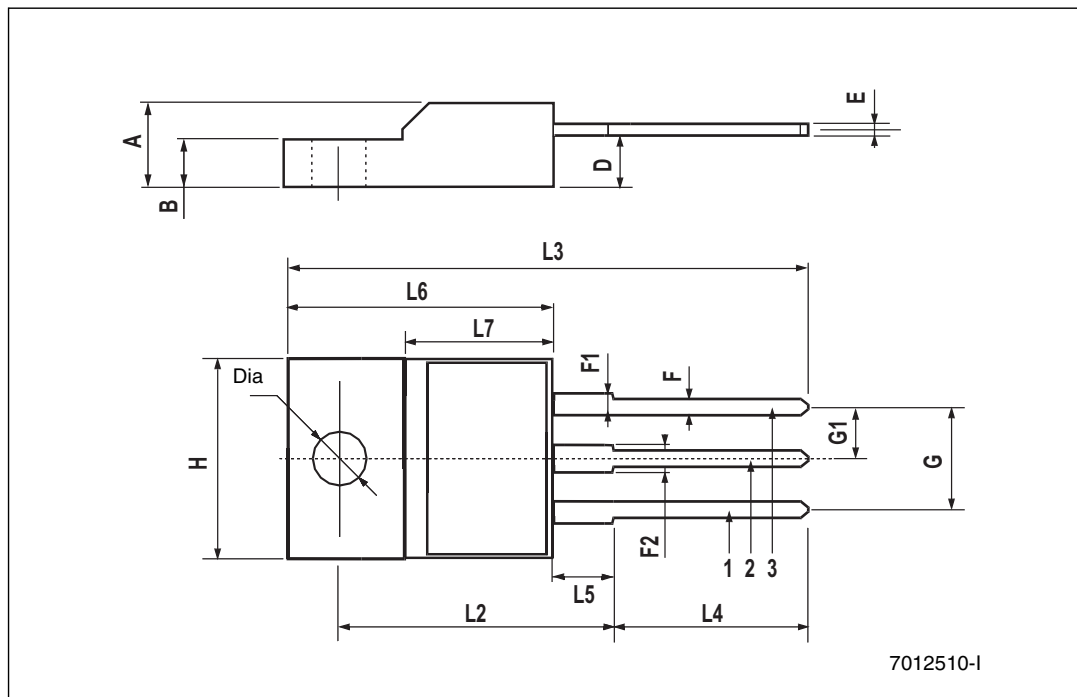
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



0015988_Rev_R

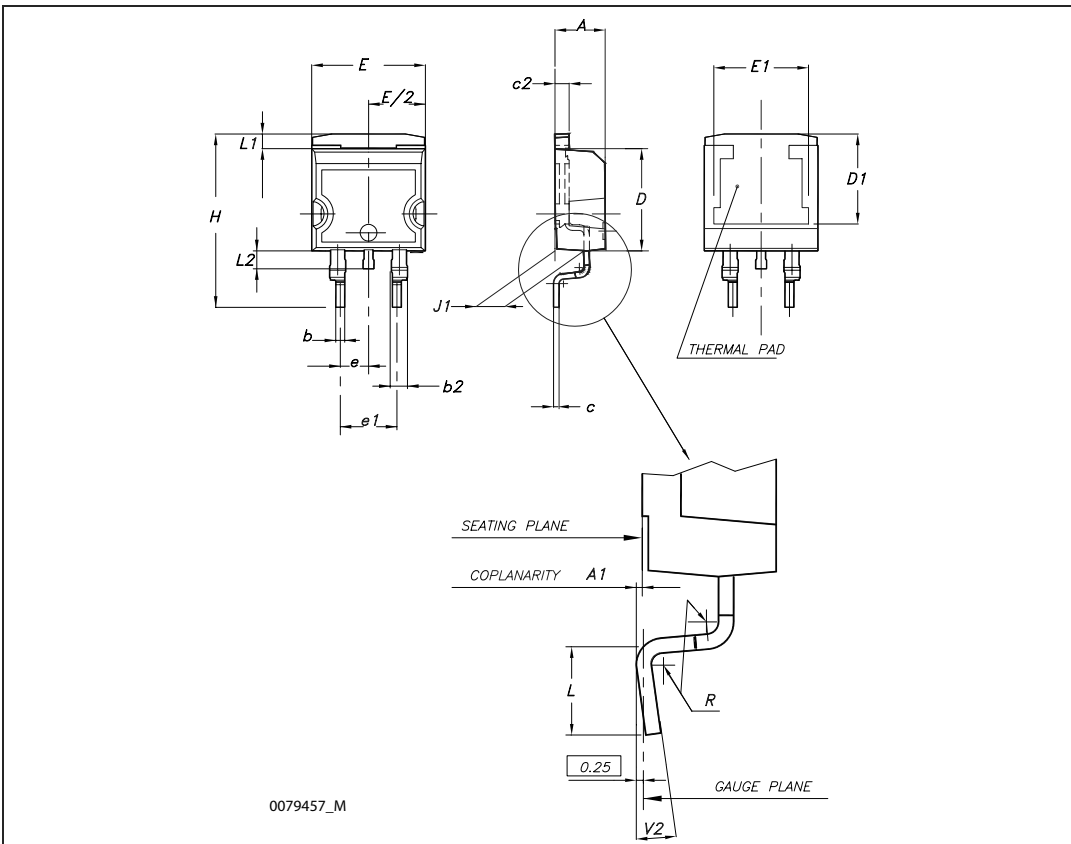
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

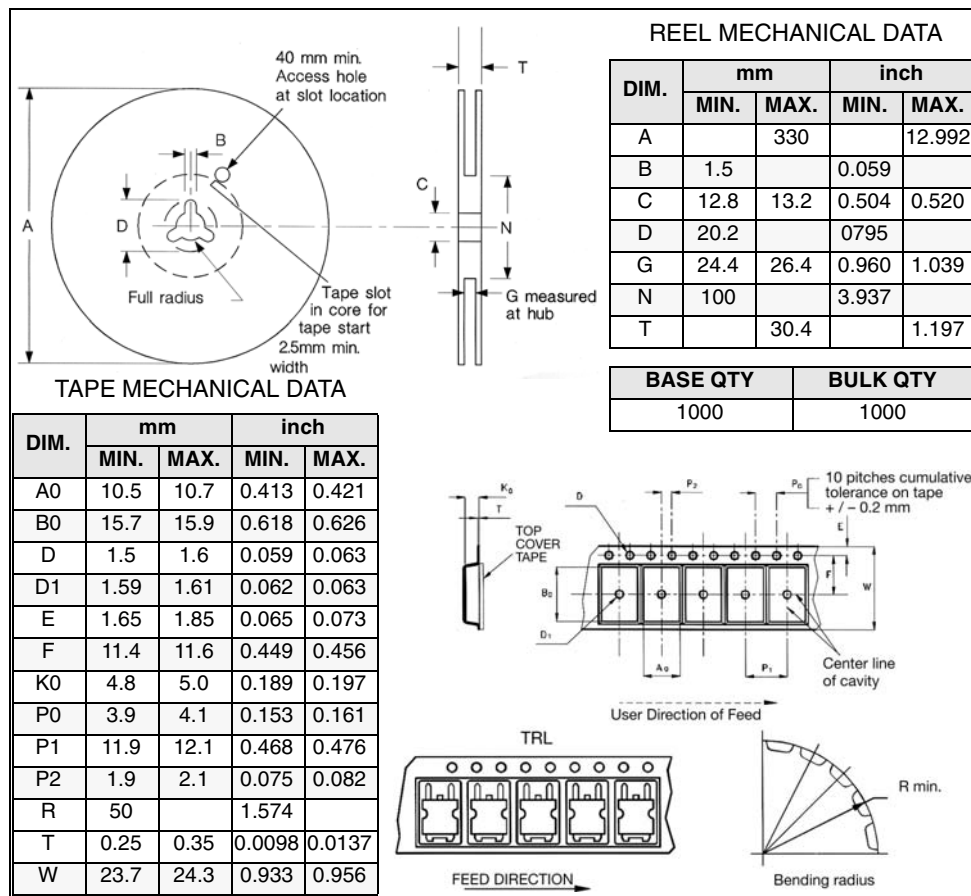


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Sep-2003	6	Data updated
13-Jun-2006	7	The document has been reformatted
14-Apr-2008	9	– Table 8 has been corrected – Package mechanical data updated.

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