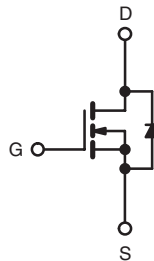
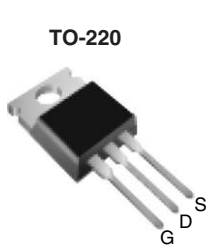


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.26
$Q_g$ (Max.) (nC)	120	
$Q_{gs}$ (nC)	34	
$Q_{gd}$ (nC)	54	
Configuration	Single	



N-Channel MOSFET

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low  $R_{DS(on)}$
- Lead (Pb)-free Available



**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB18N50KPbF
	SiHFB18N50K-E3
SnPb	IRFB18N50K
	SiHFB18N50K

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	500	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	17	A
		$T_C = 100$ °C	11	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	68		
Linear Derating Factor		1.8	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	370	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	17	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	22	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	220	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	7.8	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw	10		

#### Notes


- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting  $T_J = 25$  °C,  $L = 2.5$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 17$  A.
- $I_{SD} \leq 17$  A,  $dI/dt \leq 376$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	-	58	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain) <sup>a</sup>	$R_{thJC}$	-	0.56	

**Note**

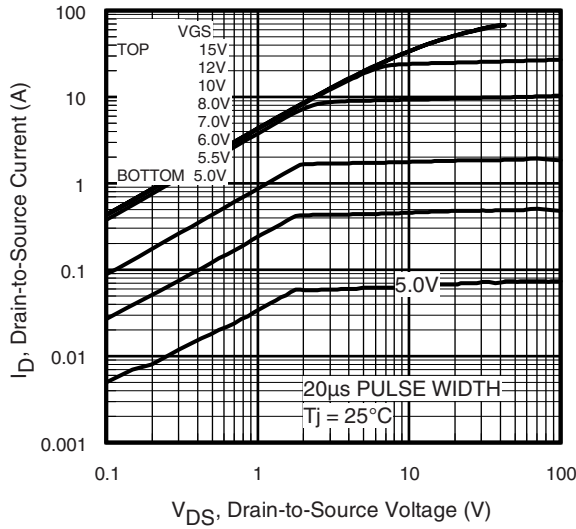
a.  $R_{th}$  is measured at  $T_J$  approximately 90 °C.

SPECIFICATIONS $T_J = 25\text{ °C}$ , unless otherwise noted									
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
<b>Static</b>									
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V		
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$		-	0.59	-	V/°C		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V		
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$		
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		-	-	250			
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}^b$	-	0.26	0.29	$\Omega$		
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 10\text{ A}$		6.4	-	-	S		
<b>Dynamic</b>									
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5		-	2830	-	pF		
Output Capacitance	$C_{oss}$			-	330	-			
Reverse Transfer Capacitance	$C_{rss}$			-	38	-			
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	3310	-	pF		
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	93	-			
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to }400\text{ V}^c$		-	155	-			
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$		$I_D = 17\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 <sup>b</sup>		-	120	nC	
Gate-Source Charge	$Q_{gs}$					-	-		34
Gate-Drain Charge	$Q_{gd}$					-	-		54
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}$		$V_{DD} = 250\text{ V}, I_D = 17\text{ A},$ $R_G = 7.5\text{ }\Omega,$ see fig. 10 <sup>b</sup>		-	22	ns	
Rise Time	$t_r$					-	60		-
Turn-Off Delay Time	$t_{d(off)}$					-	45		-
Fall Time	$t_f$					-	30		-
<b>Drain-Source Body Diode Characteristics</b>									
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	17	A		
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	68			
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V		
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 17\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	520	780	ns		
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	5.3	8.0	$\mu\text{C}$		
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )							

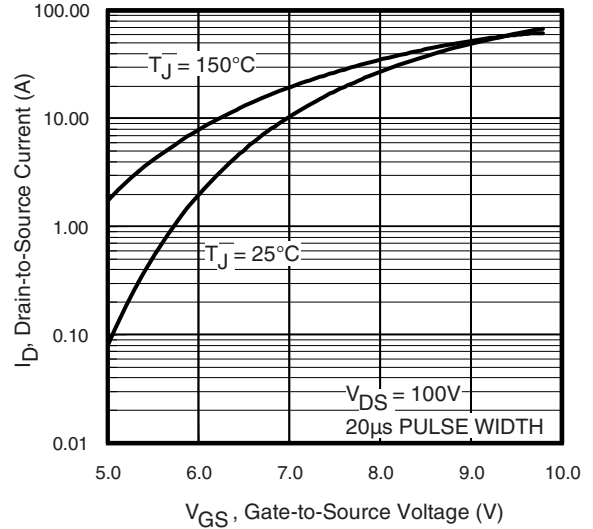
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

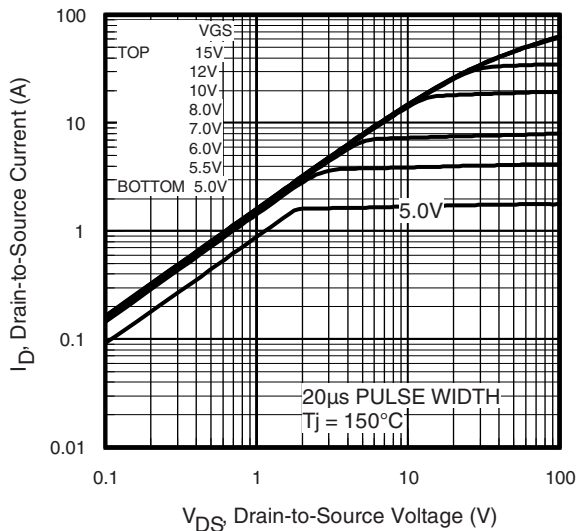
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



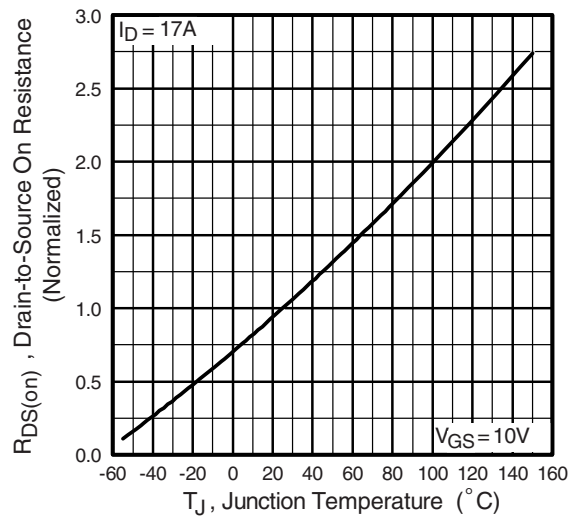
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

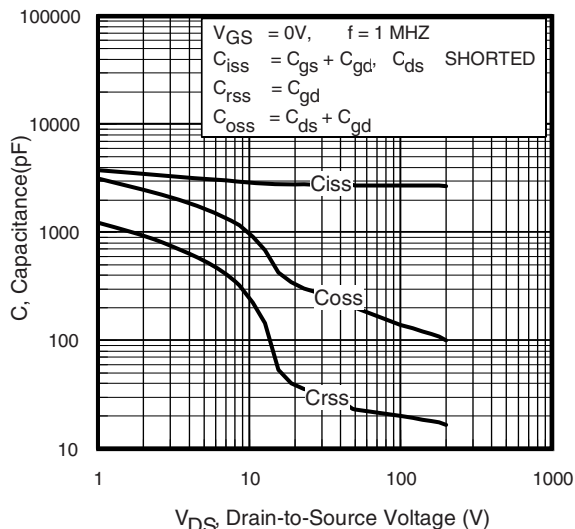


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

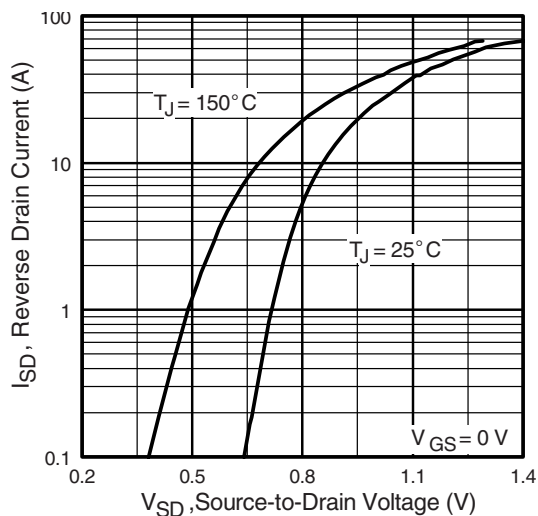


Fig. 7 - Typical Source-Drain Diode Forward Voltage

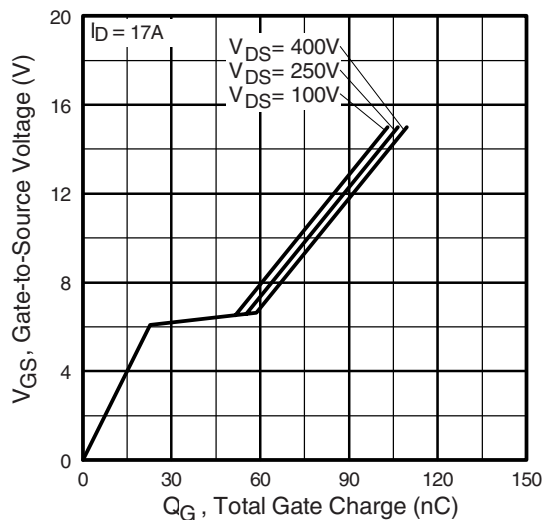


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

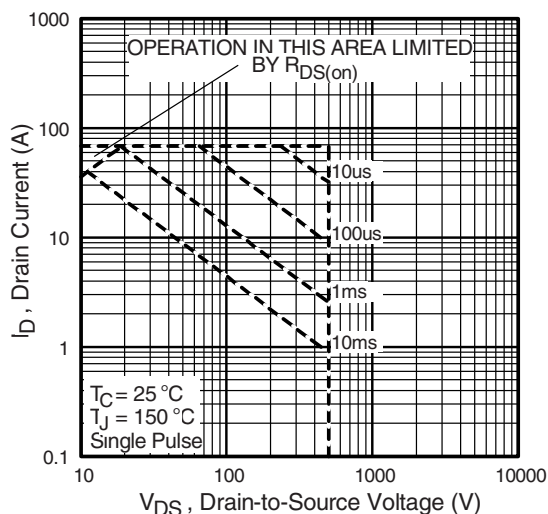
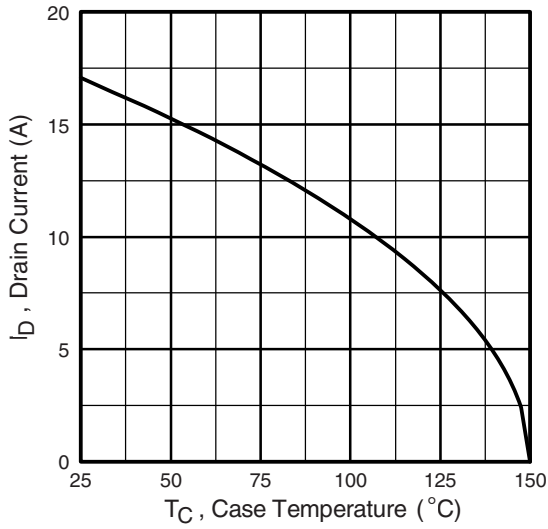
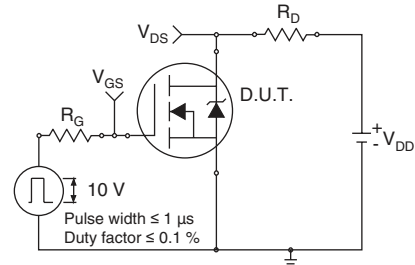


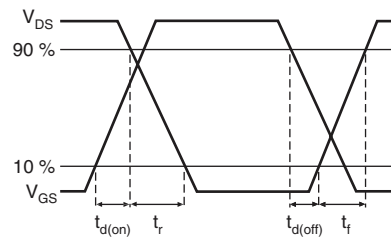
Fig. 8 - Maximum Safe Operating Area



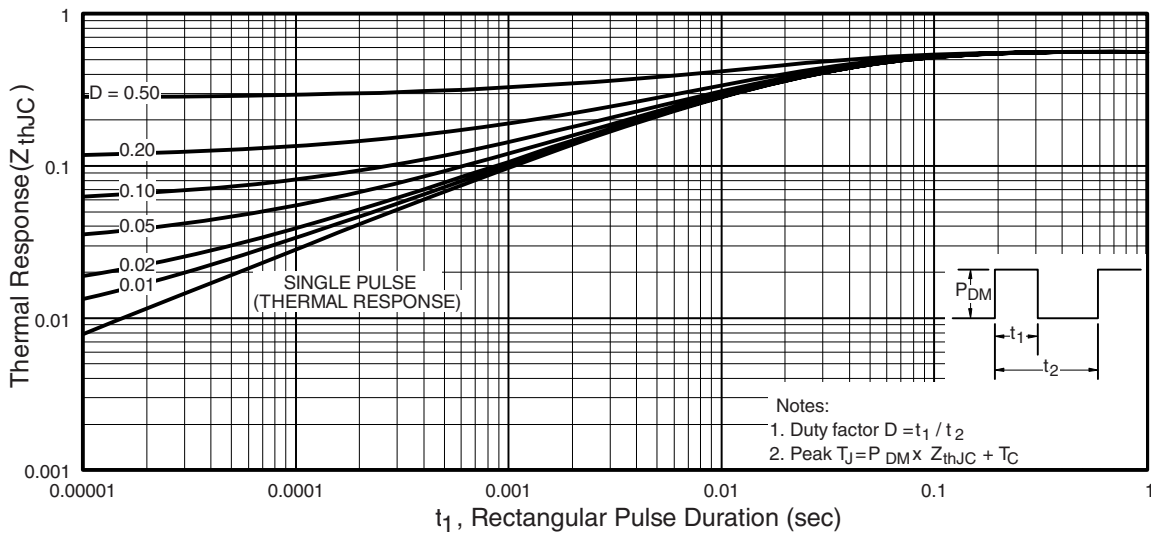
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



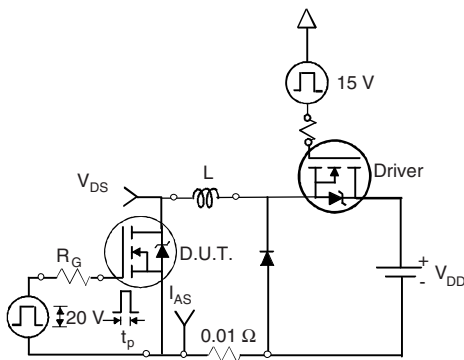
**Fig. 10a - Switching Time Test Circuit**



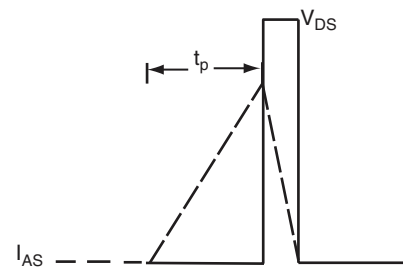
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

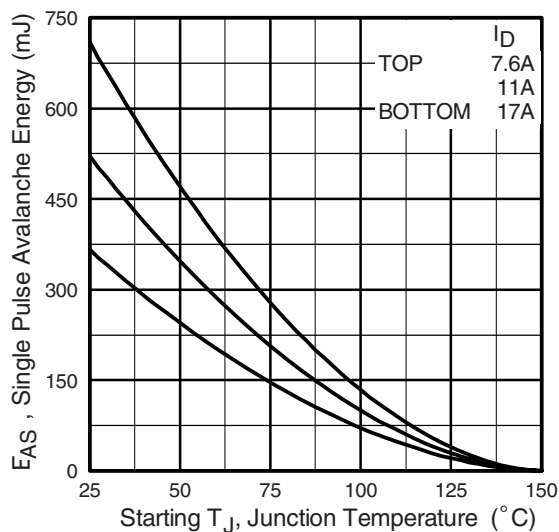


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

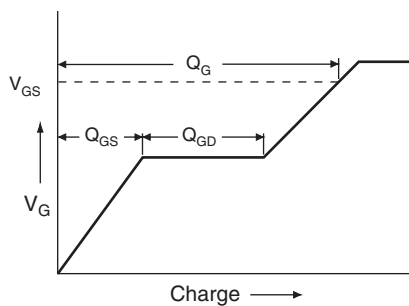


Fig. 13a - Basic Gate Charge Waveform

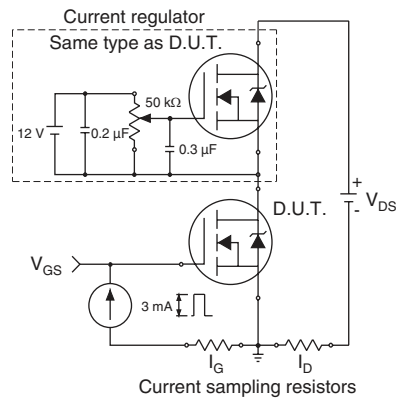


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit

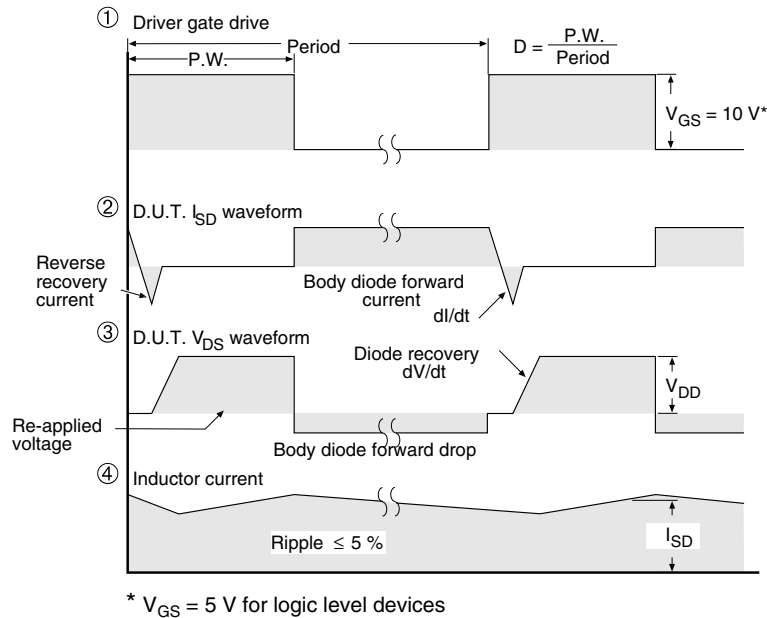
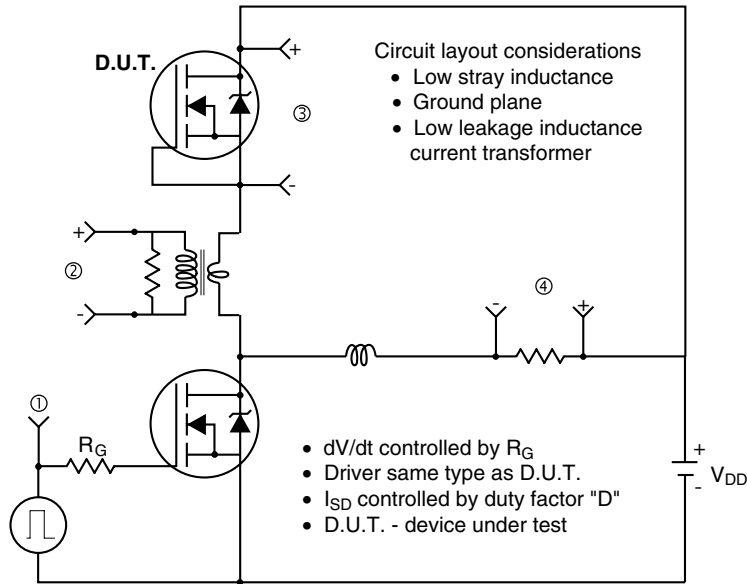
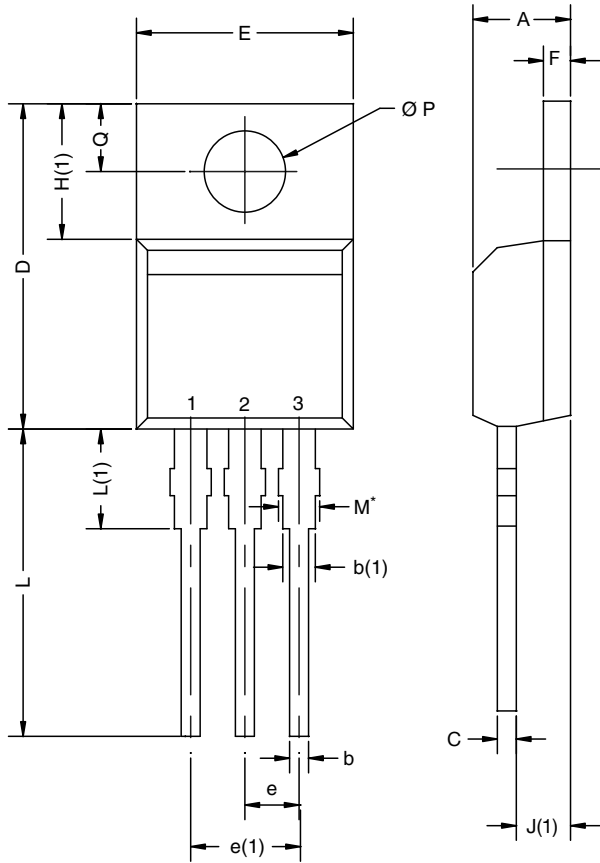


Fig. 14 - For N-Channel

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TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T13-0724-Rev. O, 14-Oct-13  
DWG: 5471

Note

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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