19-4368; Rev 1; 4/09

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5500/MAX5501 integrate four low-power, 12-bit digital-to analog converters (DACs) and four precision output amplifiers in a small, 20-pin package. Each negative input of the four precision amplifiers is externally accessible providing flexibility in gain configurations, remote sensing, and high output drive capacity, making the MAX5500/MAX5501 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC provides a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input register. The serial interface is compatible with SPI™/QSPI™/MICROWIRE™. The serial interface allows the input and DAC registers to be updated independently or simultaneously with a single software command. The 3-wire interface simultaneously updates the DAC registers. All logic inputs are TTL/CMOS-logic compatible. The MAX5500 operates from a single +5V power supply, and the MAX5501 operates from a single +3V power supply. The MAX5500/MAX5501 are specified over the extended -40°C to +105°C temperature range.

Applications

Industrial Process Controls
Automatic Test Equipment
Microprocessor (µP)-Controlled Systems
Motion Control
Digital Offset and Gain Adjustment
Remote Industrial Controls

Features

- **Four 12-Bit DACs with Configurable Output Amplifiers**
- **+5V or +3V Single-Supply Operation**
- **Low Supply Current:**
  0.85mA Normal Operation
  10µA Shutdown Mode (MAX5500)
- **Force-Sense Outputs**
- **Power-On Reset Clears All Registers and DACs to Zero**
- **Capable of Recalling Last State Prior to Shutdown**
- **SPI/QSPI/MICROWIRE Compatible**
- **Simultaneous or Independent Control of DACs through 3-Wire Serial Interface**
- **User-Programmable Digital Output**
- **Guaranteed Over Extended Temperature Range (-40°C to +105°C)**

Ordering Information

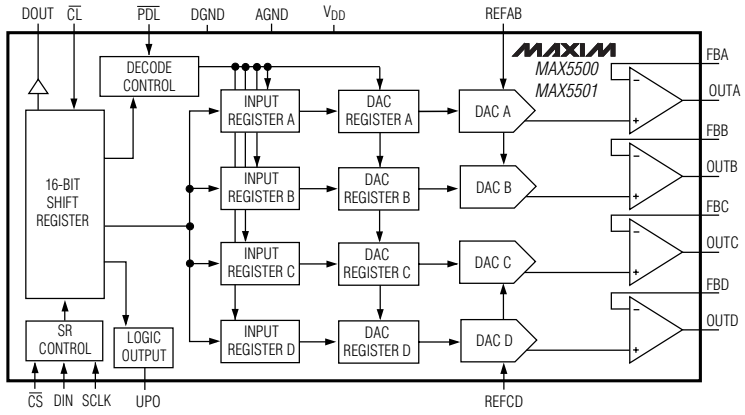
PART	PIN-PACKAGE	INL (LSB)	SUPPLY (V)
MAX5500AGAP+	20 SSOP	±0.75	+5
MAX5500BGAP+	20 SSOP	±2	+5
MAX5501AGAP+	20 SSOP	±0.75	+3
MAX5501BGAP+	20 SSOP	± 2	+3

+Denotes a lead(Pb)-free/RoHS-compliant package.

Note: *All devices are specified over the -40°C to +105°C operating temperature range.*

Pin Configuration appears at end of data sheet.

Functional Diagram



SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor, Corp.

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX5500 (V_{DD} = +5V ±10%, V_{REFAB} = V_{REFCD} = 2.5V), MAX5501 (V_{DD} = +3V to +3.6V, V_{REFAB} = V_{REFCD} = 1.25V), V_{AGND} = V_{DGND} = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Analog Section)						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5500A/MAX5501A		±0.25	±0.75	LSB
		MAX5500B/MAX5501B			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±3.5	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE	MAX5500		-0.3	±2.0	LSB
		MAX5501		-0.7	±4.0	
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	MAX5500		100	600	µV/V
		MAX5501		100	300	
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE	MAX5500		-0.3	±2.0	LSB
		MAX5501		-0.85	±4.0	
Offset Error	V_{OS}			±1.0	±3.5	mV
Integral Nonlinearity	INL	(Note 1)		±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555H	8			kΩ
Reference Current in Shutdown				0.01	±1.0	µA
DIGITAL INPUTS						
Input High Voltage	V_{IH}	MAX5500A/MAX5500B	2.4			V
		MAX5501A/MAX5501B	2.0			
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}		±0.1	±1.0	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS (continued)

(MAX5500 (V_{DD} = +5V ±10%, V_{REFAB} = V_{REFCD} = 2.5V), MAX5501 (V_{DD} = +3V to +3.6V, V_{REFAB} = V_{REFCD} = 1.25V), V_{AGND} = V_{DGND} = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5 LSB, V_{STEP} = 2.5V MAX5500A/MAX5500B		12		µs
		To ±0.5 LSB, V_{STEP} = 1.25V MAX5501A/MAX5501B		16		
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		±0.01	±1.0	µA
Startup Time Exiting Shutdown Mode		MAX5500A/MAX5500B		15		µs
		MAX5501A/MAX5501B		20		
Digital Feedthrough		$\overline{CS}$ =V_{DD}, f_{IN} = 100kHz		5		nV•s
Digital Crosstalk				5		nV•s
POWER SUPPLIES						
Supply Voltage	V_{DD}	MAX5500A/MAX5500B	4.5		5.5	V
		MAX5501A/MAX5501B	3.0		3.6	
Supply Current	I_{DD}	(Note 3)		0.85	1.1	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(MAX5500 (V_{DD} = +5V ±10%, V_{REFAB} = V_{REFCD} = 2.5V), MAX5501 (V_{DD} = +3V to +3.6V, V_{REFAB} = V_{REFCD} = 1.25V), V_{AGND} = V_{DGND} = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

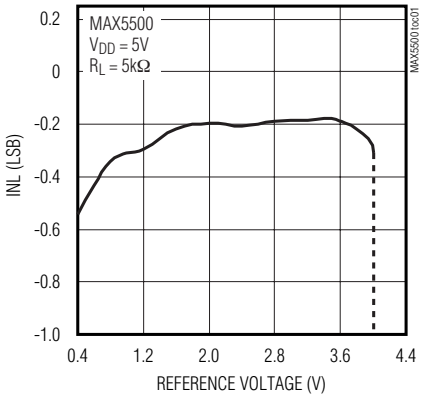
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF	MAX5500			80	ns
			MAX5501			120	
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF	MAX5500			80	ns
			MAX5501			120	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}			40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}			40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}			100			ns

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Accuracy is better than 1.0 LSB for V_{OUT} = 6mV to (V_{DD} - 60mV), guaranteed by PSR test on endpoints.
Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

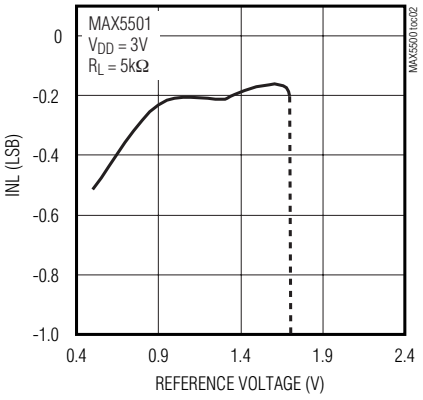
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

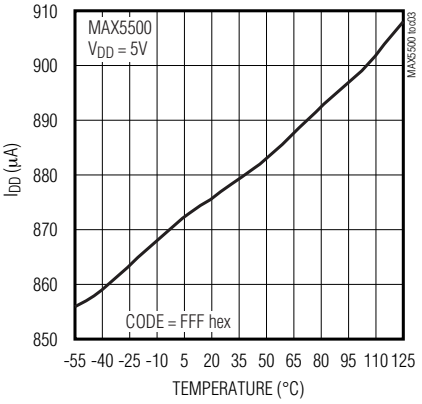
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



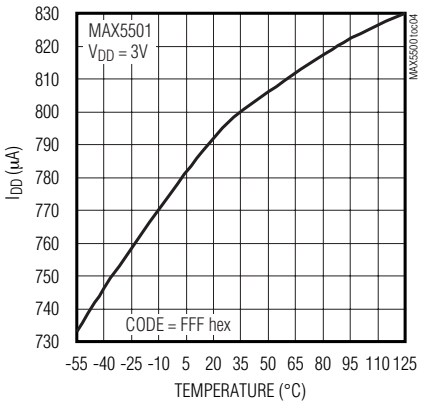
SUPPLY CURRENT vs. TEMPERATURE



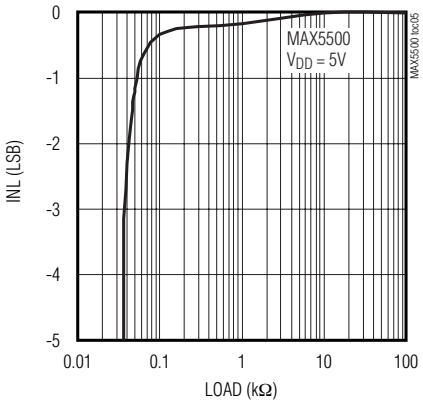
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

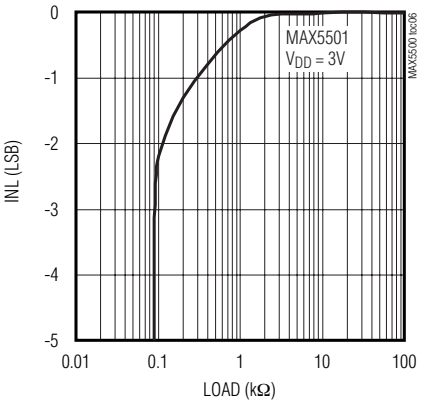
SUPPLY CURRENT vs. TEMPERATURE



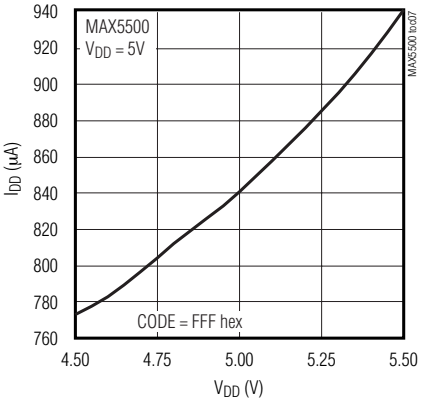
FULL-SCALE ERROR vs. LOAD



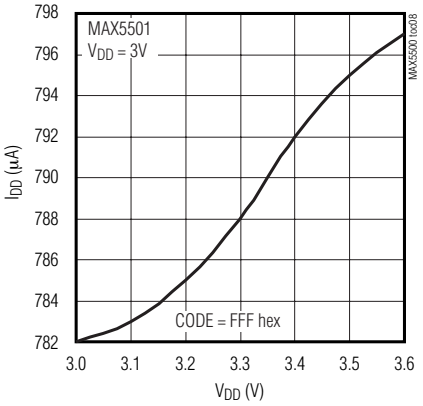
FULL-SCALE ERROR vs. LOAD



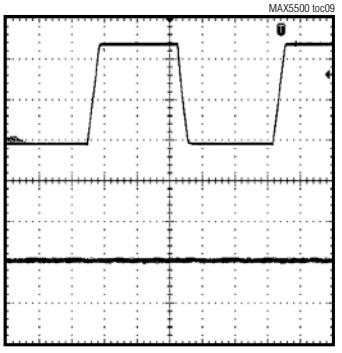
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

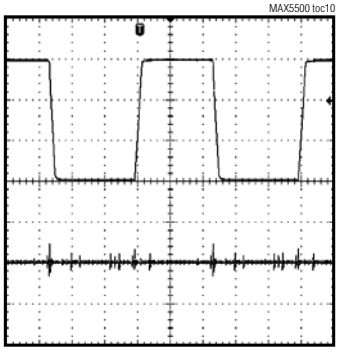


ANALOG CROSSTALK 5V



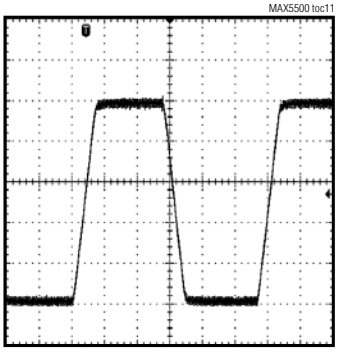
V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
DACA CODE SWITCHING FROM 00C hex TO FCC hex
DACB CODE SET TO 800 hex

ANALOG CROSSTALK 3V



V_{REF} = 1.5V, R_L = 5kΩ, C_L = 100pF
DACA CODE SWITCHING FROM 00C hex TO FFF hex
DACB CODE SET TO 800 hex

DYNAMIC RESPONSE 5V



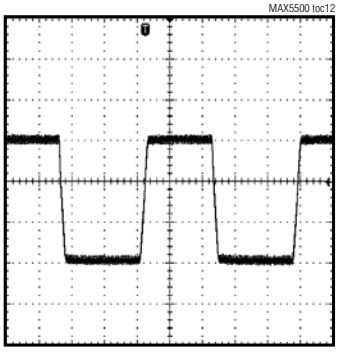
V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

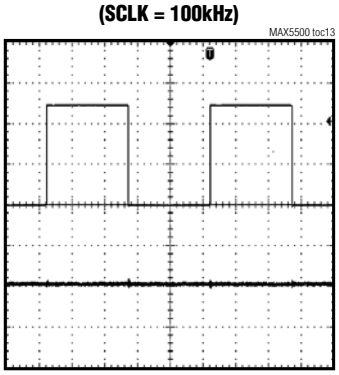
(T_A = +25°C, unless otherwise noted.)

DYNAMIC RESPONSE 3V



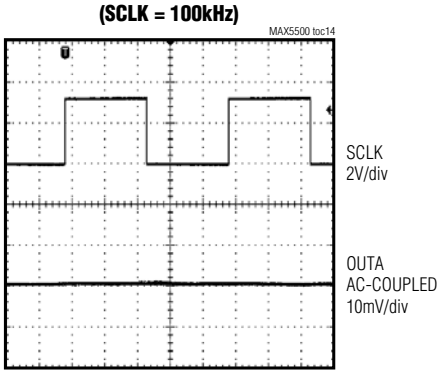
V_{REF} = 1.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +1

DIGITAL FEEDTHROUGH 3V (SCLK = 100kHz)



V_{REF} = 1.5V, R_L = 5kΩ, C_L = 100pF
$V_{\overline{CS}}$ = $V_{\overline{PDL}}$ = $V_{\overline{CL}}$ = 3.3V, V_{DIN} = 0V
DACA CODE SET TO 800 hex

DIGITAL FEEDTHROUGH 5V (SCLK = 100kHz)



V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
$V_{\overline{CS}}$ = $V_{\overline{PDL}}$ = $V_{\overline{CL}}$ = 5V, V_{DIN} = 0V
DACA CODE SET TO 800 hex

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	DAC A/DAC B Reference Voltage Input
7	$\overline{CL}$	Active-Low Clear Input. $\overline{CL}$ clears all DACs and registers. $\overline{CL}$ resets all outputs (OUT_, UPO, and DOUT) to 0.
8	$\overline{CS}$	Active-Low Chip-Select Input
9	DIN	Serial Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Active-Low Power-Down Lockout. Drive $\overline{PDL}$ low to lock out software shutdown.
15	REFCD	DAC C/DAC D Reference Voltage Input
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

Detailed Description

The MAX5500/MAX5501 integrate four 12-bit, voltage-output digital-to-analog converters (DACs) that are addressed through a simple 3-wire serial interface. The devices include a 16-bit data-in/data-out shift register. Each internal DAC provides a doubled-buffered input composed of an input register and a DAC register (see the *Functional Diagram*). The negative input of each amplifier is externally accessible.

The DACs are inverted rail-to-rail ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB input, while DACs C and D share the REFCD input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for the two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times NB/4096) \times Gain$$

where NB is the numeric value of the binary input code (0 to 4095) of the DAC. V_{REF} is the reference voltage. Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference accept an input code of 555 hex, to a high value exceeding giga-ohms with an input code of 000 hex. The load regulation of the reference source affects the performance of the devices as the input impedance at the reference inputs is code dependent. The REFAB and REFCD reference inputs provide a 10kΩ guaranteed minimum input impedance. When the same voltage source drives the two reference inputs, the effective minimum impedance is 5kΩ. A voltage reference with an excellent load regulation of 0.0002mV/mA, such as the MAX6033, is capable of driving both reference inputs simultaneously at 2.5V. Driving REFAB and REFCD separately improves reference accuracy.

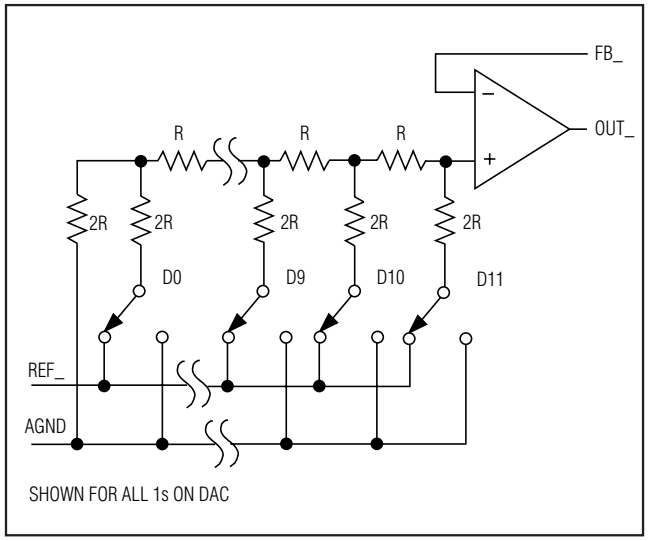


Figure 1. Simplified DAC Circuit Diagram

The REFAB and REFCD inputs enter a high-impedance state, with a typical input leakage current of 0.02µA, when the MAX5500/MAX5501 are in shutdown. The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the output, the typical settling time to within ±0.5 LSB is 12µs when the output is loaded with 5kΩ in parallel with 100pF. A load of less than 2kΩ at the output degrades performance. See the *Typical Operating Characteristics* for the output dynamic responses and settling performances of the amplifiers.

Power-Down Mode

The MAX5500/MAX5501 feature a software-programmable shutdown that reduces supply current to a typical value of 10µA. Drive PDL high to enable the shutdown mode. Write 1100XXXXXXXXXXX as the input-control word to put the device in power-down mode (Table 1).

In power-down mode, the output amplifiers and the reference inputs enter a high-impedance state.

The serial interface remains active. Data in the input registers is retained in power-down, allowing the devices to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. Allow 15µs for the outputs to stabilize when powering up the devices or bringing the devices out of shutdown.

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Serial-Interface Configurations

The MAX5500/MAX5501s' 3-wire serial interface is compatible with both MICROWIRE (Figure 2) and SPI/QSPI (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX5500/MAX5501s' response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the shift register can be shifted out of DOUT and returned to the µP for data verification.

The digital inputs of the MAX5500/MAX5501 are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX5500/MAX5501 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are don't-care bits. Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 12 data bits D11–D0 (Figure 4). The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out through the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the device is to enter shutdown mode (assuming $\overline{PDL}$ is high)
- How the device is configured when exiting out of shutdown mode

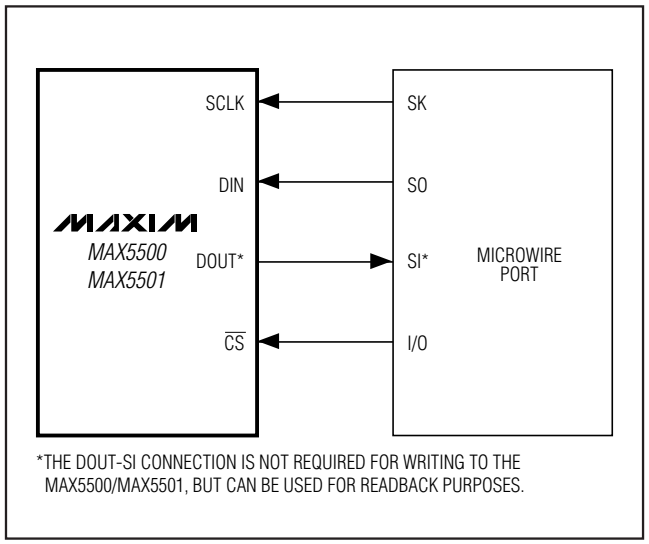


Figure 2. Connections for MICROWIRE

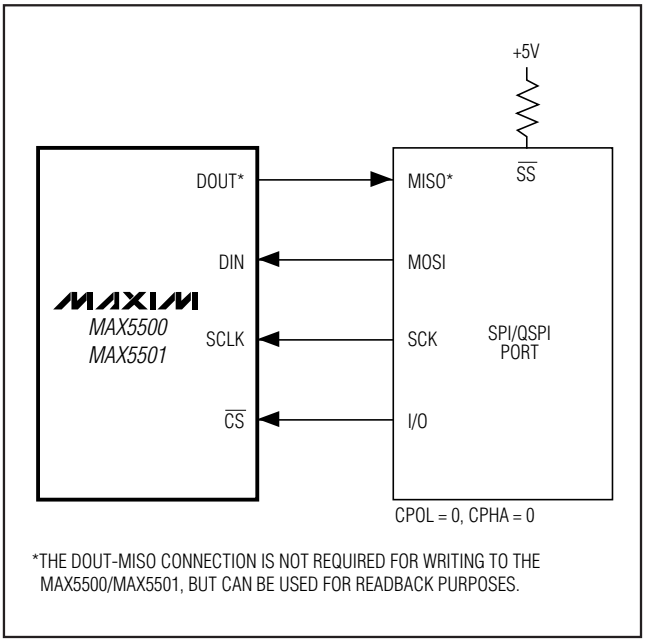


Figure 3. Connections for SPI/QSPI

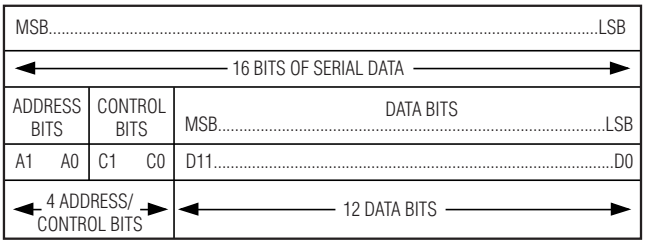


Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.....D0 MSB LSB	
0	0	0	1	12-bit DAC data	Load input register A; DAC registers unchanged.
0	1	0	1	12-bit DAC data	Load input register B; DAC registers unchanged.
1	0	0	1	12-bit DAC data	Load input register C; DAC registers unchanged.
1	1	0	1	12-bit DAC data	Load input register D; DAC registers unchanged.
0	0	1	1	12-bit DAC data	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (startup).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (startup).
1	1	0	0	XXXXXXXXXXXX	Shutdown (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

Figure 5 shows the serial-interface timing requirements. The $\overline{CS}$ input must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low for at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register through the serial data input (DIN) on the rising edge of SCLK. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate input/DAC registers on the rising edge of $\overline{CS}$.

The programming command "load-all-dacs-from-shift-register" allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected. This feature is used in a daisy-chain configuration (see the *Daisy Chaining Devices* section).

The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX5500/MAX5501 can be programmed so that data is clocked out of DOUT on the rising edge of SCLK (mode 1) or the falling edge (mode 0). In mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with MICROWIRE, SPI/QSPI, and other serial interfaces. In mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled through the MAX5500/MAX5501 serial interface (Table 1).

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

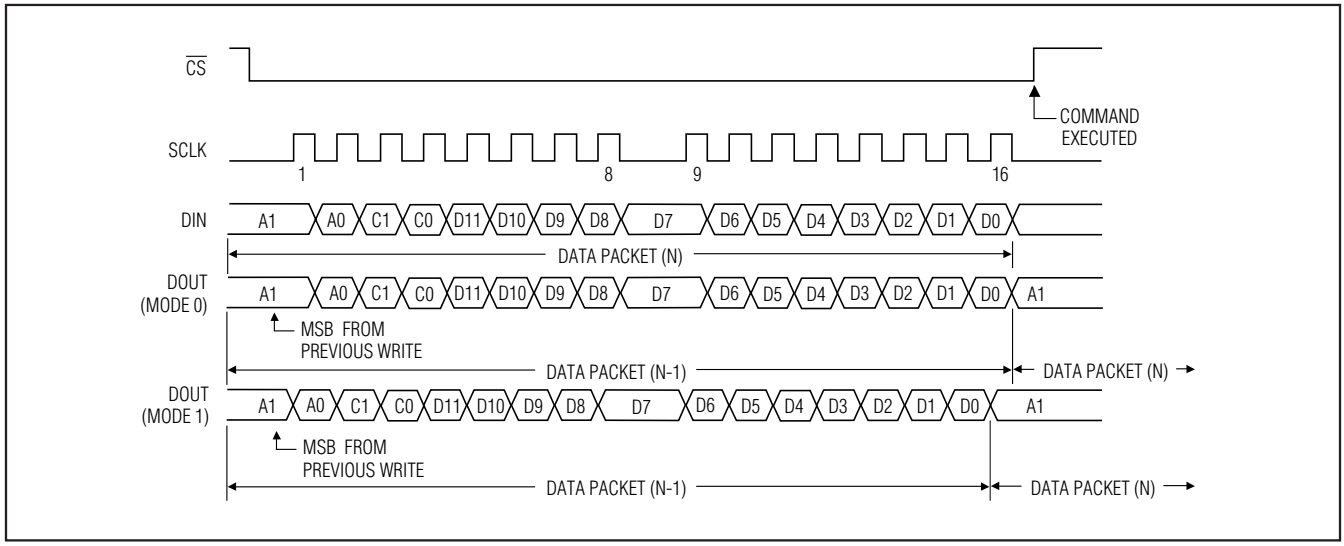


Figure 5. Serial-Interface Timing Diagram

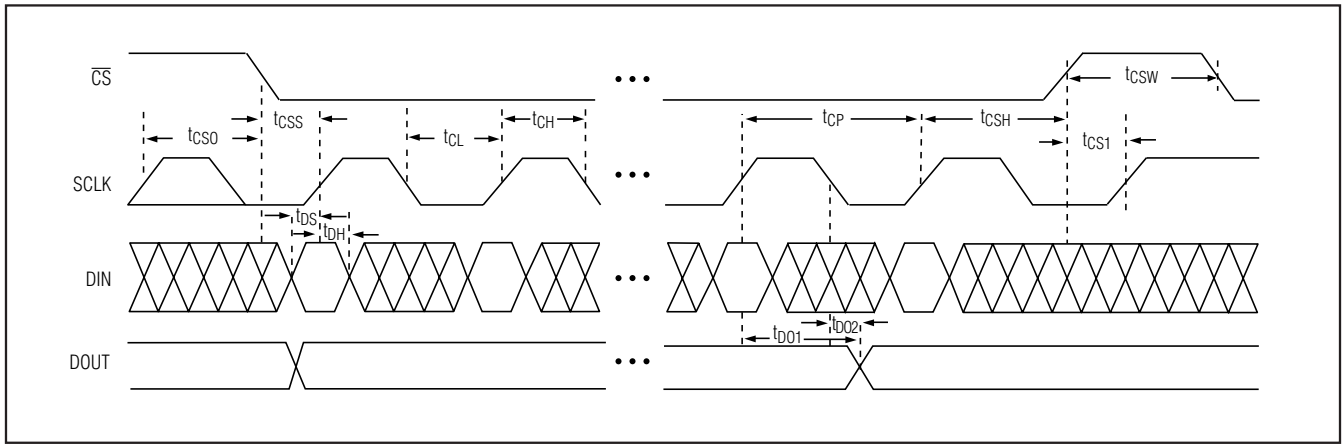


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout ($\overline{PDL}$)

Drive power-down lockout, $\overline{PDL}$, low to disable software shutdown. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the device with the output set to the state prior to shutdown. Use $\overline{PDL}$ to asynchronously wake up the device.

Daisy Chaining Devices

The MAX5500/MAX5501 can be daisy chained by connecting DOUT of one device to DIN of another device (Figure 7).

Each DOUT output of the MAX5500/MAX5501 includes an internal active pullup. The sink/source capability of DOUT determines the time required to discharge/charge a capacitive load. See the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Figure 8 shows an alternate method of connecting several MAX5500/MAX5501 devices. In this configuration, the data bus is common to all devices. Data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

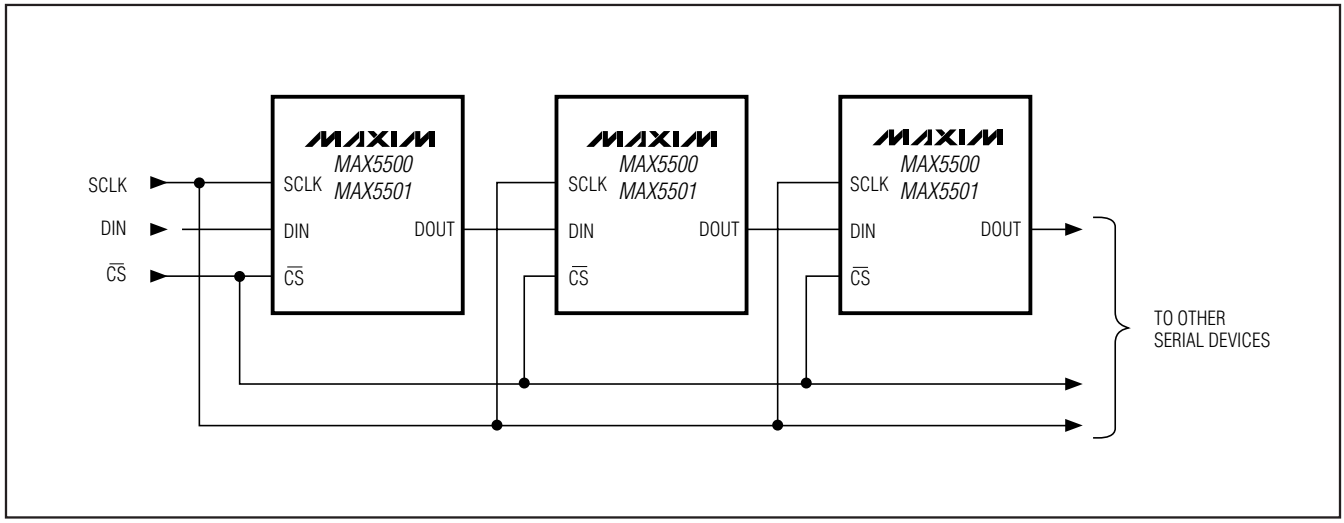


Figure 7. Daisy Chaining MAX5500/MAX5501

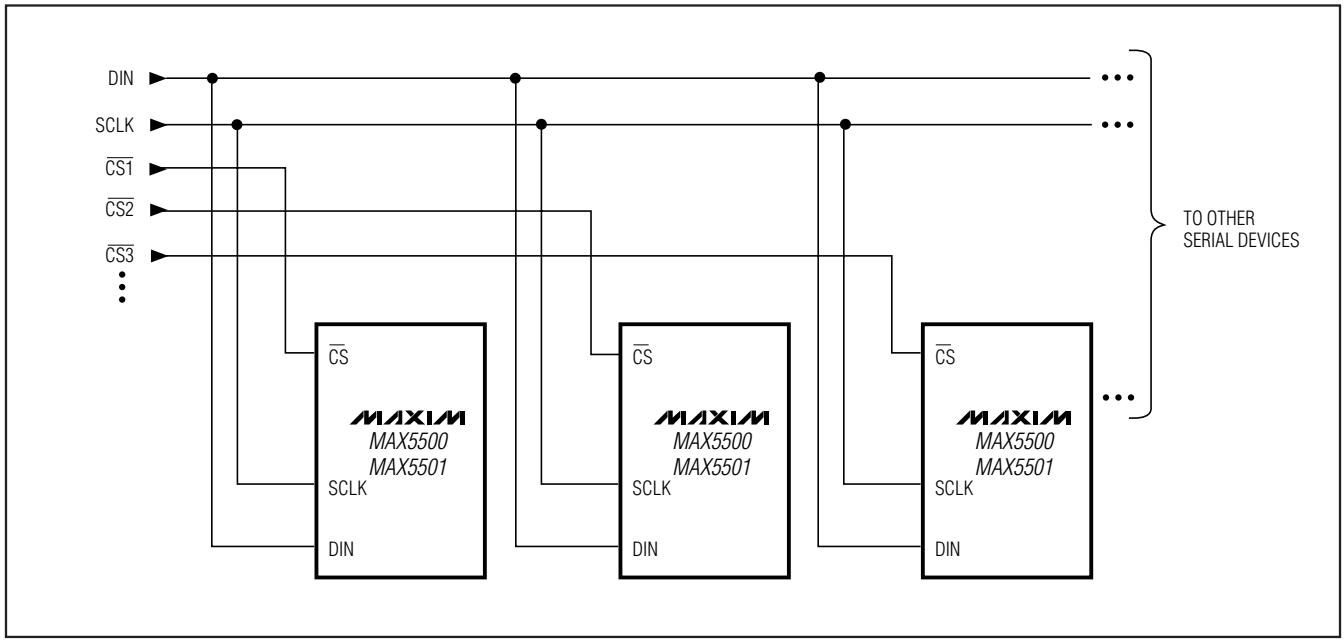


Figure 8. Multiple MAX5500/MAX5501 Devices Sharing a Common DIN Line

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs are of the same polarity. Figure 9 shows the MAX5500/MAX5501 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

See Figure 10 for rail-to-rail outputs. Figure 10 shows the MAX5500/MAX5501 with the output amplifiers configured with a closed-loop gain of +2 to provide 0 to 5V full-scale range with a 2.5V external reference voltage.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000	0000	0000	$+V_{REF}\left(\frac{2048}{4096}\right)=\frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000	0000	0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000	0000	0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)=-V_{REF}$

Note: 1 LSB = $(V_{REF})\left(\frac{1}{4096}\right)$

Bipolar Output

Figure 11 shows the MAX5500/MAX5501 configured for bipolar operation.

$$V_{OUT} = V_{REF}[(2NB/4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for the circuit of Figure 11.

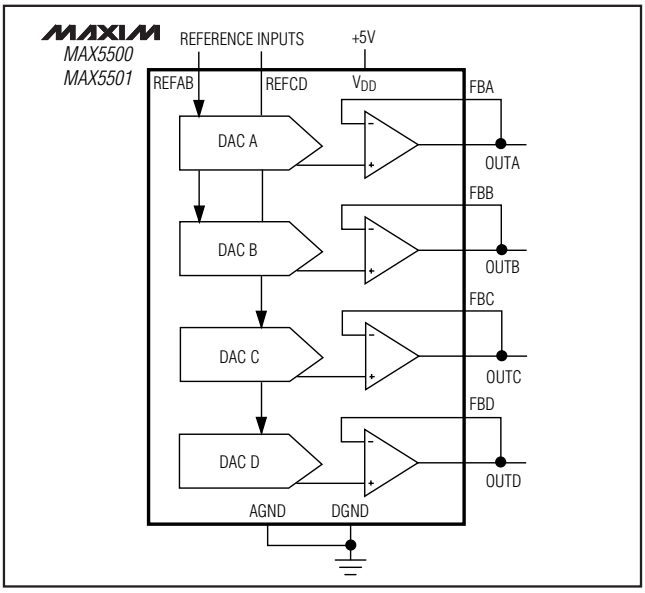


Figure 9. Unipolar Output Circuit

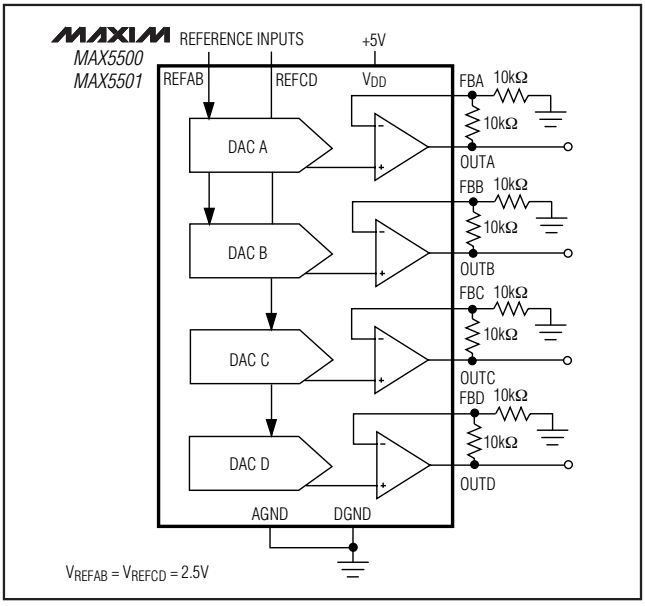


Figure 10. Unipolar Rail-to-Rail Output Circuit

Digitally Programmable Current Source

The circuit of Figure 12 places an npn transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit drives 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF}/R) \times (NB/4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and D_{OUT} is in mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

For rated MAX5500/MAX5501 performance, limit V_{REFAB}/V_{REFCD} to 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close as possible to the supply inputs.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND create noise at the analog outputs. Connect AGND and DGND together at the DAC, and then connect this point to the highest-quality ground available. Good PCB ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Do not use wire-wrapped boards.

Chip Information

PROCESS: BiCMOS

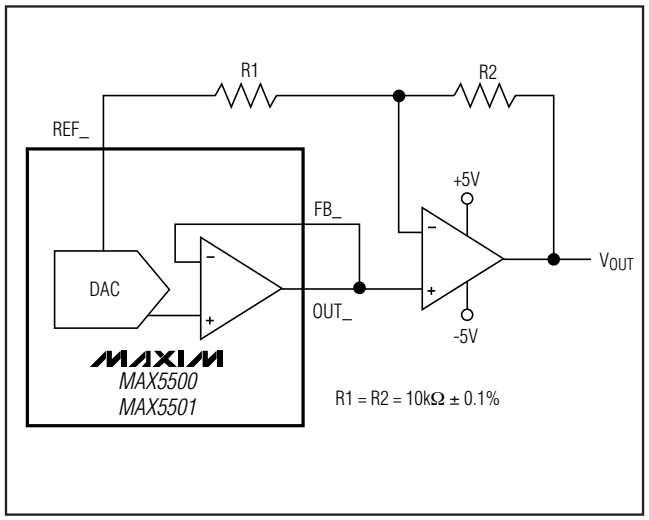


Figure 11. Bipolar Output Circuit

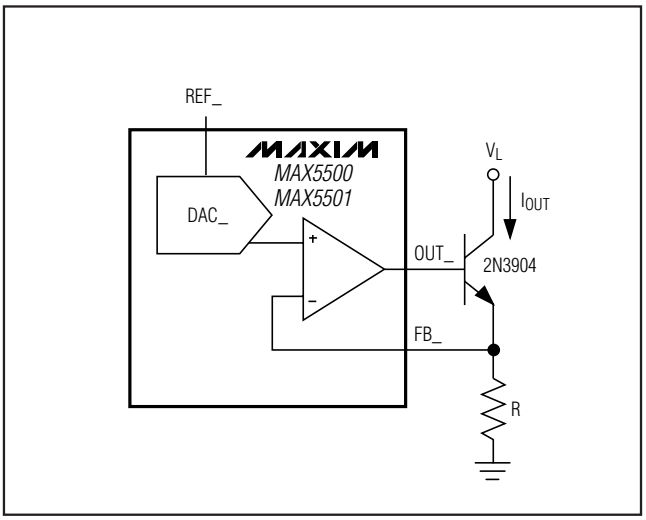
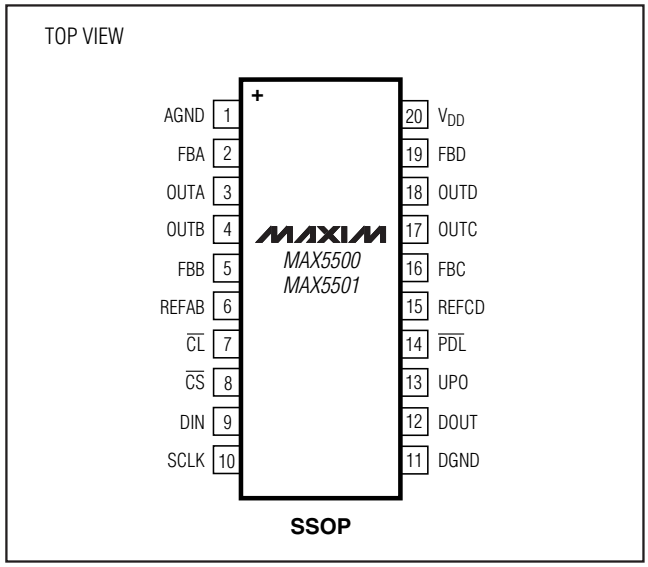


Figure 12. Digitally Progammable Current Source

Low-Power, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 SSOP	A20-2	**21-0056**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/08	Initial release	—
1	4/09	Removed future product asterisk from MAX5501 in *Ordering Information* table and updated *Electrical Characteristics* table	1–4