FAIRCHILD SEMICONDUCTOR®

74LVXC3245
8-Bit Dual Supply Configurable Voltage Interface Transceiver with 3-STATE Outputs

Features

- Dire tio a i ter a e et ee a to e
- o tro i p t o pati e it e e
- tp t o r e i p to
- ara tee i ta eo it i oi e e e a y a i t re o per or a e
- p e e t proprietary re tio ir itry
- e i e operati ra e
- o ort a to oat i ta eo y e i o

General Description

e i a pi a pply it o i ra e ota e i ter a e tra ei er ite or a ot er rea ti e o i ra e app i atio e pi a ept a pply e e e ort i a e i ate port e pi a ept a to pply e e e ort i o i re to tra t e pply e e re pe ti e y e e o t e pi i o i re t e pi at a e a a i o i re t e pi at a e e ort o i ter a e it a o t y te a t e ort to t e ar ot i e i e i a o t e ota e or e pi a pi o t e ort to oat e i eat re i e e ary to er ata to a ro a o et t at per it ar to e i erte a re o e ri or a operatio

Ordering Code:

Order Number	Package Number	Package Description
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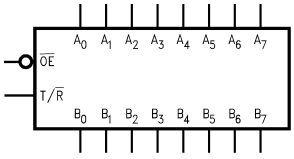
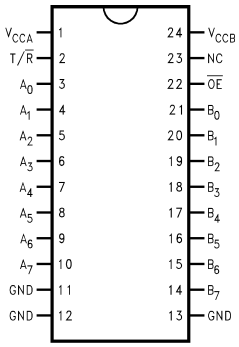
		ea i ri a ti e a a e e i e

e i e a o a ai a e i ape a ee pe i y y appe i i etter to t e or eri o e

Logic Symbol/s



Connection Diagram/s



Pin Descriptions

Pin Names	Description
	tp t a e p t
	ra it e ei e p t
	i e p t or tp t
	i e p t or tp t

Truth Table/s

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus □□□ata□to□□□□□
L	H	Bus □□□ata□to□□□□□
H	X	HIGH □□□□tate

H □=□□□□ □ □□o□ta□e□□e□e□
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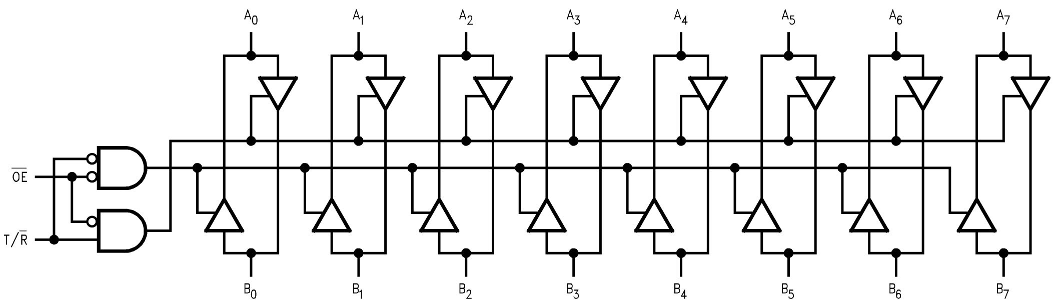
Logic Diagram/s



Absolute Maximum Ratings [illegible]

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Recommended Operating Conditions [illegible]

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Note 1: [illegible]

Note 2: [illegible]

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = −40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
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DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	$T_A = 25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
I_{OZA}	Maximum 3-STATE Output Leakage @ A_n		3.6	3.6		±0.5	±5.0	µA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND
			3.6	5.5		±0.5	±5.0		
I_{OZB}	Maximum 3-STATE Output Leakage @ B_n		3.6	3.6		±0.5	±5.0	µA	$V_I = V_{IL}, V_{IH}$, $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
			3.6	5.5		±0.5	±5.0		
ΔI_{CC}	Maximum I_{CC}/Input	B_n	3.6	5.5	1.0	1.35	1.5	mA	$V_I = V_{CCB}-2.1V$
		All Inputs	3.6	3.6		0.35	0.5		$V_I = V_{CC}-0.6V$
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		3.6	Open		5	50	µA	$A_n = V_{CCA}$ or GND B_n = Open, $\overline{OE} = V_{CCA}$, $T/\overline{R} = V_{CCA}$, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		3.6	3.6		5	50	µA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, $T/\overline{R}$ = GND
			3.6	5.5		5	50		
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6	3.6		5	50	µA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, $T/\overline{R} = V_{CCA}$
			3.6	5.5		8	80		
V_{OLPA}	Quiet Output		3.3	3.3		0.8		V	(Note 3)(Note 4)
	Maximum Dynamic		3.3	5.0		0.8			
V_{OLPB}	V_{OL}		3.3	3.3		0.8		V	(Note 3)(Note 4)
			3.3	5.0		1.5			
V_{OLVA}	Quiet Output		3.3	3.3		–0.8		V	(Note 3)(Note 4)
	Minimum Dynamic		3.3	5.0		–0.8			
V_{OLVB}	V_{OL}		3.3	3.3		–0.8		V	(Note 3)(Note 4)
			3.3	5.0		–1.2			
V_{IHDA}	Minimum HIGH Level Dynamic Input Voltage		3.3	3.3		2.0		V	(Note 3)(Note 5)
			3.3	5.0		2.0			
V_{IHDB}			3.3	3.3		2.0		V	(Note 3)(Note 5)
			3.3	5.0		3.5			
V_{ILDA}	Maximum LOW Level Dynamic Input Voltage		3.3	3.3		0.8		V	(Note 3)(Note 5)
			3.3	5.0		0.8			
V_{ILDB}			3.3	3.3		0.8		V	(Note 3)(Note 5)
			3.3	5.0		1.5			

Note 3: Worst case package.

Note 4: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 5: Max number of Data Inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V–3.6V$, $V_{CCB} = 4.5V–5.5V$			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V–3.6V$, $V_{CCB} = 4.5V–5.5V$		$T_A = +25°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V–3.6V$, $V_{CCB} = 3.0V–3.6V$			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V–3.6V$, $V_{CCB} = 3.0V–3.6V$		Units
		Min	Typ (Note 6)	Max	Min	Max	Min	Typ (Note 7)	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
t_{PLH}	A to B	1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
t_{PHL}	Propagation Delay	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
t_{PLH}	B to A	1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
t_{PZL}	Output Enable Time	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
t_{PZH}	$\overline{OE}$ to B	1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
t_{PZH}	$\overline{OE}$ to A	1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to B	1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
t_{PHZ}	Output Disable Time	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to A	1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
t_{OSHL}	Output to Output											
t_{OSLH}	Skew (Note 8)		1.0	1.5		1.5		1.0	1.5		1.5	ns
	Data to Output											

Note 6: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 5.0V$ @ 25°C.

Note 7: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 3.3V$ @ 25°C.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		10	pF	$V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$
C_{PD}	Power Dissipation	A→B	50	pF	$V_{CCB} = 5.0V$
	Capacitance (Note 9)	B→A	40	pF	$V_{CCA} = 3.3V$

Note 9: C_{PD} is measured at 10 MHz.

Power Up Considerations

To insure the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the V_{CCA} side.
- $\overline{OE}$ should ramp with or ahead of V_{CCA}. This will help guard against bus contention.
- The Transmit/Receive control pin (T/$\overline{R}$) should ramp with V_{CCA}, this will ensure that the A Port data pins are configured as inputs. With V_{CCA} receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.
- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

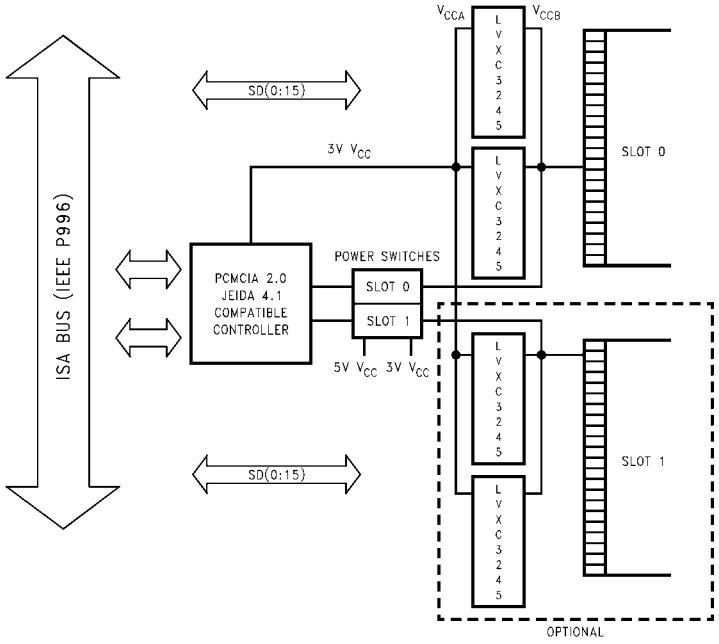
TABLE 1. Low Voltage Translator Power Up Sequencing Table

Device Type	V_{CCA}	V_{CCB}	T/$\overline{R}$	$\overline{OE}$	A Side I/O	B Side I/O	Floatable Pin Allowed
74LVXC3245	3V (power up 1st)	3V to 5.5V configurable	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	yes, V_{CCB} and B I/O's w/ $\overline{OE}$ HIGH

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.

Configurable I/O Application for PCMCIA Cards

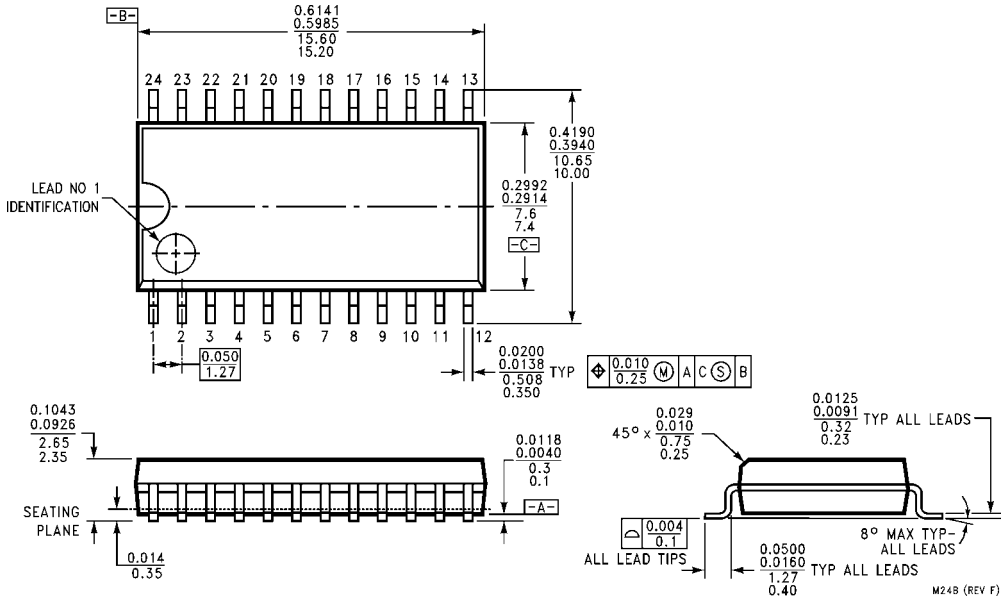
Block Diagram



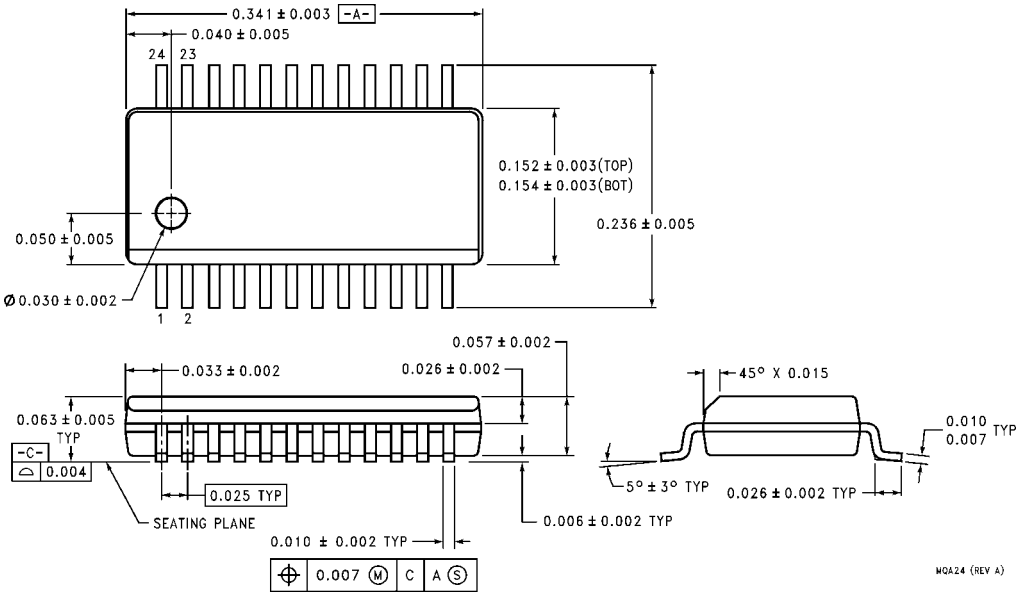
The LVXC3245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC3245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC3245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC3245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

Physical Dimensions inches (millimeters) unless otherwise noted

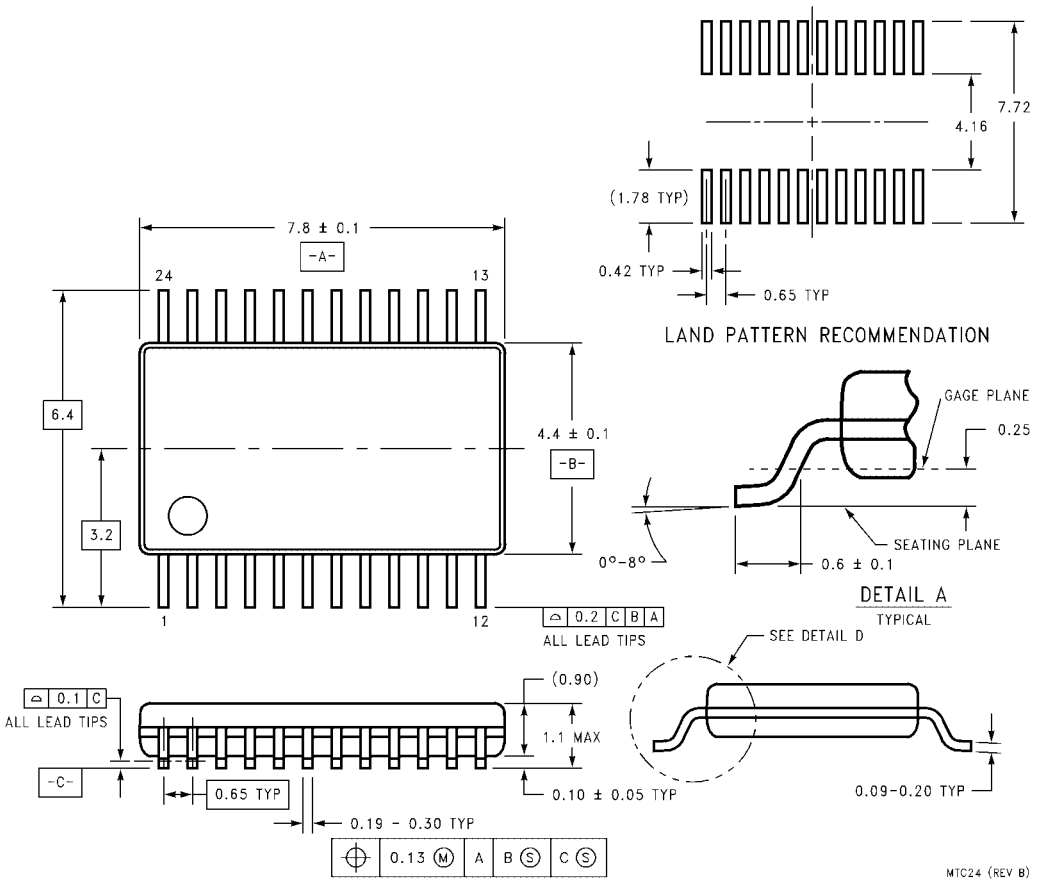


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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FRFET®
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SPM®
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SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
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TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
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ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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