

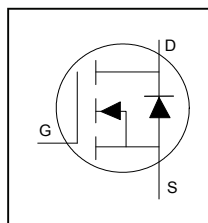
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

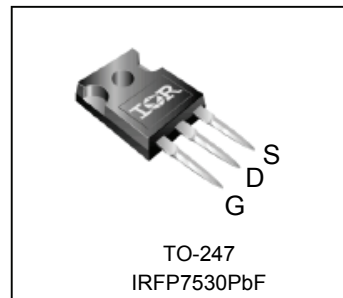
Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET



V_{DSS}	60V
R_{DS(on)} typ.	1.65mΩ
max	2.00mΩ
I_D (Silicon Limited)	281A①
I_D (Package Limited)	195A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP7530PbF	TO-247	Tube	25	IRFP7530PbF

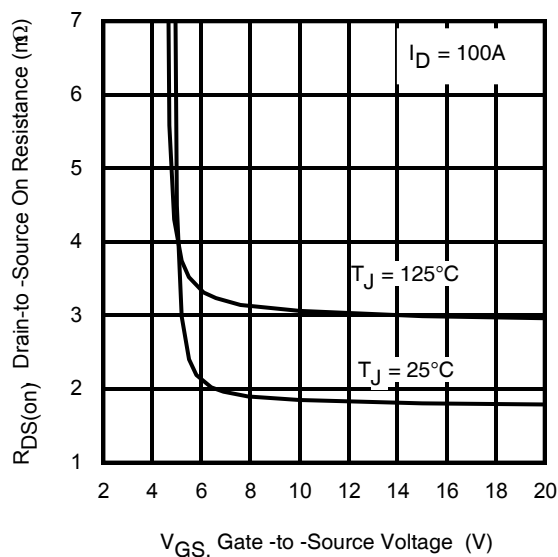


Fig 1. Typical On-Resistance vs. Gate Voltage

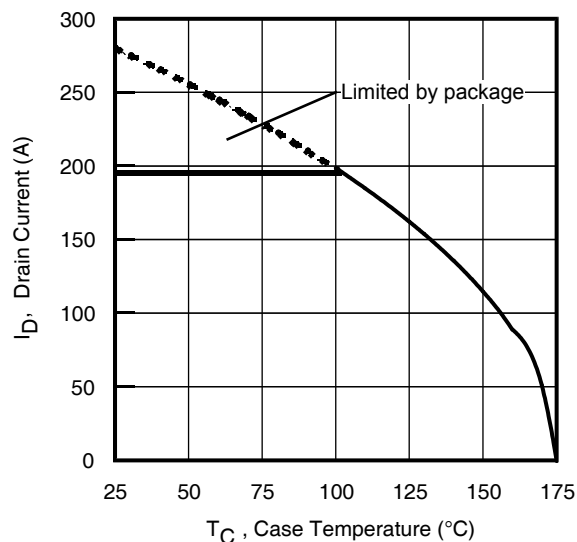


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	281①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	199①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	760	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	341	W
	Linear Derating Factor	2.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	557	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ④	865	
I_{AR}	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.44	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	47	—	mV/°C	Reference to 25°C , $I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.65	2.00	mΩ	$V_{GS} = 10\text{V}$, $I_D = 100\text{A}$
		—	2.10	—		$V_{GS} = 6.0\text{V}$, $I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	2.1	—	Ω	

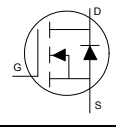
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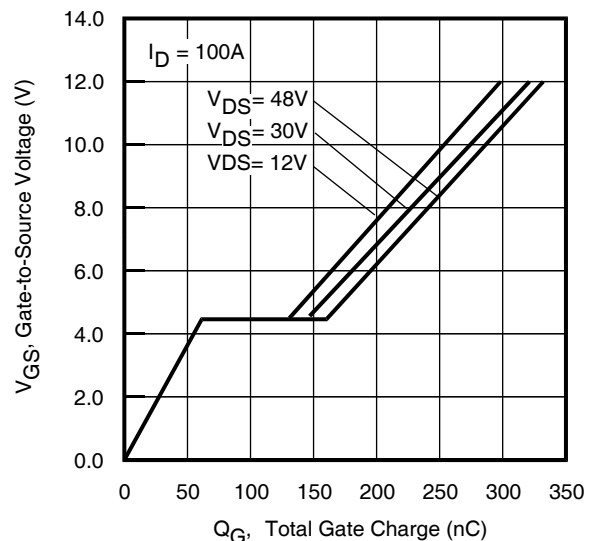
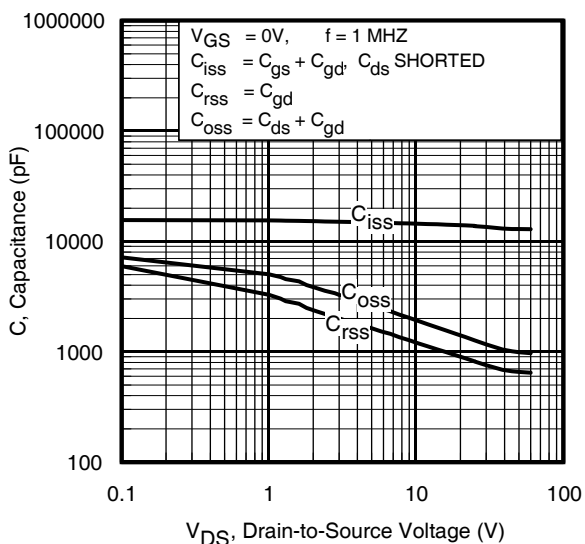
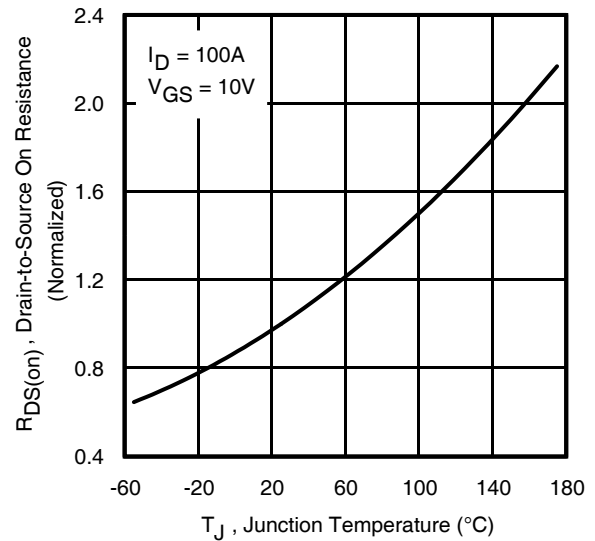
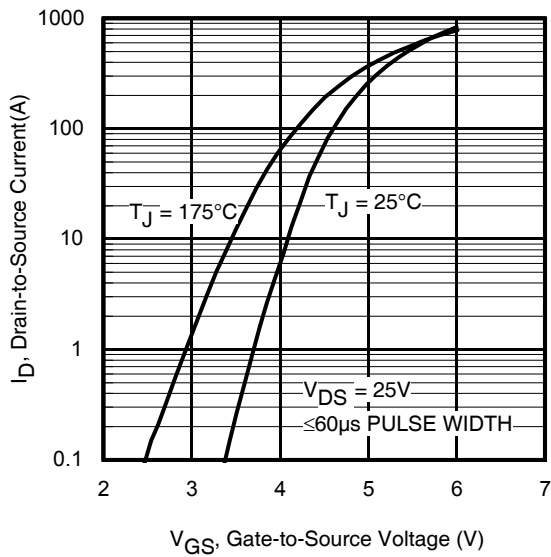
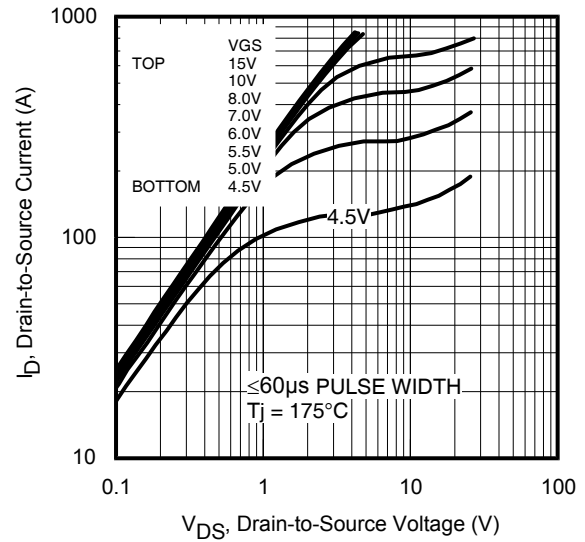
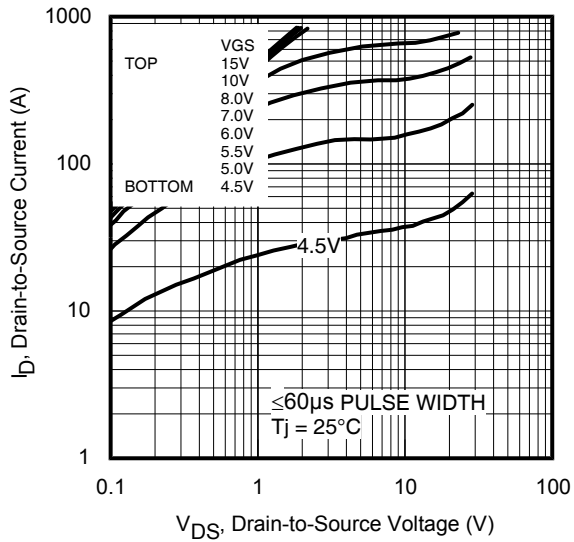
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 105\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.
- ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1338\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_{θ} is measured at T_J approximately 90°C .
- ⑨ This value determined from sample failure population, starting $T_J = 25^\circ\text{C}$, $L = 105\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.

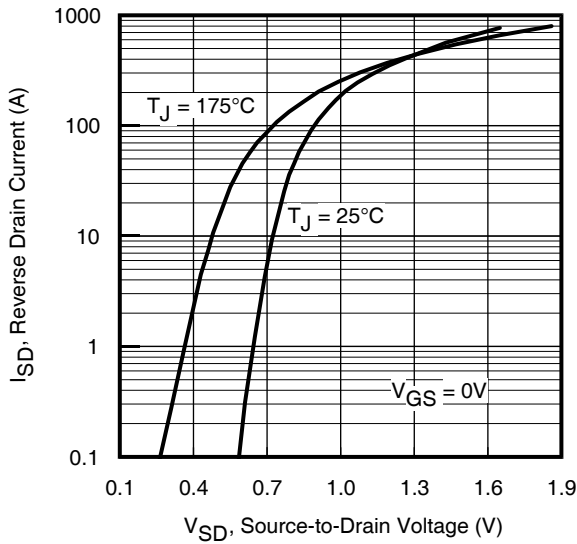
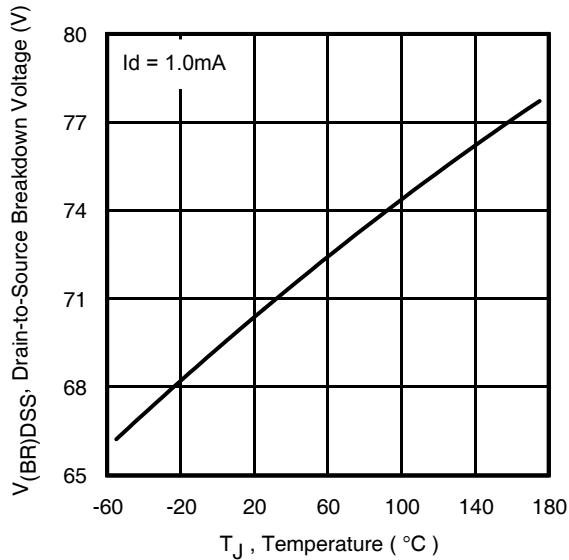
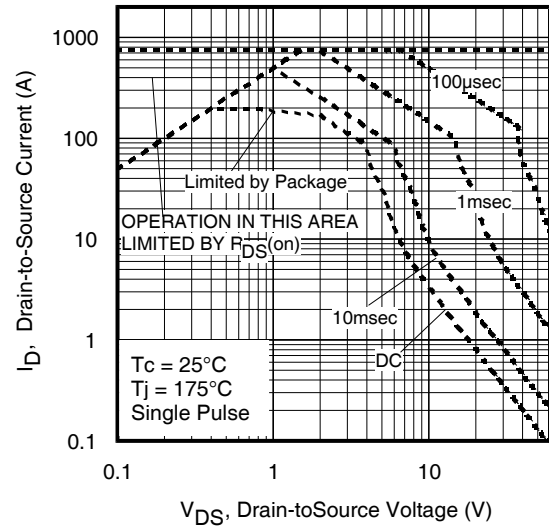
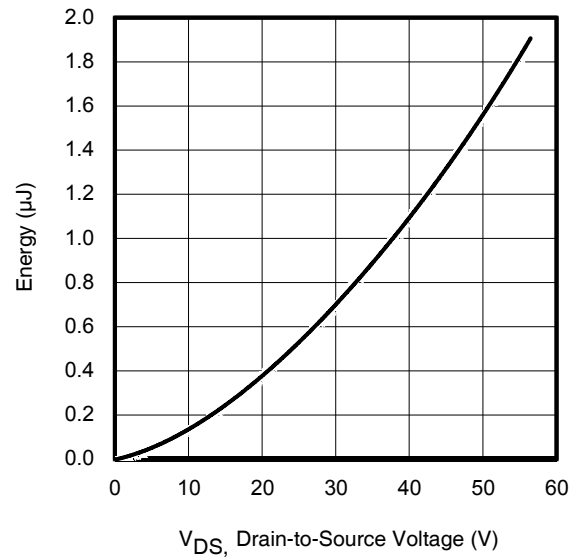
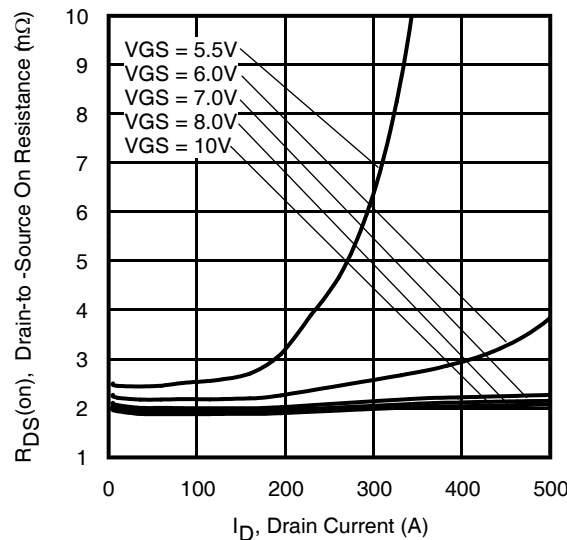
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	242	—	—	S	$V_{DS} = 10\text{V}$, $I_D = 100\text{A}$
Q_g	Total Gate Charge	—	274	411	nC	$I_D = 100\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$
Q_{gs}	Gate-to-Source Charge	—	64	—		
Q_{gd}	Gate-to-Drain Charge	—	83	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	191	—		
$t_{d(on)}$	Turn-On Delay Time	—	52	—	ns	$V_{DD} = 30\text{V}$ $I_D = 100\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}^{(5)}$
t_r	Rise Time	—	141	—		
$t_{d(off)}$	Turn-Off Delay Time	—	172	—		
t_f	Fall Time	—	104	—		
C_{iss}	Input Capacitance	—	13703	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$, See Fig.7 $V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $48\text{V}^{(7)}$ $V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $48\text{V}^{(6)}$
C_{oss}	Output Capacitance	—	1266	—		
C_{rss}	Reverse Transfer Capacitance	—	806	—		
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	1267	—		
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	1630	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	281 ⁽¹⁾	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⁽²⁾	—	—	760		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ⁽⁵⁾
dv/dt	Peak Diode Recovery dv/dt ⁽⁴⁾	—	8.1	—	V/ns	$T_J = 175^\circ\text{C}$, $I_S = 100\text{A}$, $V_{DS} = 60\text{V}$ ⁽⁵⁾
t_{rr}	Reverse Recovery Time	—	51 54	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$ $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$, $T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⁽⁵⁾ $T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	86 102	—		
I_{RRM}	Reverse Recovery Current	—	2.9	—	A	$T_J = 25^\circ\text{C}$




Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 11. Drain-to-Source Breakdown Voltage

Fig 10. Maximum Safe Operating Area

Fig 12. Typical C_{oss} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current

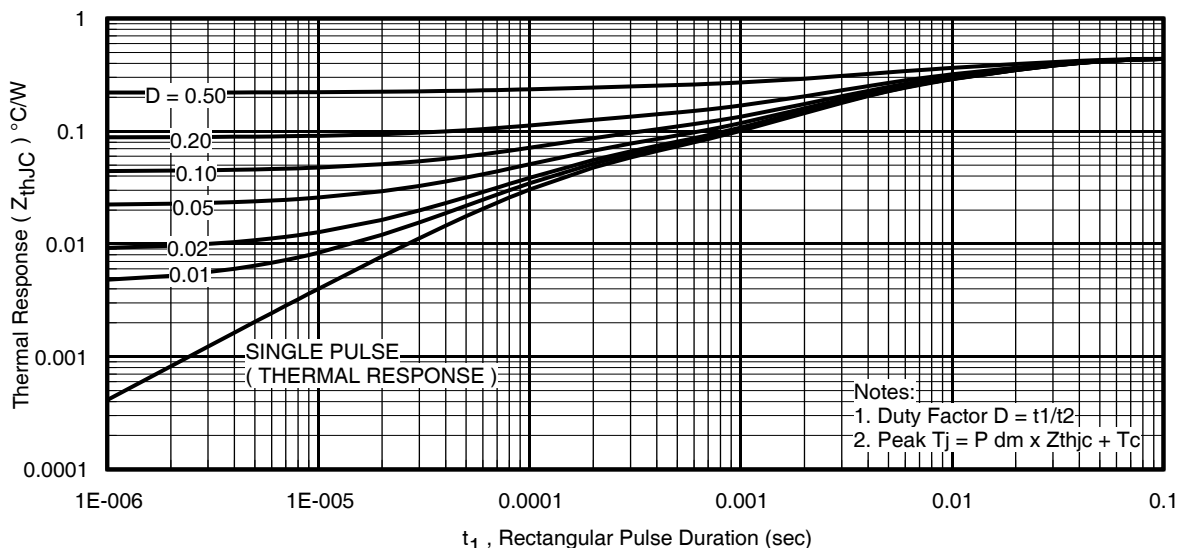


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

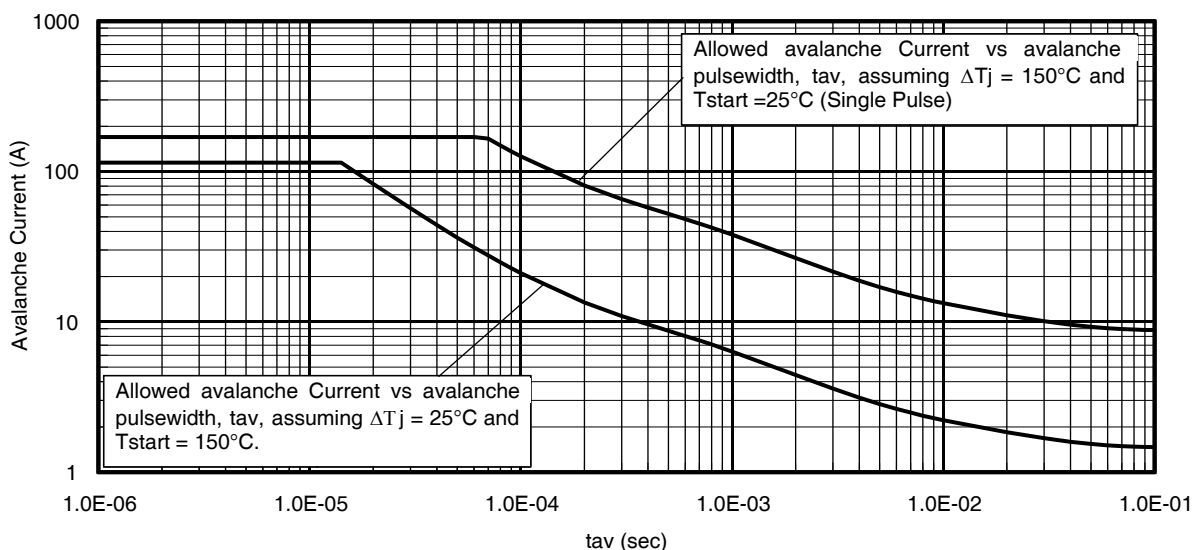


Fig 15. Avalanche Current vs. Pulse Width

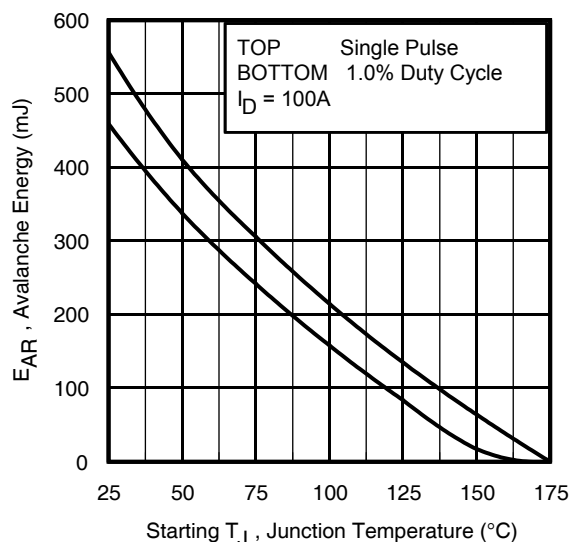
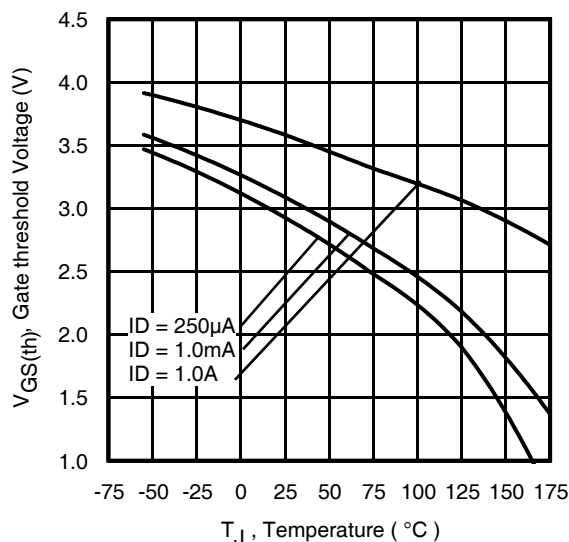
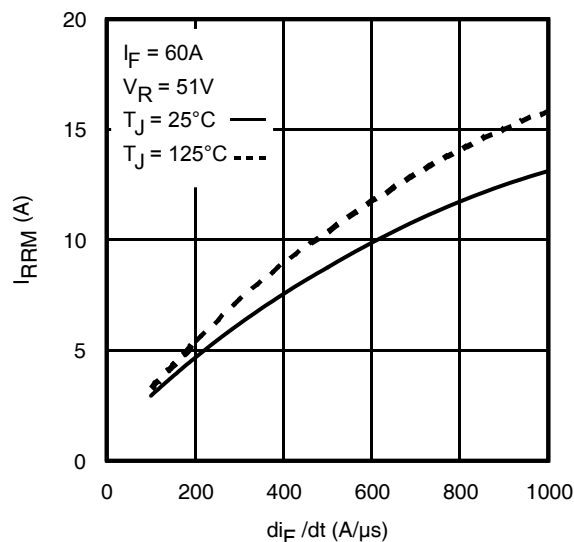
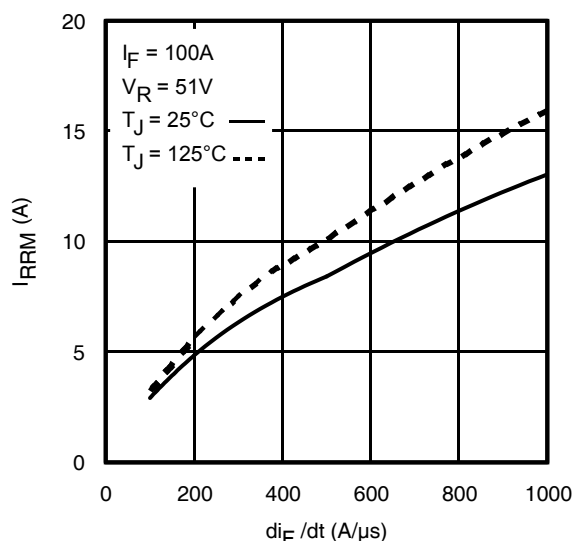
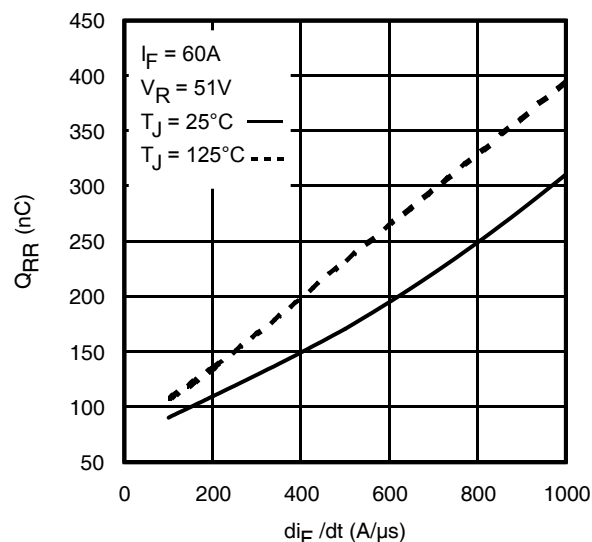
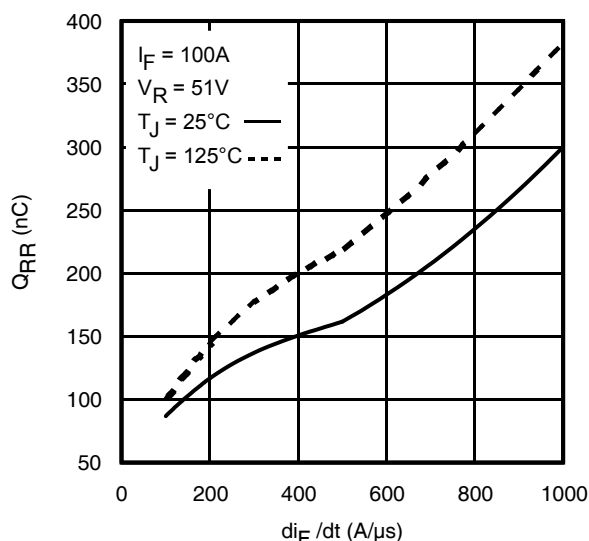


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)
 $P_D(ave) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Recovery Current vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt

Fig 21. Typical Stored Charge vs. di_F/dt

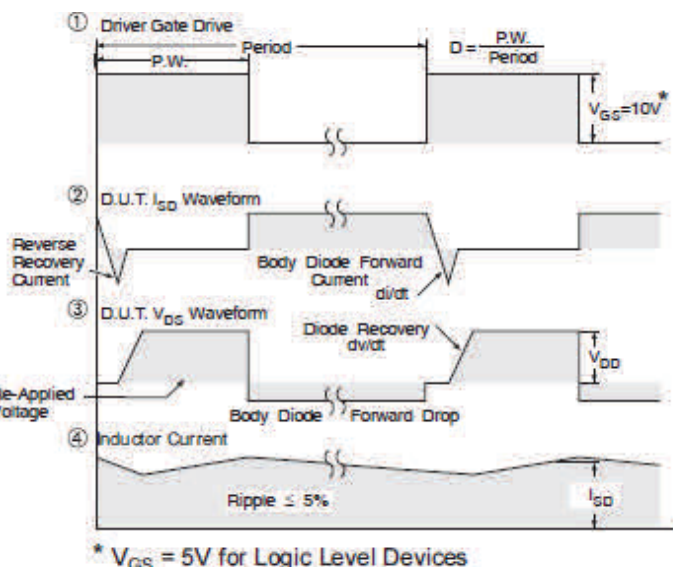
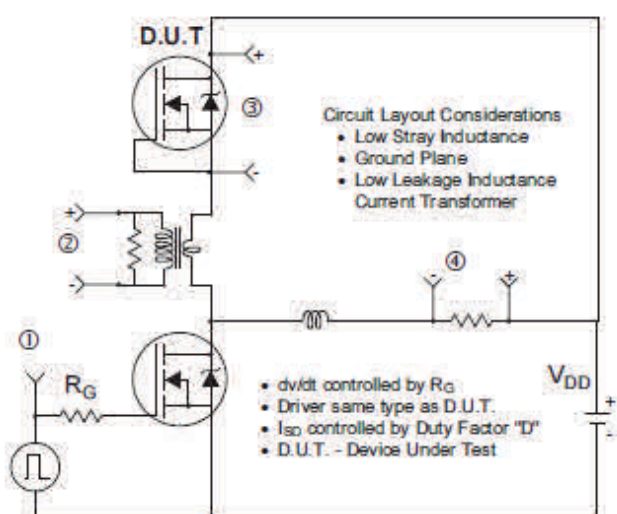


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

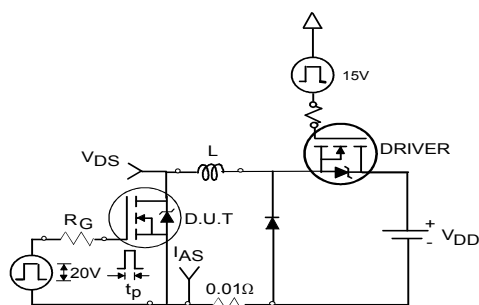


Fig 23a. Unclamped Inductive Test Circuit

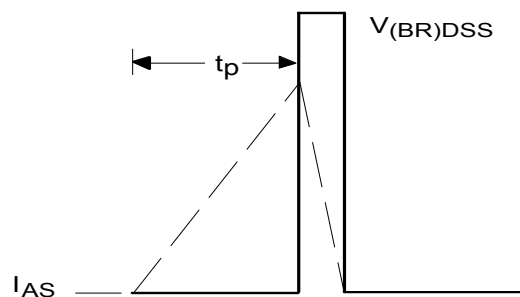


Fig 23b. Unclamped Inductive Waveforms

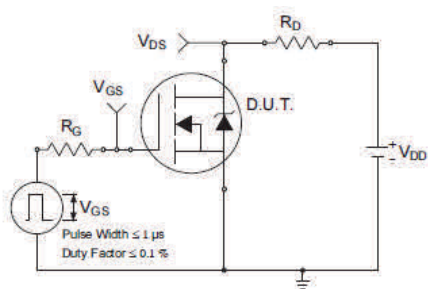


Fig 24a. Switching Time Test Circuit

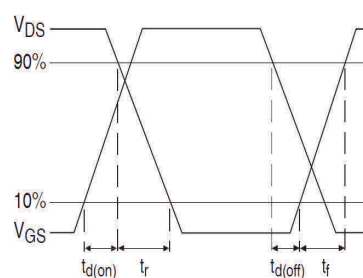


Fig 24b. Switching Time Waveforms

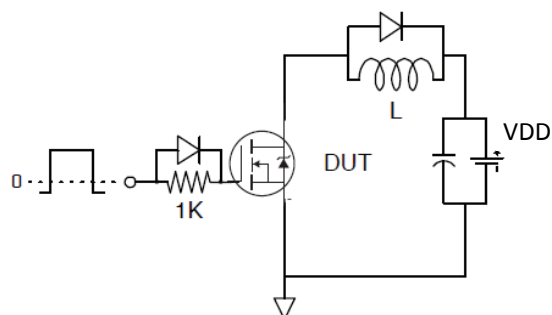


Fig 25a. Gate Charge Test Circuit

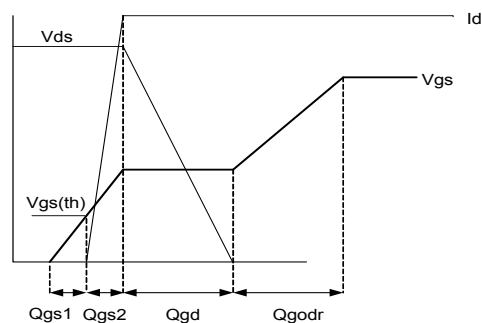
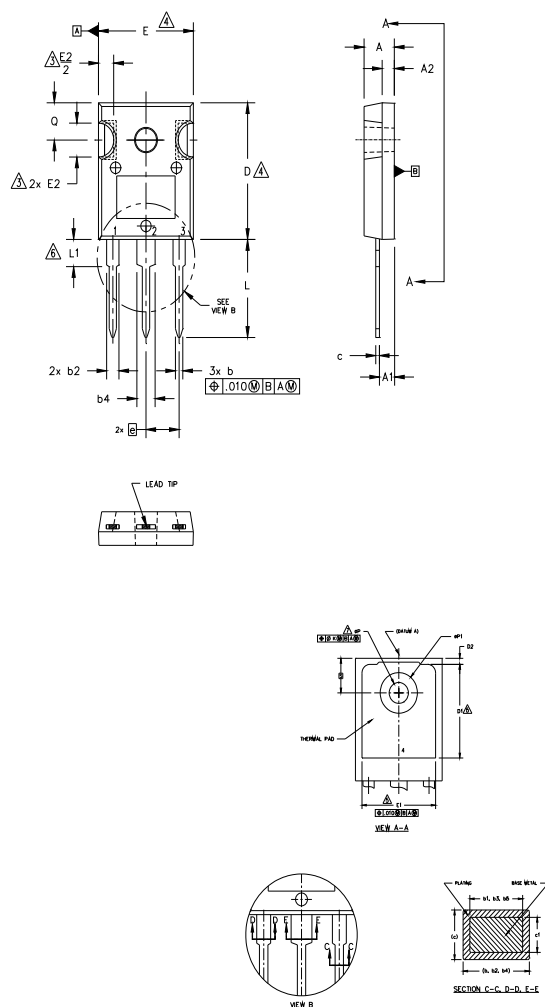


Fig 25b. Gate Charge Waveform

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

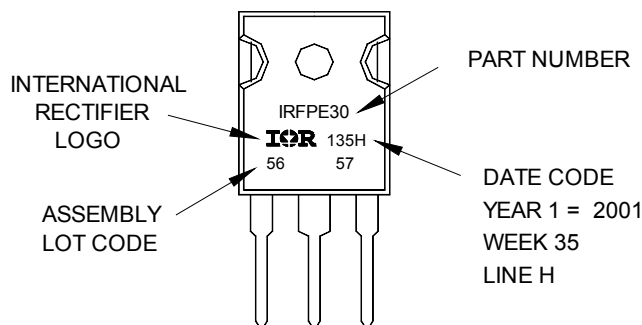
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-247	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
 To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>