

NLX1G99

Configurable Multifunction Gate

The NLX1G99 MiniGate™ is an advanced high-speed CMOS multifunction gate with a 3-state output. With the output enable input ($\overline{OE}$) at High, the output is disabled and is kept at high impedance. With the output enable input ($\overline{OE}$) at Low, the device can be configured for logic functions such as MUX, AND, OR, NAND, NOR, XOR, XNOR, INVERT and BUFFER, depending on the combination of the 4-bit input. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G99 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

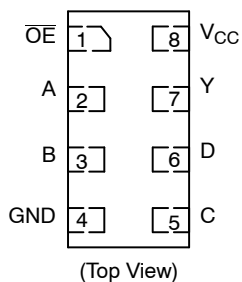
Features

- High Speed: $t_{PD} = 6.7$ ns (Max) @ $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

PIN ASSIGNMENT

1	$\overline{OE}$
2	A
3	B
4	GND
5	C
6	D
7	Y
8	V_{CC}

PIN ASSIGNMENTS



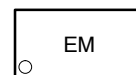
ON Semiconductor®

<http://onsemi.com>

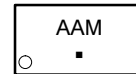
MARKING DIAGRAMS



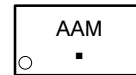
ULLGA8
1.45 x 1.0
CASE 613AA



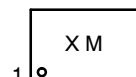
ULLGA8
1.6 x 1.0
CASE 613AB



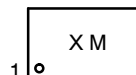
ULLGA8
1.95 x 1.0
CASE 613AC



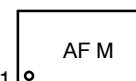
UDFN8
1.45 x 1.0
CASE 517BZ



UDFN8
1.6 x 1.0
CASE 517BY



UDFN8
1.95 x 1.0
CASE 517CA



AA or E = Specific Device Code
M = Date Code
▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NLX1G99

FUNCTION DIAGRAM

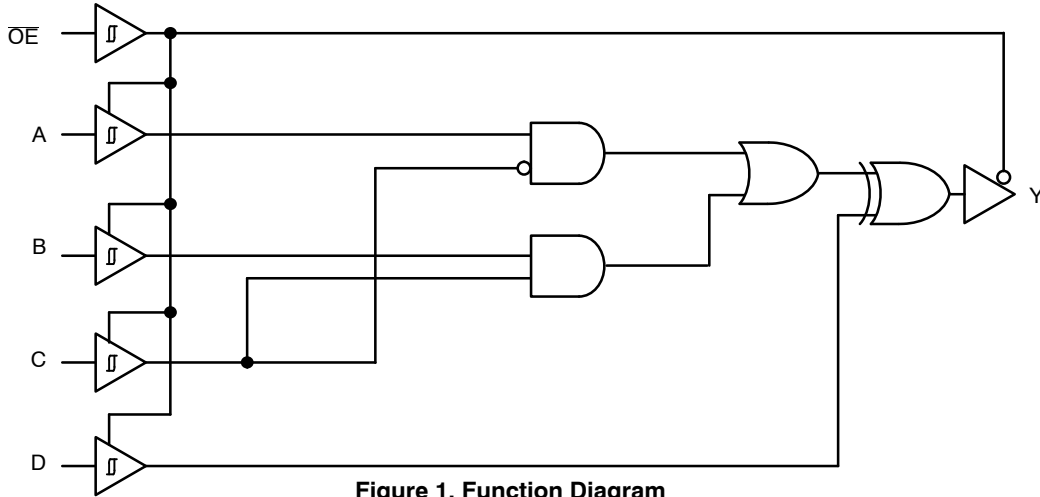


Figure 1. Function Diagram

FUNCTION TABLE*

INPUT					OUTPUT
OE	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	H or L	H or L	H or L	H or L	Z

*To select a logic function, please refer to "Logic Configurations" section.

FUNCTION SELECTION	LOGIC CONFIGURATION PAGE
3-State Buffers	3
3-State Inverters	3
3-State MUXes	3
3-State AND / OR / NOR	4
3-State NAND / OR	5
3-State XOR/XNOR	6

NLX1G99

LOGIC CONFIGURATIONS

3-State Buffer Functions Available

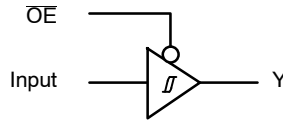


Figure 2.

Function	OE	A	B	C	D
3-State Buffer	L	Input H or L L H H H or L L	H or L Input H L H or L L L	L H Input Input L H H or L	L L L H Input Input Input

3-State Inverter Functions Available

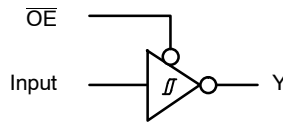


Figure 3.

Function	OE	A	B	C	D
3-State Buffer	L	Input X L H H H or L H	H or L Input H L H or L H H	L H Input Input L H H or L	H H H L Input Input Input

3-State MUX Functions Available

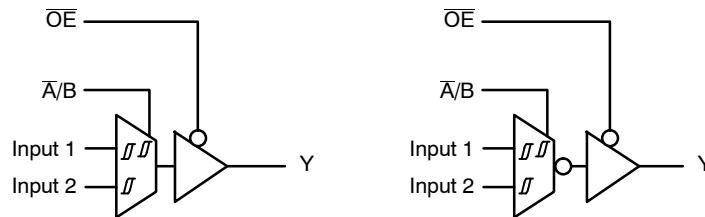


Figure 4.

Function	OE	A	B	C	D
3-State 2-to-1 3-State 2-to-1	L	Input 1 Input 2	Input 2 Input 1	Input 1 or Input 2 Input 2 or Input 1	L L
3-State 2-to-1, Inverted Out 3-State 2-to-1, Inverted Out		Input 1 Input 2	Input 2 Input 1	Input 1 or Input 2 Input 2 or Input 1	H H

NLX1G99

3-State AND/NOR/OR Function Available

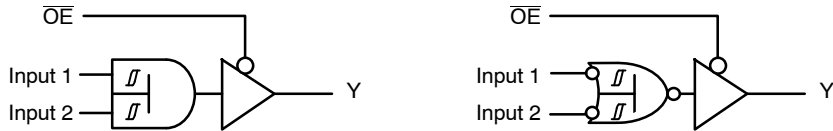


Figure 5.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	L	Input 1	Input 2	L
2	3-State AND	3-State NOR	L	L	Input 2	Input 1	L

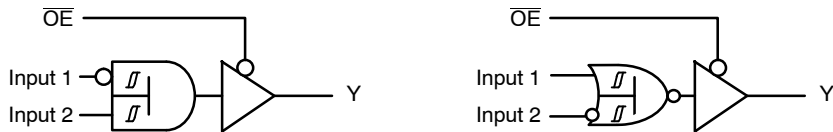


Figure 6.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 2	L	Input 1	L
2	3-State AND	3-State NOR	L	H	Input 1	Input 2	H

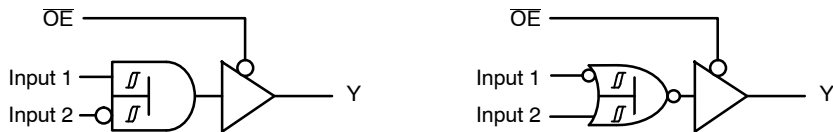


Figure 7.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 1	L	Input 2	L
2	3-State AND	3-State NOR	L	H	Input 2	Input 1	H

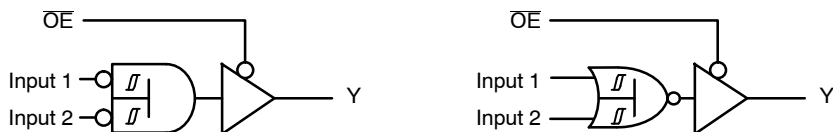


Figure 8.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR	L	Input 2	H	Input 1	L

NLX1G99

3-State NAND/OR Function Available

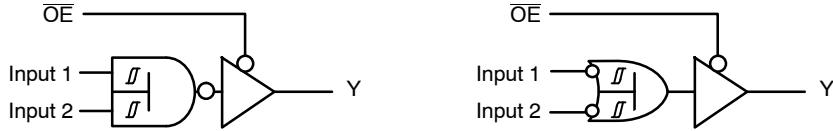


Figure 9.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	L	Input 1	Input 2	H
2	3-State NAND	3-State OR		L	Input 2	Input 1	H

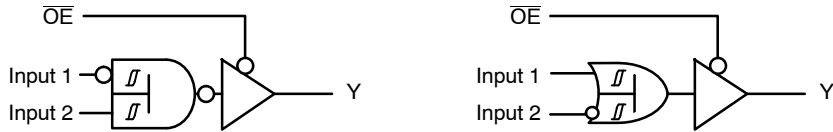


Figure 10.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 2	L	Input 1	H
2	3-State NAND	3-State OR		H	Input 1	Input 2	L

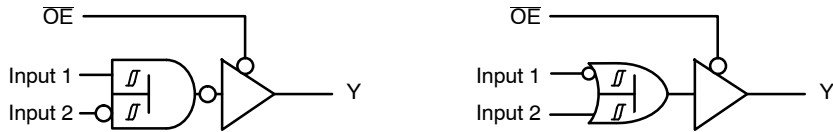


Figure 11.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 1	L	Input 2	H
2	3-State NAND	3-State OR		H	Input 2	Input 1	L

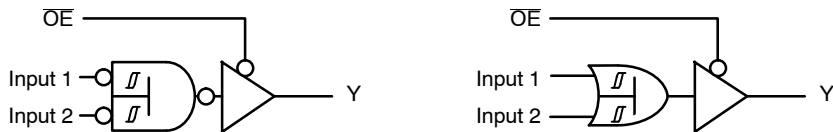


Figure 12.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR		Input 2	H	Input 1	L

NLX1G99

3-State XOR/XNOR Function Available

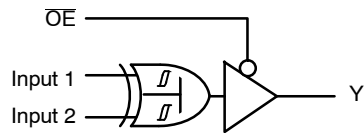


Figure 13.

Function	OE	A	B	C	D
3-State XOR	L	Input 1 Input 2 H or L H or L L L	H or L H or L Input 1 Input 2 H H	L L H H Input 1 Input 2	Input 2 Input 1 Input 2 Input 1 Input 2 Input 1

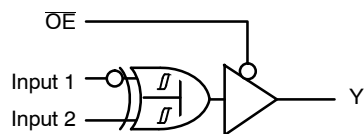


Figure 14.

Function	OE	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

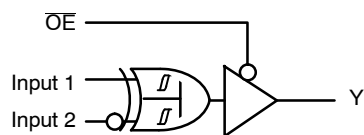


Figure 15.

Function	OE	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

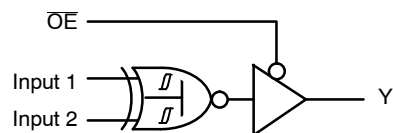


Figure 16.

Function	OE	A	B	C	D
3-State XNOR 3-State XNOR	L	H H	L L	Input 1 Input 2	Input 2 Input 1

NLX1G99

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage Active Mode (High or Low State) Tristate Mode (Output at Hi-Z) Power Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC}	DC Supply Current Per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	Digital Input Voltage	0	5.5	V
V_{OUT}	Output Voltage Active Mode (High or Low State) Tristate Mode (Output at Hi-Z) Power Down Mode ($V_{CC} = 0$ V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature	-55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 2.5$ V $\pm$ 0.2 V $V_{CC} = 3.3$ V $\pm$ 0.3 V $V_{CC} = 5.0$ V $\pm$ 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NLX1G99

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A ≤ +85°C		T _A = -55°C to +125°C		Unit
				Min	Max	Min	Max	Min	Max	
V _{T+}	Positive Threshold Voltage		1.65	0.79	1.16		1.16		1.16	V
			1.8	0.87	1.28		1.28		1.28	
			2.3	1.11	1.56		1.56		1.56	
			3.0	1.5	1.87		1.87		1.87	
			4.5	2.16	2.74		2.74		2.74	
			5.5	2.61	3.33		3.33		3.33	
V _{T-}	Negative Threshold Voltage		1.65	0.35	0.62	0.35		0.35		V
			1.8	0.38	0.68	0.38		0.38		
			2.3	0.58	0.87	0.58		0.58		
			3.0	0.84	1.19	0.84		0.84		
			4.5	1.41	1.9	1.41		1.41		
			5.5	1.78	2.29	1.78		1.78		
V _H	Hysteresis Voltage		1.65	0.30	0.62	0.30	0.62	0.30	0.62	V
			1.8	0.33	0.68	0.33	0.68	0.33	0.68	
			2.3	0.40	0.8	0.40	0.8	0.40	0.8	
			3.0	0.53	0.87	0.53	0.87	0.53	0.87	
			4.5	0.71	1.04	0.71	1.04	0.71	1.04	
			5.5	0.8	1.2	0.8	1.2	0.8	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OH} = -50 μA I _{OH} = -100 μA	1.65-5.5	V _{CC} -0.1		V _{CC} -0.1		V _{CC} -0.1		V
			1.65-5.5	V _{CC} -0.1		V _{CC} -0.1		V _{CC} -0.1		V
		V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65	1.2		1.2		1.2		V
			2.3	1.9		1.9		1.9		V
			2.7	2.2		2.2		2.2		V
			3.0	2.4		2.4		2.4		V
			3.0	2.3		2.3		2.3		V
			4.5	3.8		3.8		3.8		V
										V
										V
										V
										V
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OL} = 50 μA I _{OL} = 100 μA	1.65-5.5		0.1		0.1		0.1	V
			1.65-5.5		0.1		0.1		0.1	
		V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65		0.45		0.45		0.45	
			2.3		0.3		0.3		0.3	
			2.7		0.4		0.4		0.4	
			3.0		0.4		0.4		0.4	
			3.0		0.55		0.55		0.55	
			4.5		0.55		0.55		0.55	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 - 5.5		± 0.1		± 1.0		± 1.0	μA
I _{off}	Power off Leakage Current	V _{IN} or V _O = 5.5 V	0		± 1.0		± 10		± 10	μA
I _{OZ}	Tri-state Output Leakage Current	V _O = V _{CC} or GND	1.65-5.5		± 1.0		± 10		± 10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _O = 0	1.65-5.5		1.0		10		10	μA
ΔI _{CC}	Increase in I _{CC} Per Input	One input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND	2.3 - 5.5		10		100		100	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

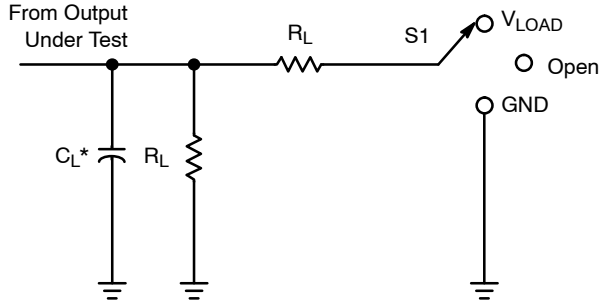
NLX1G99

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	$T_A = 25^\circ\text{C}$			$T_A \leq +85^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.3 2.4 1.7 1.3	12.8 7.1 5.2 4.0	25.1 10.2 6.7 4.5	4.3 2.4 1.7 1.3	25.1 10.2 6.9 4.9	4.3 2.4 1.7 1.3	25.1 10.2 7.0 5.0	ns
t_{EN}	Output Enable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	3.4 2.1 1.3 1.0		24.7 11 7.5 5.7	3.4 2.1 1.3 1.0	24.7 12 8.0 6.2	3.4 2.1 1.3 1.0	24.7 12.2 8.3 6.5	ns
t_{DIS}	Output Disable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.0 2.7 3.5 2.0		15.5 7.5 7.0 5.5	4.0 2.7 3.5 2.0	15.5 7.5 7.0 5.5	4.0 2.7 3.5 2.0	15.5 7.5 7.0 5.5	ns
t_{PLH} , t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.3 2.5 2.3 1.6	13.6 7.8 5.6 4.4	25.7 10.7 7.6 5.2	4.3 2.5 2.3 1.6	25.7 10.7 7.6 5.2	4.3 2.5 2.3 1.6	25.7 10.7 7.6 5.2	ns
t_{EN}	Output Enable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.2 2.4 2.0 1.7		25.2 11.3 8.0 6.0	4.2 2.4 2.0 1.7	25.2 12.2 8.5 6.5	4.2 2.4 2.0 1.7	25.2 13 8.7 6.7	ns
t_{DIS}	Output Disable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	3.7 2.0 2.1 1.0		15 6.5 5.6 4.5	3.7 2.0 2.1 1.0	15 6.7 5.8 4.7	3.7 2.0 2.1 1.0	15 6.9 5.9 4.9	ns
C_{IN}	Input Capacitance	3.3			3.5						pF
C_O	Output Capacitance	3.3			6.0						pF
C_{PD}	Power Dissipation Capacitance (Note 6)	3.3	$f = 10$ MHz		22						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

TEST CIRCUIT AND VOLTAGE WAVEFORMS



* C_L includes probes and jig capacitance.

Figure 17. Load Circuit

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V

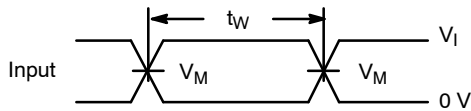


Figure 18. Voltage Waveforms Pulse Duration

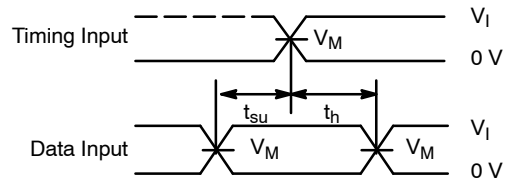


Figure 19. Voltage Waveforms Setup and Hold Times

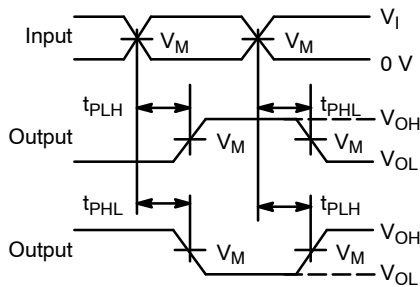


Figure 20. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

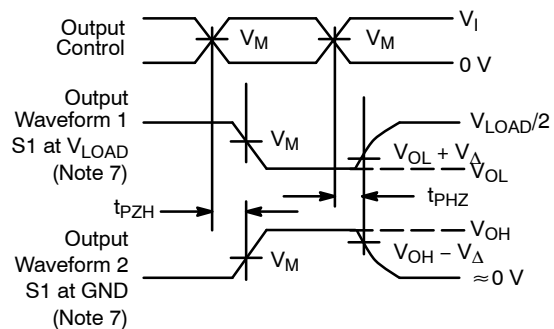
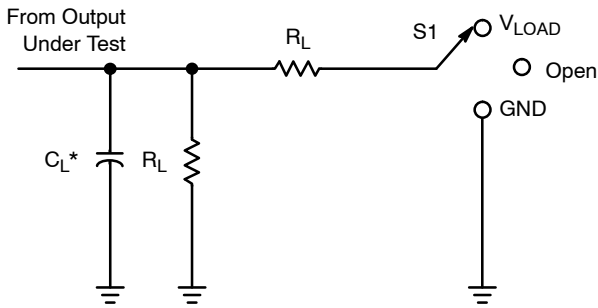


Figure 21. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- All parameters are waveforms are not applicable to all devices.

NLX1G99



*C_L includes probes and jig capacitance.

Figure 22. Load Circuit

Test	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

V _{CC}	Inputs		V _M	V _{LOAD}	C _L	R _L	V _Δ
	V _I	t _r /t _f					
1.8 V ± 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 x V _{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 x V _{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.5 V ± 0.5 V	V _{CC}	≤ 2.5 ns	V _{CC} /2	2 x V _{CC}	50 pF	500 Ω	0.3 V

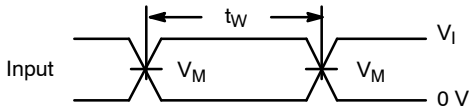


Figure 23. Voltage Waveforms Pulse Duration

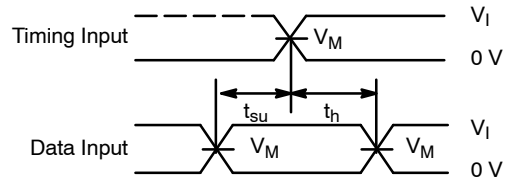


Figure 24. Voltage Waveforms Setup and Hold Times

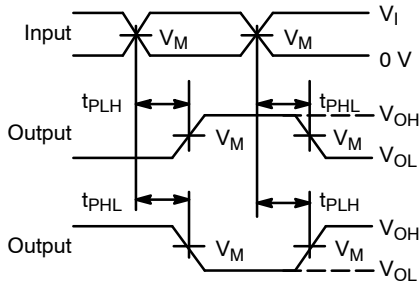


Figure 25. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

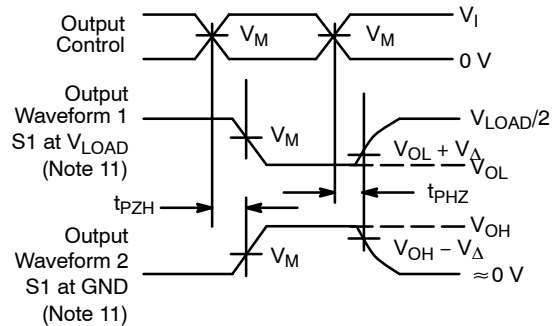


Figure 26. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

11. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
12. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
13. The outputs are measured one at a time, with one transition per measurement.
14. All parameters are waveforms are not applicable to all devices.

NLX1G99

ORDERING INFORMATION

Device	Package	Shipping [†]
NLX1G99AMX1TCG	ULLGA8 – 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G99BMX1TCG	ULLGA8 – 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G99CMX1TCG	ULLGA8 – 0.35P (Pb-Free)	3000 / Tape & Reel
NLX1G99DMUTCG	UDFN8, 1.95 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G99EMUTCG In Development	UDFN8, 1.6 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G99FMUTCG In Development	UDFN8, 1.45 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

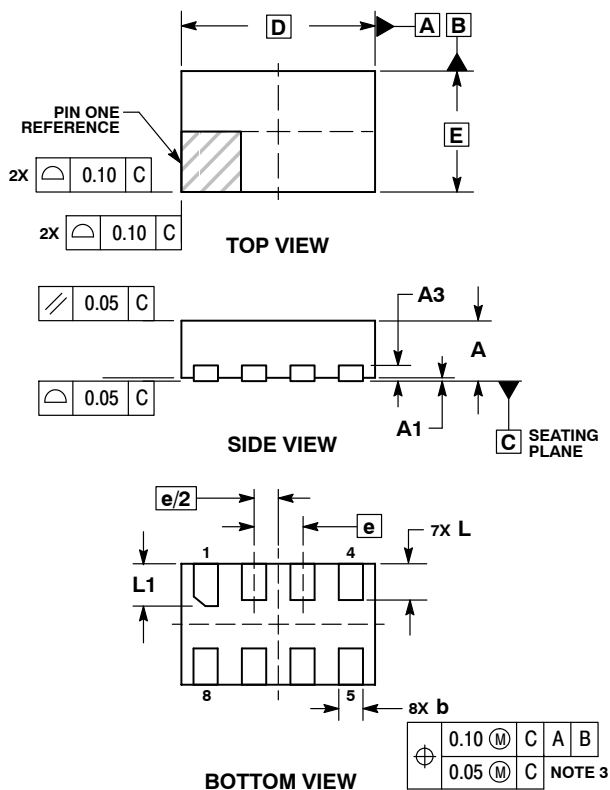
NLX1G99

PACKAGE DIMENSIONS

UDFN8 1.6x1.0, 0.4P

CASE 517BY

ISSUE O

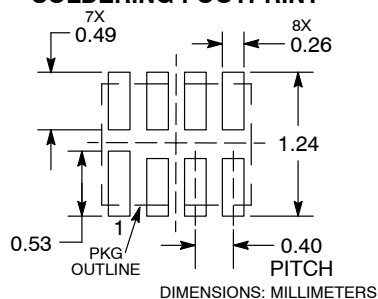


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.00	BSC
e	0.40	BSC
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

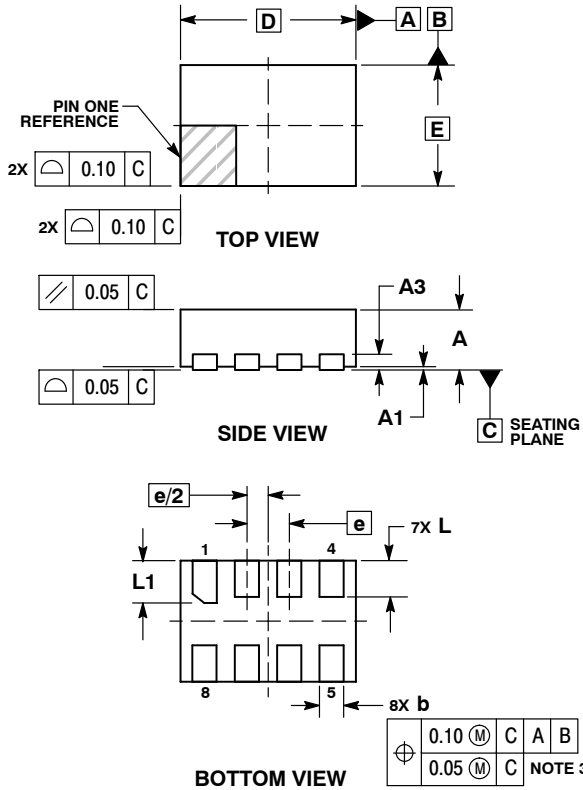


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G99

PACKAGE DIMENSIONS

UDFN8 1.45x1.0, 0.35P
CASE 517BZ
ISSUE O

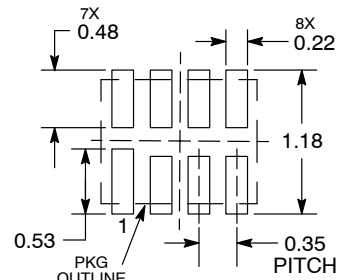


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.45	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



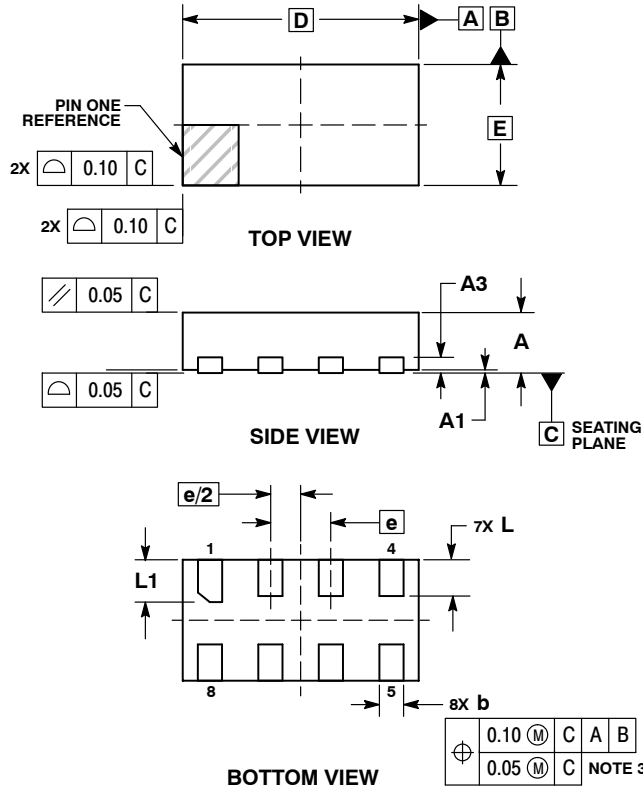
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G99

PACKAGE DIMENSIONS

UDFN8 1.95x1.0, 0.5P
CASE 517CA
ISSUE O

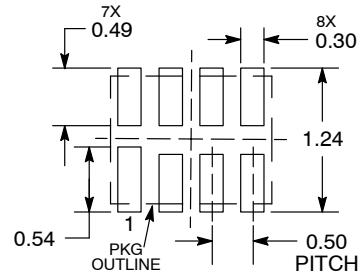


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.95	BSC
E	1.00	BSC
e	0.50	BSC
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



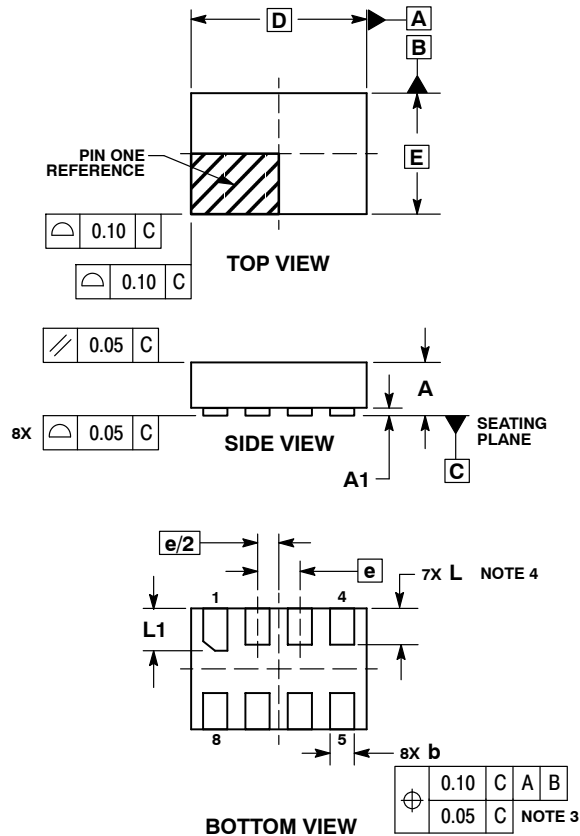
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G99

PACKAGE DIMENSIONS

ULLGA8 1.45x1.0, 0.35P
CASE 613AA
ISSUE A

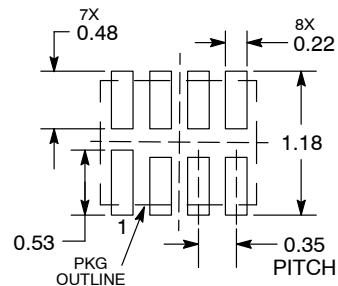


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



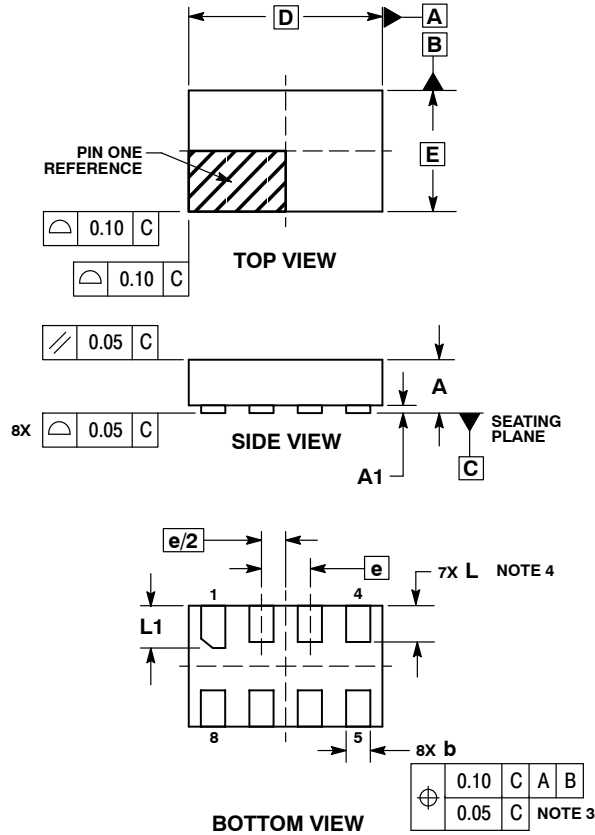
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G99

PACKAGE DIMENSIONS

ULLGA8 1.6x1.0, 0.4P
CASE 613AB
ISSUE A

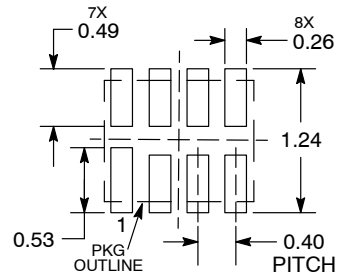


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60	BSC
E	1.00	BSC
e	0.40	BSC
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



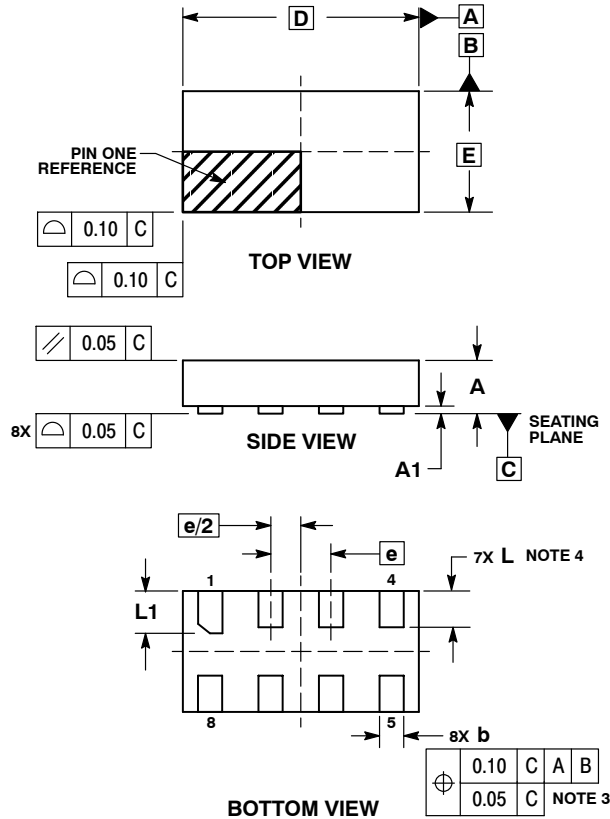
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G99

PACKAGE DIMENSIONS

ULLGA8 1.95x1.0, 0.5P
CASE 613AC
ISSUE A

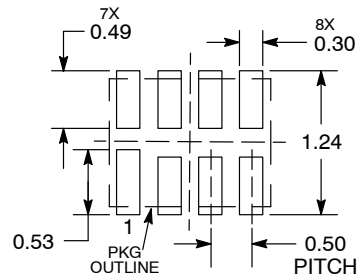


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

NLX1G99/D