Product Standards

Part No.	AN30259A
Package Code No.	XBGA012-W-1316AEL

Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H. Shidooka	M. Hiramatsu	Y.Higuchi	A.Kitagawa

AN30259A

3-ch. LED driver for illumination

■ Overview

AN30259A has 3-ch. LED Driver. It is a suitable product to use for RGB Illumination. By synchronous clock function, combined operation is possible.

■ Features

- I^2C Interface (Slave address is switchable.)
- Build-in 3-ch. LED Driver Circuit (Max Current Selectable [63.75 mA / 31.875 mA / 25.50 mA / 12.75 mA])
- 2.4 MHz OSC

■ Application

- LED driver IC

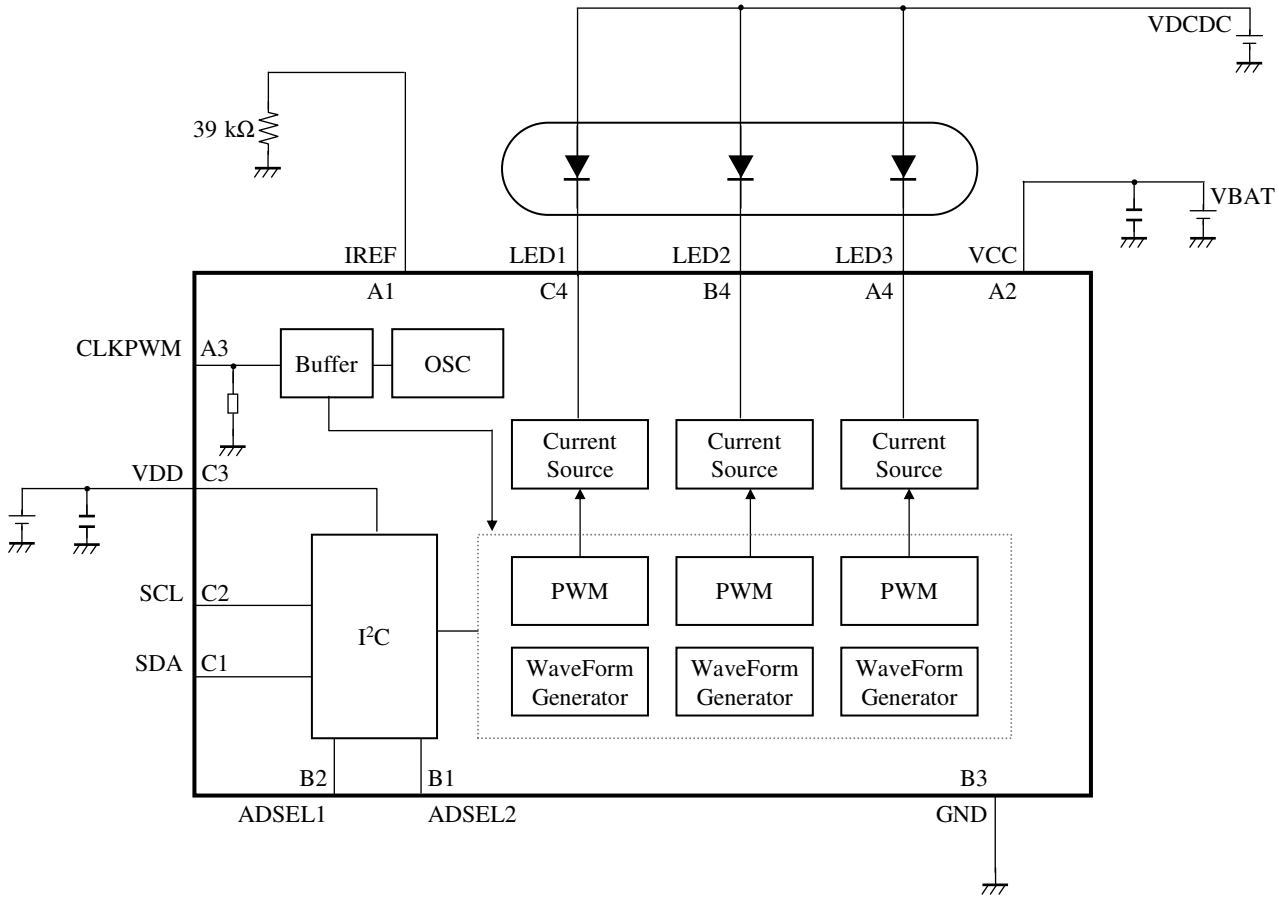
■ Package

- 12 pin Wafer level chip size package (WLCSP)
  Size : 1.56 mm × 1.26 mm (0.4 mm pitch)

■ Type

- Bi-CMOS IC

■ Application circuit example (Block diagram)

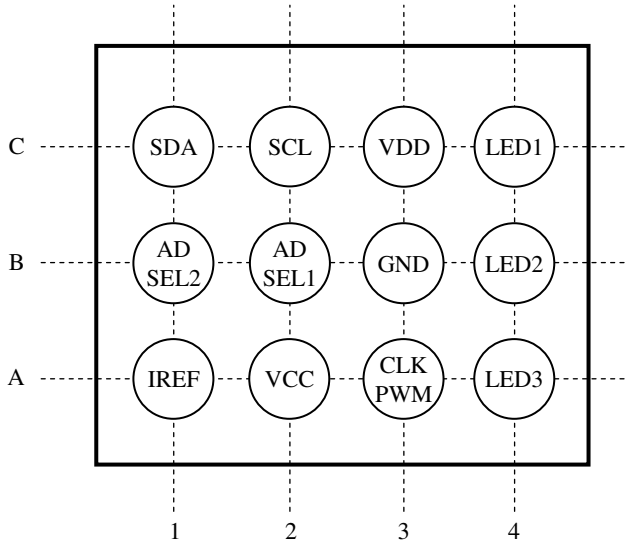


Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

• This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

■ Pin Description

Pin No.	Pin Name	Type	Description
A1	IREF	Output	Resistor connection pin for setting constant current value
A2	VCC	Power Supply	Power supply pin for LED Circuit
A3	CLKPWM	Input/Output	Reference clock I/O / PWM input pin
A4	LED3	Output	LED3 output pin
B1	ADSEL2	Input	I^2C Interface slave address switch pin 2
B2	ADSEL1	Input	I^2C Interface slave address switch pin 1
B3	GND	Ground	Ground pin
B4	LED2	Output	LED2 output pin
C1	SDA	Input/Output	I^2C interface data I/O pin
C2	SCL	Input	I^2C interface clock input pin
C3	VDD	Power Supply	Power supply pin for interface
C4	LED1	Output	LED1 output pin



Bottom view

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Power supply voltage	V_{CC}	7.0	V	*1
		V_{DD}	4.6	V	*1
2	Power supply current	I_{CC}	—	A	—
3	Power dissipation	P_D	46.8	mW	*2
4	Operating ambience temperature	T_{opr}	–30 to + 85	°C	*3
5	Storage temperature	T_{stg}	–55 to + 125	°C	*3

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Voltage Supply Range

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage range	V_{CC}	3.1 to 6.0	V	*
	V_{DD}	1.7 to 3.2	V	*

Note) * : The values in the chart above shows the results when using the product under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Please use under the condition where V_{DD} voltage does not exceed V_{CC} voltage.

■ Allowable Voltage and Current Range

Notes) • Allowable voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
• Voltage values, unless otherwise specified, are with respect to GND.
• Do not apply external currents or voltages to any pin not specifically mentioned.

Pin No.	Pin name	Rating	Unit	Notes
A1	IREF	0.0 to (VCC + 0.3)	V	*1, *3
A2	VCC	0.0 to + 7.0	V	—
A3	CLKPWM	–0.2 to (VDD + 0.3)	V	*2, *3
A4	LED3	0.0 to + 7.0	V	—
B1	ADSEL2	–0.2 to (VDD + 0.3)	V	*2
B2	ADSEL1	–0.2 to (VDD + 0.3)	V	*2
B3	GND	GND	V	—
B4	LED2	0.0 to + 7.0	V	—
C1	SDA	–0.2 to (VDD + 0.3)	V	*2, *3
C2	SCL	–0.2 to (VDD + 0.3)	V	*2
C3	VDD	0.0 to + 4.6	V	—
C4	LED1	0.0 to + 7.0	V	—

Notes) *1 : (VCC + 0.3) V must not be exceeded 7.0 V.
*2 : (VDD + 0.3) V must not be exceeded 4.6 V.
*3 : Rating when used for input. External voltage or current must not be applied when used for output.

■ Electrical Characteristic at V_{CC} = 3.6 V, V_{DD} = 1.8 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Current consumption									
1	Current consumption 1 OFF mode	I_{CC1}	1	V_{DD} = 0 V	—	0	2	µA	—
2	Current consumption 2 OFF mode	I_{CC2}	1	V_{DD} = 1.8 V	—	1	5	µA	—
3	Current consumption 3 LED lighting mode	I_{CC3}	1	$I_{LED1\ to\ 3}$ = 25.50 mA setting All LED = ON	—	0.6	1.0	mA	—

■ Electrical Characteristic (continued) at V_{CC} = 3.6 V, V_{DD} = 1.8 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
LED Driver									
4	Off time leak current	I_{LEAK}	1	Off setting $V_{LED1\ to\ 3}$ = 6.0 V	—	—	1.0	µA	—
5	Minimum setting current value 1	I_{MIN1}	1	IMAX[1:0] = 01, $V_{LED1\ to\ 3}$ = 1.0 V	0.05	0.10	0.15	mA	—
6	Minimum setting current value 2	I_{MIN2}	1	IMAX[1:0] = 01, $V_{LED1\ to\ 3}$ = 1.0 V	0.736	0.80	0.864	mA	—
7	Maximum setting current value	I_{MAX}	1	IMAX[1:0] = 01, $V_{LED1\ to\ 3}$ = 1.0 V	23.46	25.50	27.54	mA	—
8	Current step	I_{STEP}	1	IMAX[1:0] = 01, $V_{LED1\ to\ 3}$ = 1.0 V	0.00	0.10	0.18	mA	—
9	Minimum voltage for retainable constant current value	V_{SAT}	1	IMAX[1:0] = 01, Terminal minimum voltage of LED1 to 3 becoming 85% of the LED current value in 1 V.	—	0.2	0.4	V	—
10	Error between channels	I_{MATCH}	1	12.80 mA setting, $V_{LED1\ to\ 3}$ = 1.0 V	–5	—	5	%	—
Internal oscillator									
11	Oscillation frequency	f_{OSC}	1	—	1.92	2.40	2.88	MHz	—

■ Electrical Characteristic (continued) at V_{CC} = 3.6 V, V_{DD} = 1.8 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
SCL, SDA									
12	High-level input voltage range	V_{IH1}	1	Voltage which recognized that SDA and SCL are High-level	V_{DD} × 0.7	—	V_{DDmax} + 0.5	V	*1
13	Low-level input voltage range	V_{IL1}	1	Voltage which recognized that SDA and SCL are Low-level	–0.5	—	V_{DD} × 0.3	V	*1
14	High-level input current	I_{IH1}	1	V_{SDA}, V_{SCL} = 1.8 V	—	0	1	µA	—
15	Low-level input current	I_{IL1}	1	V_{SDA}, V_{SCL} = 0 V	—	0	1	µA	—
16	Low-level output voltage (SDA)	V_{OL1H}	1	I_{SDA} = 3 mA, V_{DD} > 2 V	0	—	0.4	V	—
17	Low-level output voltage (SDA)	V_{OL1L}	1	I_{SDA} = 3 mA, V_{DD} < 2 V	0	—	0.2 × V_{DD}	V	—
18	SCL clock frequency	f_{SCL}	1	—	0	—	400	kHz	—
CLKPWM									
19	High-level input voltage range	V_{IH2}	1	—	V_{DD} × 0.7	—	V_{DD} + 0.2	V	—
20	Low-level input voltage range	V_{IL2}	1	—	–0.2	—	V_{DD} × 0.3	V	—
21	Pin pull down resistance value	R_{PD2}	1	—	0.5	1.0	2.0	MΩ	—
22	High-level output voltage	V_{OH2}	1	I_{CLKPWM} = –2 mA	V_{DD} × 0.8	—	V_{DD} + 0.2	V	—
23	Low-level output voltage	V_{OL2}	1	I_{CLKPWM} = 2 mA	–0.2	—	V_{DD} × 0.2	V	—
ADSEL1, ADSEL2									
24	High-level input voltage range	V_{IH3}	1	—	V_{DD} × 0.7	—	V_{DD} + 0.2	V	—
25	Low-level input voltage range	V_{IL3}	1	—	–0.2	—	V_{DD} × 0.3	V	—
26	High-level input current	I_{IH3}	1	$V_{ADSEL1, 2}$ = 1.8 V	—	0	1	µA	—
27	Low-level input current	I_{IL3}	1	$V_{ADSEL1, 2}$ = 0 V	—	0	1	µA	—

Note)*1 : The input threshold voltage of I²C bus (Vth) is linked to V_{DD} (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not V_{DD}, the threshold voltage (Vth) is fixed to ((V_{DD} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{DD}).

■ Electrical Characteristic (Reference values for design) at V_{CC} = 3.6 V, V_{DD} = 1.8 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuit	Conditions	Reference Values			Unit	Note
					Min	Typ	Max		
CLKPWM									
28	External PWM operation mode Data-enabled high pulse width	W_{PWM}	1	—	2	—	—	µs	—

■ Electrical Characteristic (Reference values for design) (continued) at V_{CC} = 3.6 V, V_{DD} = 1.8 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

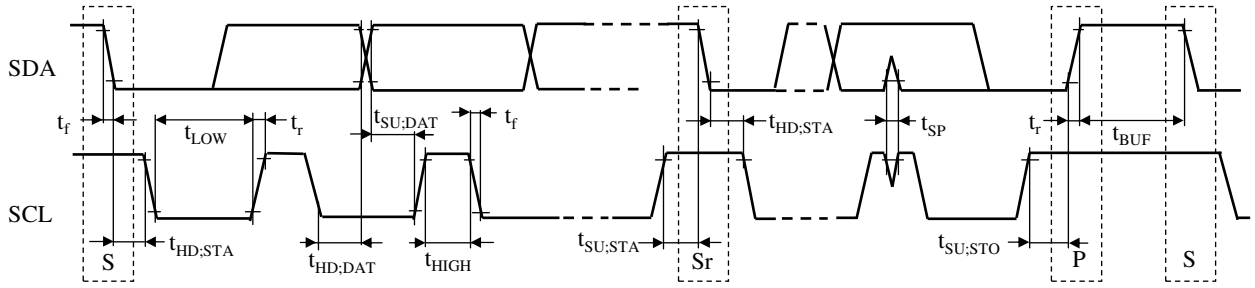
B No.	Parameter	Symbol	Test circuit	Conditions	Reference Values			Unit	Note
					Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)									
29	Input voltage hysteresis (1)	V_{hys1}	1	SCL, SDA hysteresis voltage VDD > 2 V	0.05 × V_{DD}	—	—	V	—
30	Input voltage hysteresis (2)	V_{hys2}	1	SCL, SDA hysteresis voltage VDD < 2 V	0.1 × V_{DD}	—	—	V	—
31	Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	1	Bus capacitance : 10 pF to 400pF $I_P \leq 6$ mA (V_{OLmax} = 0.6 V) I_P : Max. sink current	20 + 0.1×C_b	—	250	ns	—
32	Spike pulse width kept down by input filter	t_{sp}	1	—	0	—	50	ns	—
33	I/O pin capacitance	C_i	1	—	—	—	10	pF	—

■ Electrical Characteristic (Reference values for design) (continued) at VCC = 3.6 V, VDD = 1.8 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test Circuit	Conditions	Reference Values			Unit	Note
					Min	Typ	Max		
I²C bus (Bus line specifications)									
34	Hold duration (recursive)	$t_{HD:STA}$	1	After $t_{HD:STA,.}$ the first clock pulse is generated.	0.6	—	—	µs	*2
35	SCL clock "L" duration	t_{LOW}	1	—	1.3	—	—	µs	*2
36	SCL clock "H" duration	t_{HIGH}	1	—	0.6	—	—	µs	*2
37	Recursive 「START」 condition setting time	$t_{SU:STA}$	1	—	0.6	—	—	µs	*2
38	Data hold time	$t_{HD:DAT}$	1	—	0	—	0.9	µs	*2
39	Data setup time	$t_{SU:DAT}$	1	—	100	—	—	ns	*2
40	SDA, SCL signal rise up time	t_r	1	—	$20 + 0.1 \times C_b$	—	300	ns	*2
41	SDA, SCL signal fall time	t_f	1	—	$20 + 0.1 \times C_b$	—	300	ns	*2
42	Setup time under 「STOP」 condition	$t_{SU:STO}$	1	—	0.6	—	—	µs	*2
43	Bus free time between under 「STOP」 condition and 「START」 condition	t_{BUF}	1	—	1.3	—	—	µs	*2
44	Capacitive load for each bus line	C_b	1	—	—	—	400	pF	*2
45	Noise margin of each connection device at Low-level	V_{nL}	1	—	$0.1 \times V_{DD}$	—	—	V	*2
46	Noise margin of each connection device at High-level	V_{nH}	1	—	$0.2 \times V_{DD}$	—	—	V	*2

Note) *2 : The timing of Fast-mode devices in I²C-bus is specified as follows.
All values referred to V_{IHmin} and V_{ILmax} level.



S : START condition
Sr : Repeat START condition
P : STOP condition

■ Test Circuit Diagram

Test Circuit 1