



AD9119-CBLTX-EBZ and AD9129-CBLTX-EBZ Cable Transmitter Evaluation Board Quick Start Guide

Getting Started with the AD9119/AD9129 Cable Transmitter Evaluation Board and Software

What's in the Box

- AD9119-CBLTX-EBZ or AD9129-CBLTX-EBZ Evaluation Board
- Mini-USB Cable
- Evaluation Board CD

Recommended Equipment List

- +5Vdc, +8 Vdc Power Supply
- Data Pattern Generator Series 2 (DPG2)
- Spectrum Analyzer Ex: Agilent PXA or Rohde Schwarz FSU

Introduction

The AD9119-CBLTX-EBZ and AD9129-CBLTX-EBZ are built from the same printed circuit board, with the only difference being which DAC device is loaded, the AD9119 or the AD9129. This Quick Start Guide will describe the set-up of the AD9129-CBLTX-EBZ, but the steps apply equally to setting up the AD9119-CBLTX-EBZ. The slight differences in performance between the two boards are documented in the data sheet, and are related to the 11-bit resolution of the AD9119. Thus, noise spectral density and some ACLR measurements are affected, and the AD9119 performance is lower than the corresponding performance of the AD9129. For ease of reading, only the AD9129-CBLTX-EBZ will be mentioned for the rest of the document.

The AD9129-CBLTX-EBZ connects to a DPG2 to allow for quick evaluation of the AD9129, a high-speed, RF Digital to Analog converter (RF DAC). The DPG2 automatically formats the data and sends it to the AD9129-CBLTX-EBZ, simplifying evaluation of the device. The Evaluation Board (EVB) runs from +5

volt and +8 volt supplies. Figure 2 is an image of the top side of the AD9129 EVB. The AD9129-CBLTX-EBZ evaluation board is intended for evaluation purposes only with no implied guarantee of performance or reliability. This evaluation board was solely developed to aid our customers in the development of a cable transmit solution and not intended to be directly leveraged into any final product.

AD9129 Evaluation Software

The AD9129 Evaluation Board software has an easy-to-use graphical user interface (GUI). It is included on the Evaluation Board CD, or can be downloaded from the DPG Web site at <http://www.analog.com/dpg>. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9129 SPI Controller application.

Hardware Setup

Connect +5V to P3, GND to P4, and +8V to P5. The evaluation board connects to the DPG2 unit through connectors P1 and P2. The spectrum analyzer should connect to the N-connector at J1. Because cable systems are typically 75 Ω systems, the output of the board is also 75 Ω. For best results using a 50 Ω spectrum analyzer, a transformer should be used to transform the output impedance from 75 Ω to 50 Ω. The PC should be connected to the EVB using the mini-USB connector XP2 after installation of the Evaluation Board software.

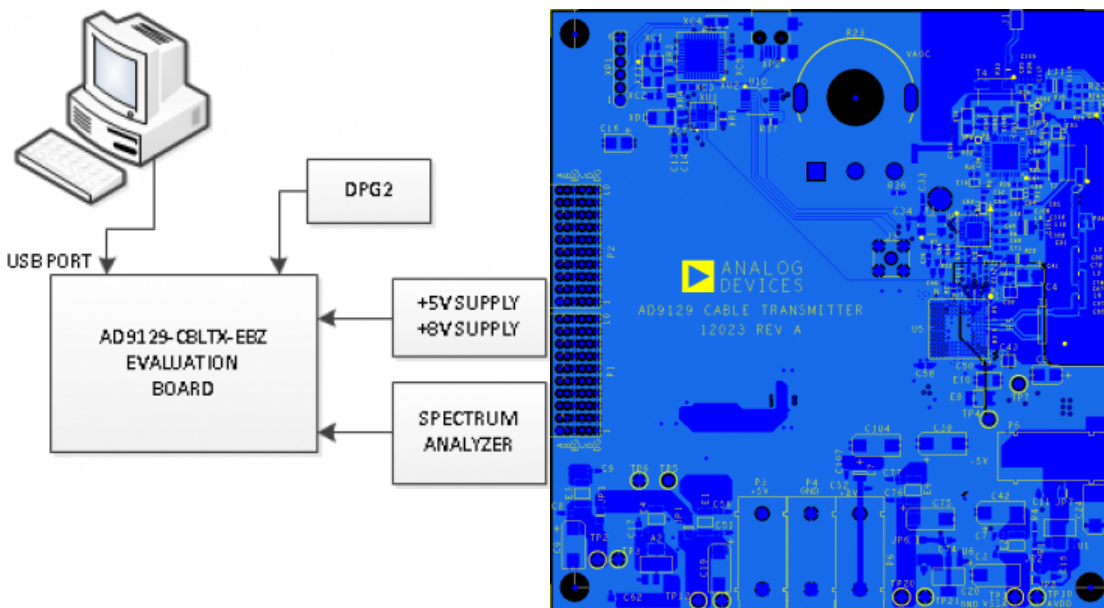


Figure 1 - Block diagram of the AD9129 lab bench set-up

Figure 2 - Top view of AD9129-CBLTX-EBZ Evaluation Board

Getting Started

The PC software comes on the included Evaluation Board CD, but may also be downloaded from the DPG Web site at <http://www.analog.com/dpg>. The installation will include the DPG Downloader and ADF4350 programming software as well as all the necessary AD9129 files including schematic, board layout, data sheet, SPI GUI, and other files. The following procedure will set up a basic 1-carrier, 256-QAM signal.

Initial Set-Up

1. Install the DPG Downloader, ADF4350, and AD9129 software and support files on your PC
2. Start the AD9129 Control Panel GUI (but don't hit the run arrow yet)
3. Connect the EVB to your PC and lab equipment as shown in Figure 1 above. Use a USB cable to connect your PC to the EVB, and another USB cable to connect your PC to the DPG2 unit. Note that a DPG3 unit can also be used.
4. Start the ADF4350 SPI for AD9129

It is suggested that the basic set-up is verified before making any modifications to the evaluation board.

Load Initial Settings

To begin, open the AD9129 SPI application (Start > Programs > Analog Devices > AD9129 > AD9129_27 SPI). The screen should look similar to Figure 3 on the Common tab. The AD9129 SPI loads default settings that should be usable for most applications.

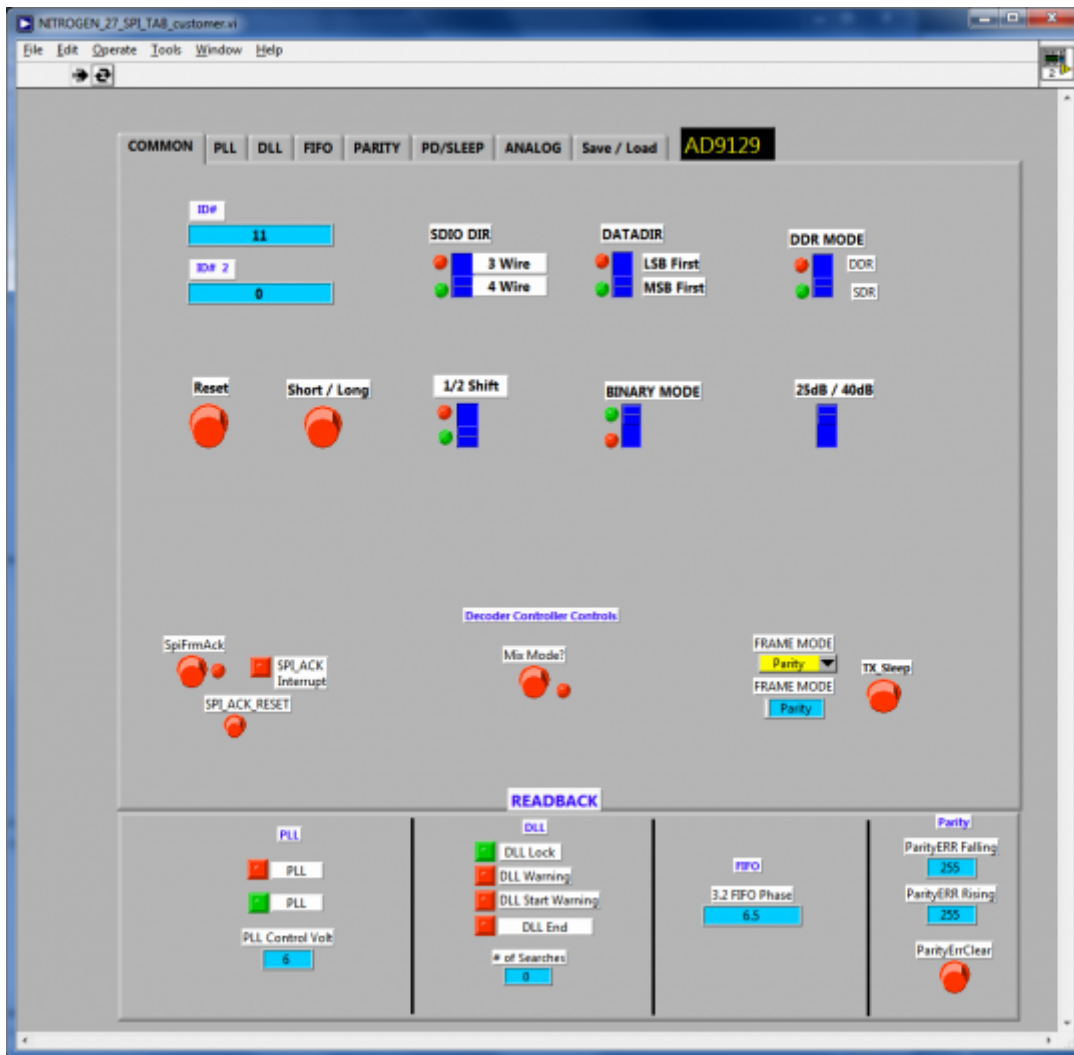


Figure 3. Entry screen of the AD9129 SPI GUI

Configure Hardware

Configure the hardware according to the hardware set-up instructions given in the Hardware Setup section above. The spectrum analyzer can be configured with Start Frequency = 20 MHz, Stop Frequency 1 GHz, and Resolution Bandwidth of 100 kHz. Use an Average/RMS detector setting, and choose Input Attenuation to be 10 dB. This can be adjusted later if indications are that the analyzer is causing degradations (warnings on the analyzer itself, or third order products appearing on the output spectrum.). The potentiometer should be tuned so that VAGC, the automatic gain control voltage for the power amplifier, is 1.2 V to replicate the following example measurements.

Program the PLL

Open the ADF4350 SPI application (Start>Programs>Analog Devices> AD9129>ADF4350 SPI for AD9129) that programs the external PLL on the board. The screen should look like Figure 4 on the Main Window tab.

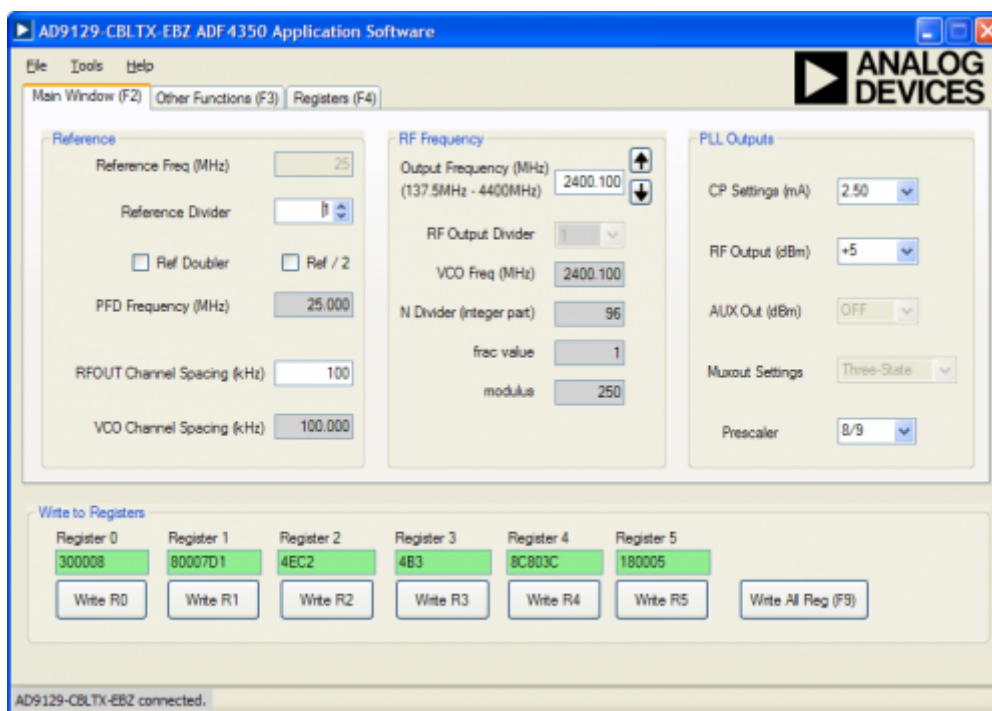


Figure 4. Main Window of the ADF4350 SPI GUI

The PLL and the chosen reference crystal do not allow for as much frequency precision as the DPG, which specifies its sample frequency down to tens of Hertz. A suggested accuracy for this evaluation board is 100 kHz. To achieve this level of precision, the “Reference Divider” is changed to 250 so that the “PFD Frequency” changes to 0.100 MHz. Then, in the “RF Frequency” section, the “Output Frequency” box should be changed to 2305 MHz to most closely match the DPG sample frequency of 2.30503091 GHz. The discrepancy between the data sample frequency and the programmed clock frequency may create some low level distortion, but the effects have proven negligible in lab. The rest of the settings may be left in their default states. Click the “Write All Reg” button, and the boxes along the bottom of the screen should change from green to grey, indicating that the registers have been programmed.

Enable the PLL

On the “PLL” tab, the “Controller Ena” button should be green. Click the “Play” button (⏮) to program the registers. The Readback light next to the button should change from red to green, and the PLL LOCK light should turn green. Note that in some cases, it may be necessary to click the “Controller Reset” button (it goes to green), click the (⏮) button, and then click the “Controller Reset” button (it goes to red) and the (⏮) button again to reset the PLL in order for it to lock.

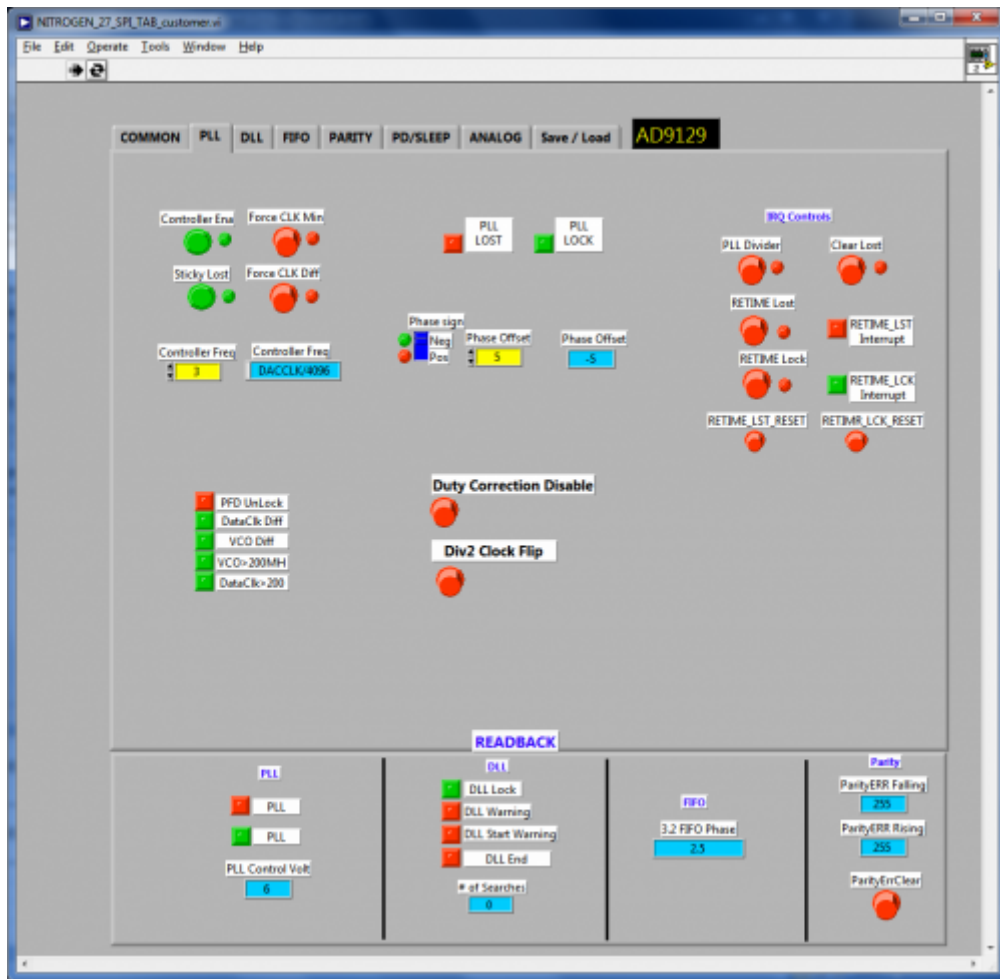


Figure 5. PLL screen of the AD9129 SPI GUI

Load Pattern from the DPG2

Open DPGDownloader (Start > Programs > Analog Devices > DPG > DPGDownloader). Ensure that the program detects the AD9129, as indicated in the “Evaluation Board” drop-down list, and select it. For this evaluation board, LVDS is the only valid Port Configuration, and it will be selected automatically. The “Data Clock Frequency” window may not yet show a clock frequency, but it normally does.

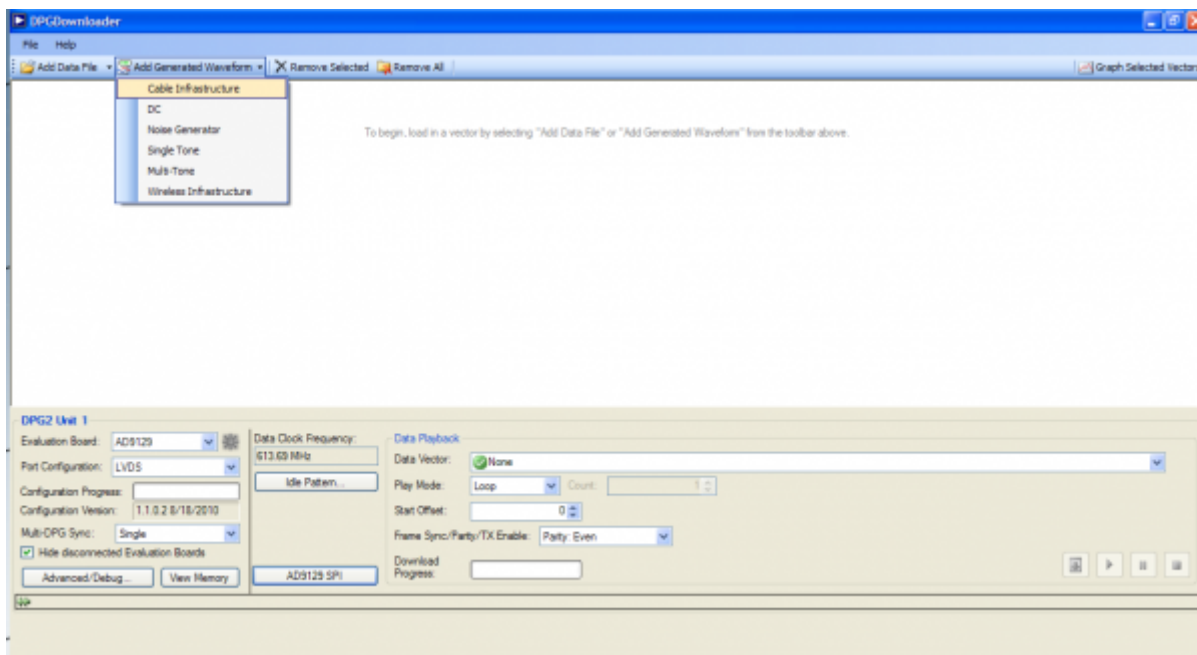


Figure 6. Choose “Cable Infrastructure” as the vector type

Click on “Add Generated Waveform”, and then “Cable Infrastructure”, as shown in Figure 6. A Cable Infrastructure panel will be added to the vector list. Enter the sample rate, or DAC clock frequency, in this case 2.305030910 GHz. Next, choose the “Resolution” to be 14 bits. Choose a center frequency of 70 MHz. Keep “Relative Amplitude” as 0 dB, and “Number of Channels” as ‘1’. Then, click the “Add Channels” button. The signal should appear on the list of signals as shown in Figure 7.

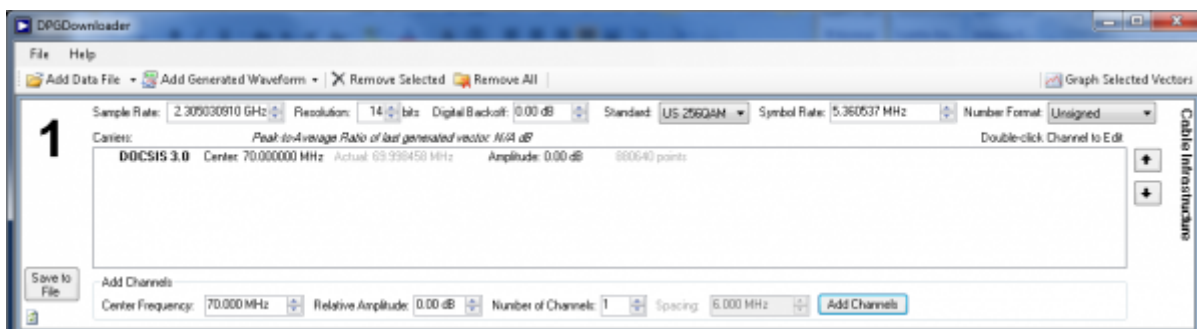


Figure 7. DPG Downloader Upper section, used to select and configure the desired signal to be generated

Next, in the lower portion of the screen, select “1I: C1FR Vector (I)” as the Data Vector. The other options can be left at their default values. The Data Clock Out (DCO) frequency from the AD9129 should be reported in the Data Clock Frequency window as roughly 576.25 MHz.

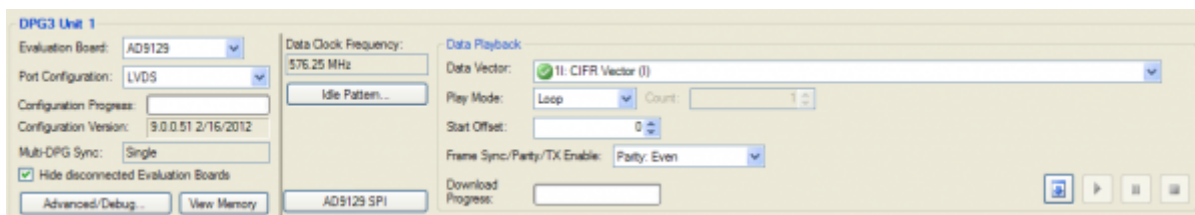







Figure 8. DPG Downloader Lower section, used to select the desired vector and download it to the DPG2 unit

Make sure the DPG2 unit is powered up and the AD9129 eval board is plugged into it correctly. Click the “Download” button () to download the pattern from the computer to the DPG2 unit, wait for the Play () button to become active, and then click the Play () button to begin vector playback to the AD9129.

Enable the LVDS Controller

On the AD9129 SPI GUI’s “DLL” tab, the “DUTY Corr Ena” button and the “DLL_ENA” button should be green (selected). Click the () button to program the registers. The Readback light next to both buttons should change from red to green, and the DLL Lock light should change from red to green. It may be necessary to click the () button again to get a full readback status since the controller may take slightly longer to lock than the GUI allowed on the first write and then readback.

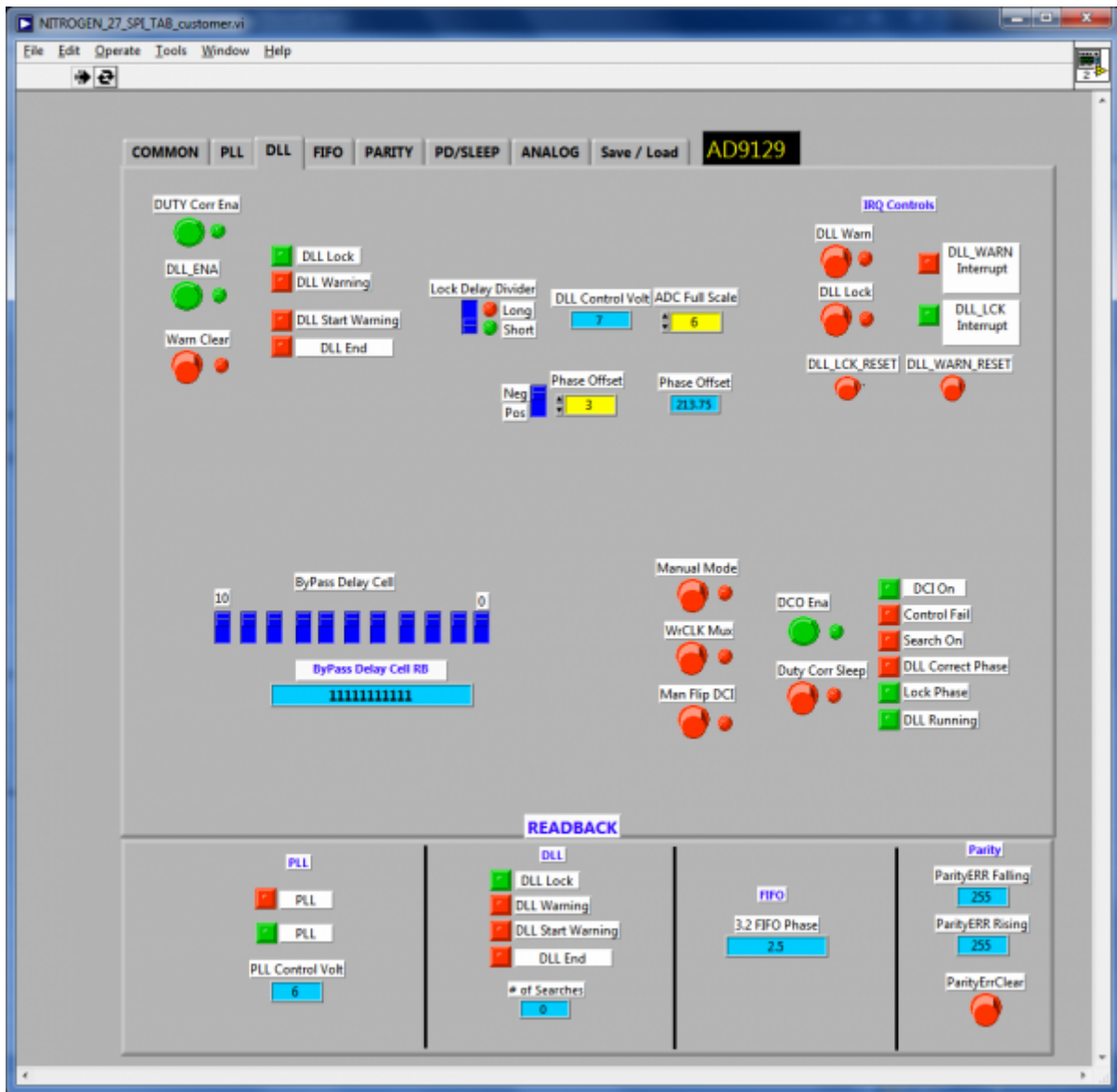


Figure 9. DLL screen of the AD9129 SPI GUI

In rare cases, the data link may have gotten corrupted and the registers not programmed correctly. In these cases, the output of the DAC will show significantly degraded performance. To remedy this situation, click the “DUTY Corr Ena” button and the “DLL_ENA” buttons, and then click the (⊕) button to program the registers. Then, re-click the “DUTY Corr Ena” button and the “DLL_ENA” buttons, and then click the (⊖) button to program the registers. This disables and re-enables the Data Interface DLL and allows it to re-lock to the DCI. At this time, it is also possible to click the “Repeat” button (🔄) to continuously program the part, making the SPI GUI run in a more interactive mode.

Result

The final result should be a single 256-QAM carrier centered at 70 MHz, as shown in Figure 10. An attenuation of 30 dB was used in this measurement, which raises the noise floor of the measurement, but avoided saturating the input and causing higher-ordered products being created. Selecting



appropriate attenuation becomes especially important for the cable transmitter board, since its output power is relatively high. A 6 dB pad was used at the output of the board to add some attenuation before the input of the spectrum analyzer. The output signal in Figure 10 is tuned to a level 2 dB above the DOCSIS requirements for a single channel. This is accomplished by adjusting the Vagc knob until the appropriate level is achieved. The power is best adjusted using a narrow span on the spectrum analyzer. In Figure 11, an adjacent channel power ratio (ACPR) measurement is done and in that measurement the power of the signal is properly measured. The measurement is taken with a 6 dB pad at the input to the spectrum analyzer, so 6 dB must be added to the result seen in the plot.

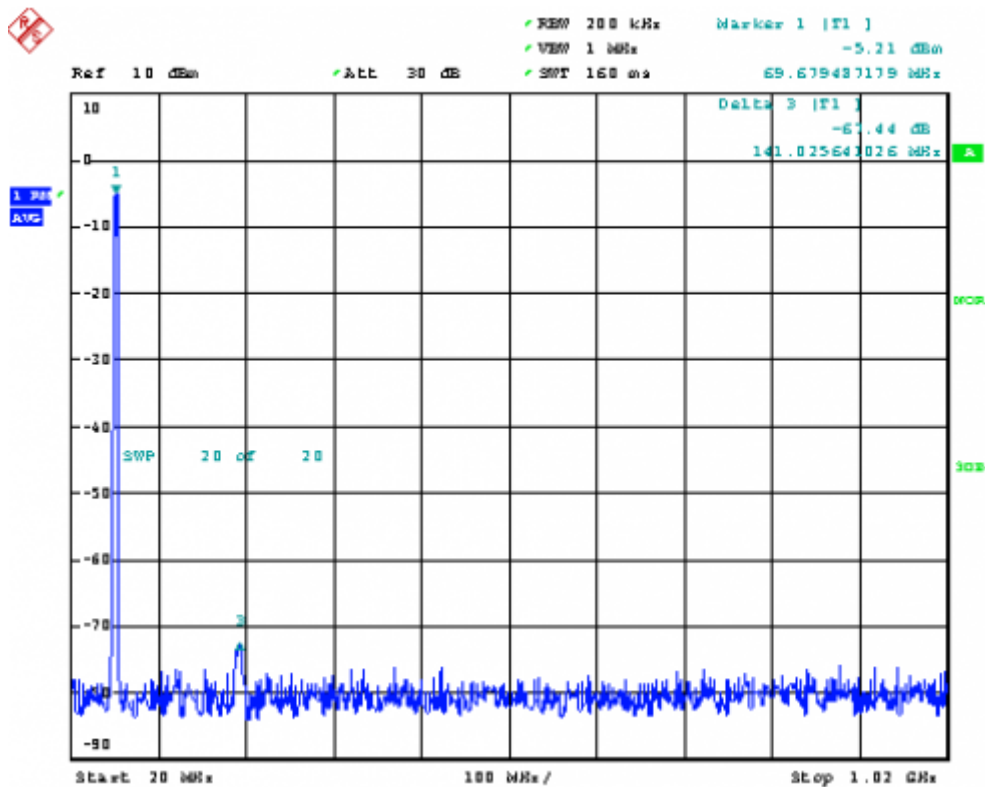


Figure 10. Single 256-QAM channel at AD9129-CBLTX-EBZ output

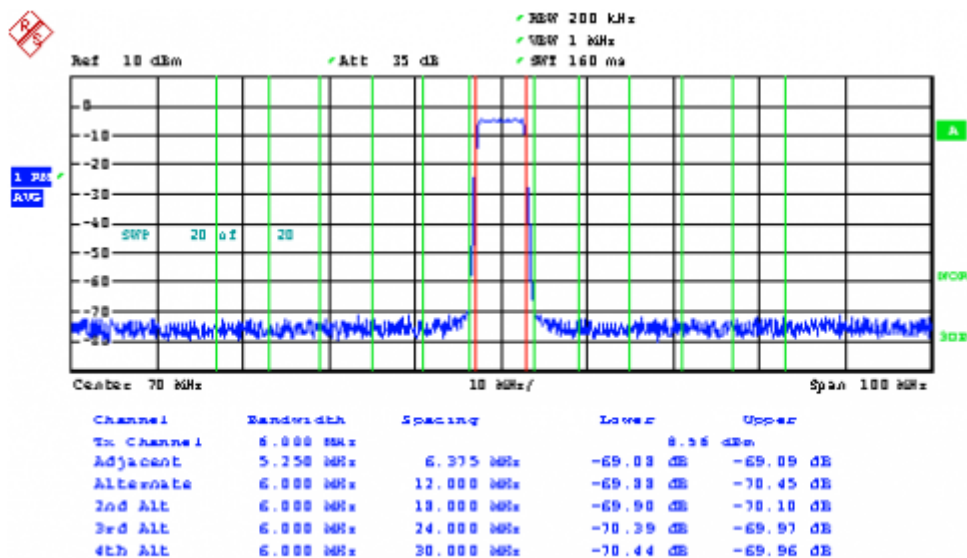


Figure 11. ACPR measurement of single 256-QAM channel at AD9129 output

Full Band Measurement

To check for flatness across the full cable band, the user can create a new vector or load the vector included in the EVB document package. To do this, select “Add Data File” in the DPG Downloader window, as shown in Figure 12.

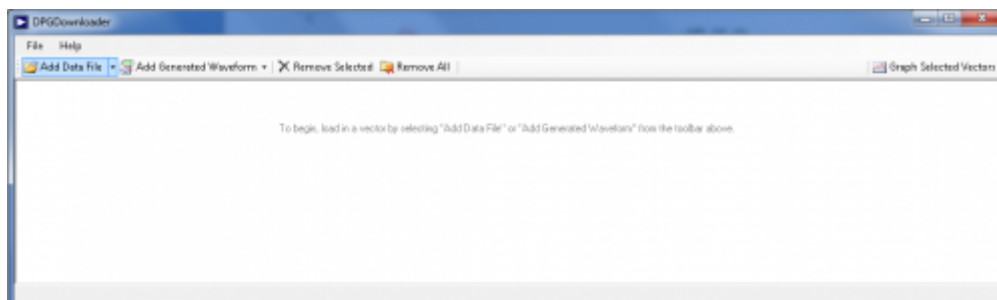


Figure 12. Choosing “Add Data File” in DPG Downloader

Then, choose the file called “158Channel2.3GSample0dBbackoff.txt” in the C:\Program Files (x86)\Analog Devices\HSDAC\AD9129 folder. Click the button to download the pattern from the computer to the DPG2 unit, wait for the Play () button to become active, and then click the Play () button to begin vector playback to the AD9129. Then, re-initialize and lock the LVDS interface by clicking the “DUTY Corr Ena” button and the “DLL_ENA” buttons, and then clicking the () button to program the registers. Then, re-click the “DUTY Corr Ena” button and the “DLL_ENA” buttons, and then click the () button to program the registers. This disables and re-enables the Data Interface DLL and allows it to re-lock to the DCI. If the () button has been pressed and the SPI is in continuous programming mode, the () button does not need to be pressed. The registers will be programmed when each of the DUTY Corr Ena and DLL_ENA buttons are pressed. The output spectrum should then appear similar to that in Figure 13. Note that the analyzer settings have been changed to show more

detail, with 2 dB/division on the vertical scale. It can be seen that there is about 1.4 dB of variation in output amplitude across the band, meeting DOCSIS 3.0 specifications.

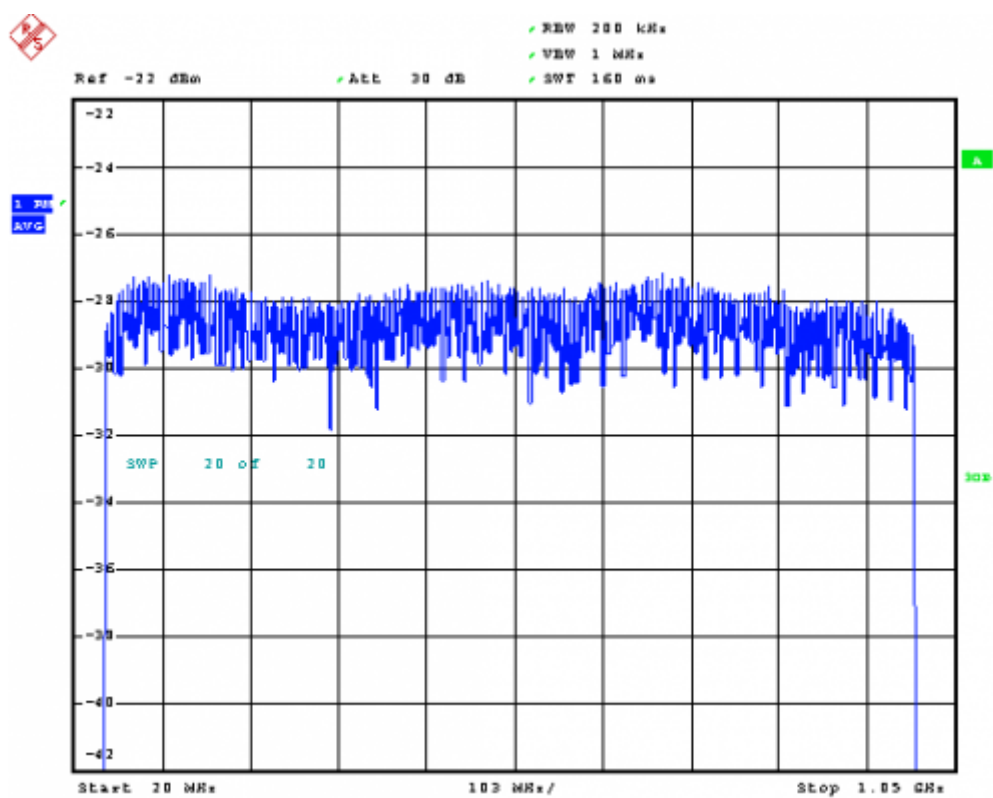


Figure 13. Full cable band spectrum with 158 channels transmitted

SPI Software

The AD9129 SPI software is conveniently organized in a series of tabs that groups registers according to their functions. In this way, all registers associated with the fDAC PLL, for example, are on the “PLL” tab, all registers associated with the data clock Delay Locked Loop (DLL) are on the “DLL” tab, and so on. A full description of each register and its settings is given in the AD9129 data sheet. Some of the registers and their functions are described here as they pertain to the AD9129 evaluation board. Please note that some of the screen images in this document may not match exactly with the latest revision of the software, due to ongoing improvements and enhancements to the software. The full screen layout is shown in Figure 14. The tabs can be seen across the top of the work area, and a “READBACK” area is below the active tab area. This READBACK section is present on each of the tabs, so that the user can quickly assess status of the PLL and DLL lock, as well as parity and the FIFO phase. Each of the tabs is discussed in its own section below.

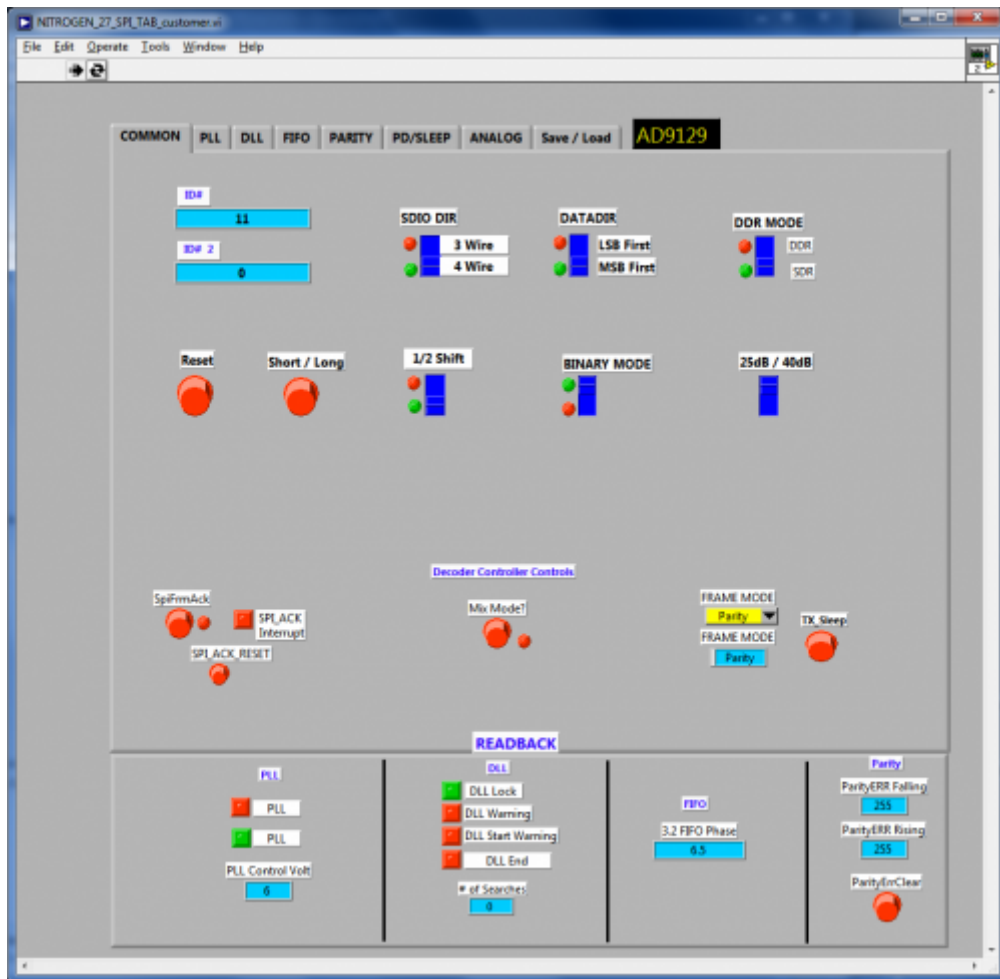


Figure 14. Common tab on the AD9129 SPI GUI

Common Tab

The common tab has selections that apply to the general configuration of the DAC. The Reset bit is set or reset here, as well as basic configuration of the serial port: Short vs. Long mode; SDIO pin as an output or bi-directional, MSB or LSB first for the data words, format of the data words (unsigned or two's complement), and whether the 2x interpolator filter is ENabled ("DDR") or DISabled ("SDR"). With the 2x interpolator filter enabled, two filter options are available to provide either 25 or 40 dB of out of band rejection. Filter selection is controlled in the common tab. The mode of the Frame/Parity pins is also chosen on this tab, along with MixMode™ or Normal mode for the DAC output. Finally, the SPI_FRM_ACK bit (reg 0x11[6]) is set on this tab. That bit is used to flag an interrupt if the SPIFrmReq bit is set, which indicates that a SPI-based FIFO alignment has been requested.

PLL Tab

The PLL tab has functions associated with the DAC clock PLL on it. In addition to the enable bit discussed in the Getting Started section,

this tab also has settings associated with the PLL retimer registers, reg 0x33 - 0x38. The interrupt control and status bits associated with the PLL (in regs 0x03 - 0x06) are also in this section.

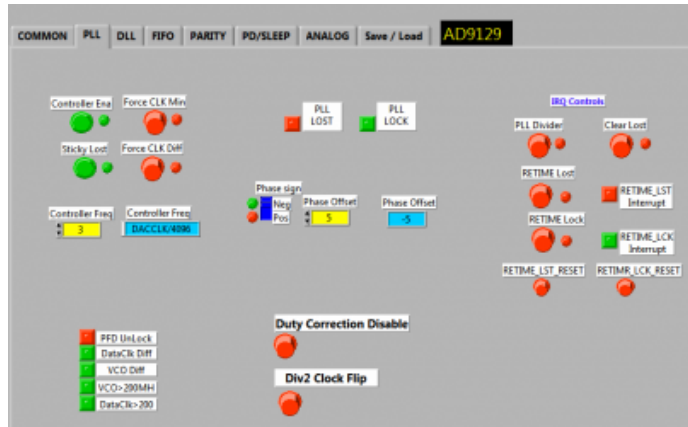


Figure 15. PLL tab of the AD9129 SPI GUI

DLL Tab

The DLL tab has the DLL Enable and Duty Cycle Correction Enable bits as discussed in the Getting Started section. Additional status bits associated with the Data interface DLL are also on this tab, including lock status bits, lock lost bit, warning bits, etc. These are mostly located in the Data Control and Data Status registers, regs 0x0A - 0x0F. The bypass delay cell area is for test only and can be ignored.

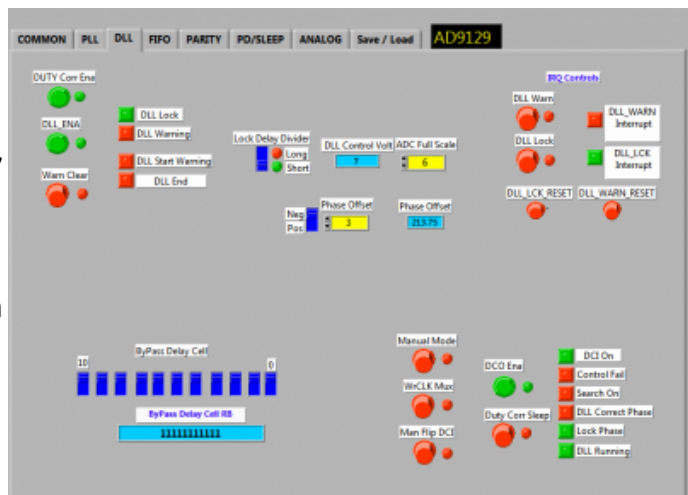


Figure 16. DLL tab of the AD9129 SPI GUI

FIFO Tab

The FIFO tab has controls and status lights associated with the data interface FIFO. For most uses of the AD9129 EVB, these controls can be left in their default state, and there is no need to change them in the SPI. For more details on the FIFO's operation and the control and status registers for it, please consult the AD9129 Data Sheet. The FIFO registers are located in address range 0x11 - 0x17.

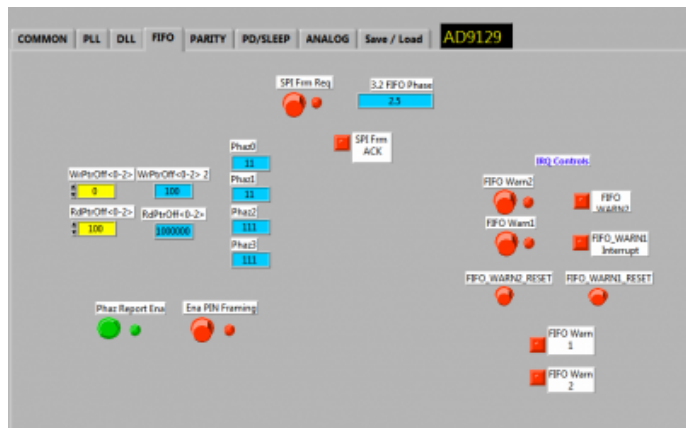




Figure 17. FIFO tab of the AD9129 SPI GUI

Parity Tab

Similar to the FIFO tab, the Parity tab can be left in its default state for most uses of the AD9129 EVB. Parity can be enabled and disabled on this tab, and Even or Odd Parity can be chosen. The parity counter values are also shown. These controls and status bits are associated with the parity registers located at addresses 0x5C - 0x5E. The parity interrupts are in the Interrupt Control and Status registers, 0x03 - 0x06. To reset the parity counters, click the PARITY_FALL_RESET and PARITY_RISE_RESET buttons, then press the  button repeatedly until the values are reset. Alternatively, the  button can be pressed, and then the SPI programming will run in a loop, and the count values can be observed to go to '0', at which time the PARITY_FALL_RESET and PARITY_RISE_RESET buttons can be unclicked.

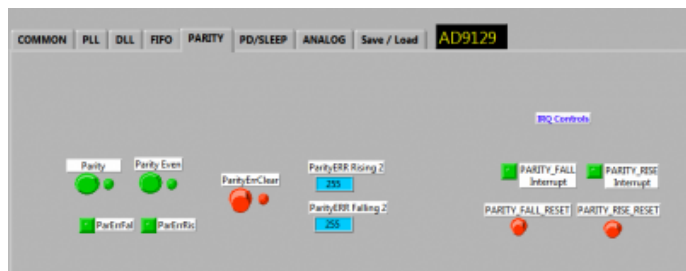


Figure 18. PARITY tab of the AD9129 SPI GUI

Power Control (PD) Tab

The Power Control, or Power Down, tab contains individual controls to power down various blocks on the AD9129. These are associated with the power down registers,

0x01 and 0x02.



Figure 19. Power Down tab of the AD9129 SPI GUI

Analog Tab

On the Analog tab, the Full Scale Current of the DAC output can be set by using the increment/decrement arrows or by typing an integer value into the yellow window. This updates registers 0x20 and 0x21 with the new value. The other controls on this tab should be left to their default values.

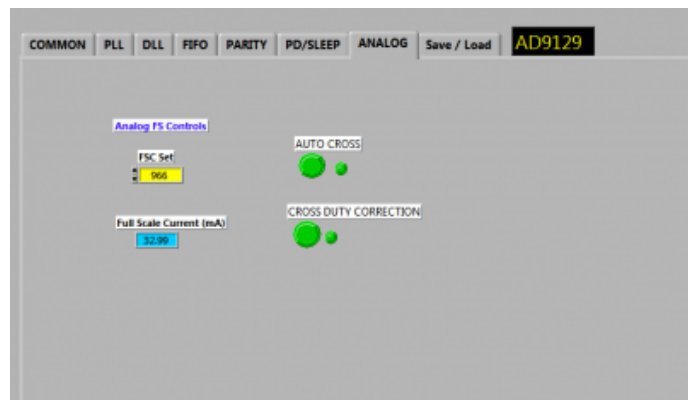


Figure 20. Analog control tab of the AD9129 SPI GUI

Save/Load Tab

The Save/Load tab enables a different way of configuring the AD9129. The “Save” function allows a user to save to a file all of the settings currently set in the various tabs. The “Load” function allows these settings to be recalled and loaded at a later date. While useful in some situations, this method of loading saved settings does not modify the screens or the tabs, it simply loads the

settings directly to the DAC, so it can be confusing to use this function. It is recommended that the user begin with the user GUI and tab interface, and only use this "Save/Load" function as an advanced feature.

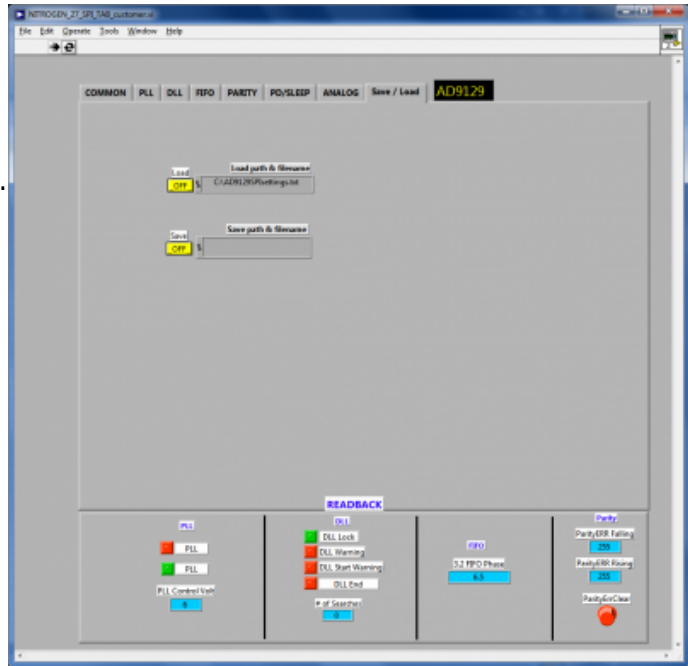


Figure 21. Save/Load tab of the AD9129 SPI GUI

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