

FCD380N60E

600V N-Channel MOSFET

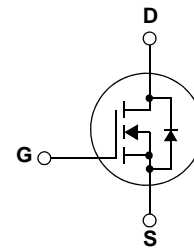
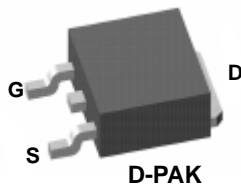
Features

- 650V @ $T_J = 150^\circ\text{C}$
- Max. $R_{DS(on)} = 380\text{m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 34\text{nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss,eff} = 97\text{pF}$)
- 100% Avalanche Tested

Description

SuperFET®II is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET®II is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCD380N60E	Units
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC ($f > 1\text{Hz}$)	± 30
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	10.2
		-Continuous ($T_C = 100^\circ\text{C}$)	6.4
I_{DM}	Drain Current - Pulsed (Note 1)	30.6	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	211.6	mJ
I_{AR}	Avalanche Current (Note 1)	2.3	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	1.06	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
	MOSFET dv/dt	100	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	106
		- Derate above 25°C	0.85
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCD380N60E	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.18	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD380N60E	FCD380N60E	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10mA, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0V, I_D = 10mA, T_J = 150^\circ\text{C}$	650	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10mA, \text{Referenced to } 25^\circ\text{C}$	-	0.67	-	$V/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0V, I_D = 10A$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480V, V_{GS} = 0V$	-	-	5	μA
		$V_{DS} = 480V, T_C = 125^\circ\text{C}$	-	-	20	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 5A$	-	0.32	0.38	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V, I_D = 5A$	-	10	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V$ $f = 1\text{MHz}$	-	1330	1770	pF
C_{oss}	Output Capacitance		-	945	1260	pF
C_{rss}	Reverse Transfer Capacitance		-	60	90	pF
C_{oss}	Output Capacitance	$V_{DS} = 380V, V_{GS} = 0V, f = 1.0\text{MHz}$	-	25	-	pF
$C_{oss \text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0V \text{ to } 480V, V_{GS} = 0V$	-	97	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380V, I_D = 5A$ $V_{GS} = 10V$	-	34	45	nC
Q_{gs}	Gate to Source Gate Charge		-	5.3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	13	-
ESR	Equivalent Series Resistance	Drain open	-	6	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380V, I_D = 5A$ $V_{GS} = 10V, R_G = 4.7\Omega$	-	17	44	ns
t_r	Turn-On Rise Time		-	9	28	ns
$t_{d(off)}$	Turn-Off Delay Time		-	64	138	ns
t_f	Turn-Off Fall Time		(Note 4)	-	10	30

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	10.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	30.6	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 5A$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_{SD} = 5A$	-	240	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100A/\mu\text{s}$	-	3	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 2.3A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 5.1A, di/dt \leq 200A/\mu\text{s}, V_{DD} \leq BV_{DSS}, \text{Starting } T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

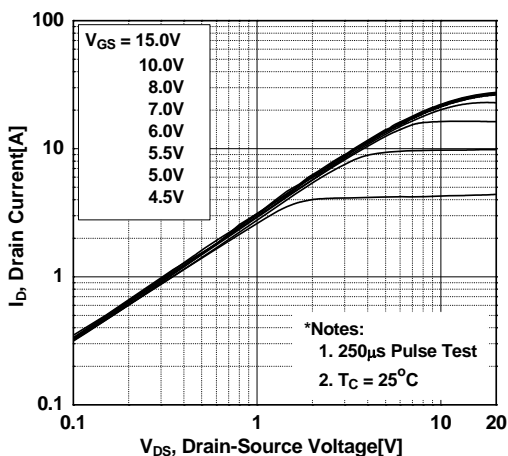


Figure 2. Transfer Characteristics

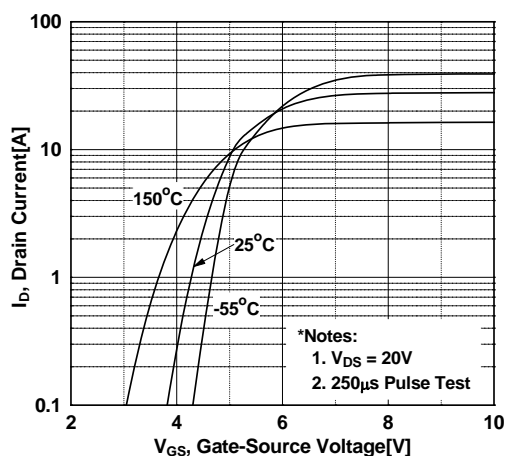


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

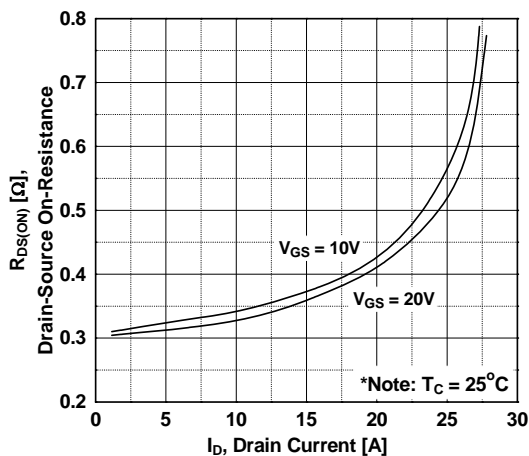


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

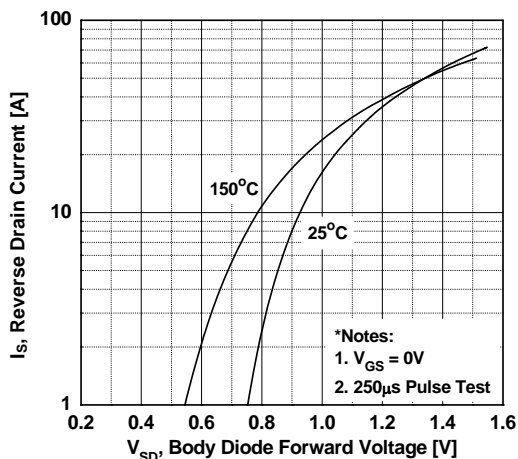


Figure 5. Capacitance Characteristics

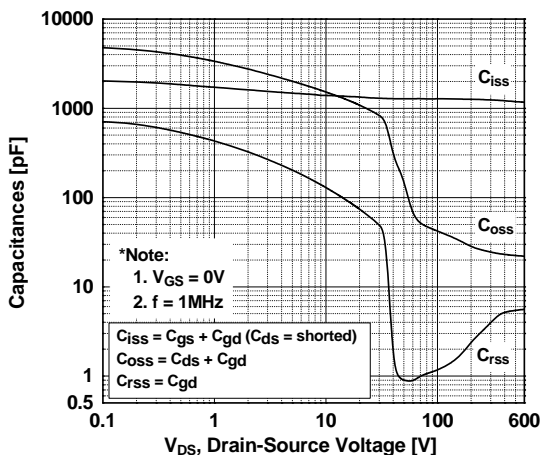
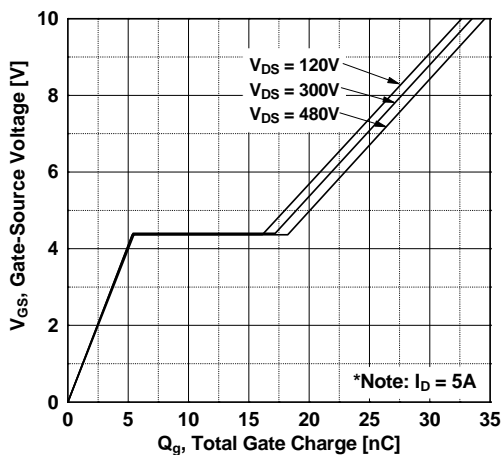


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

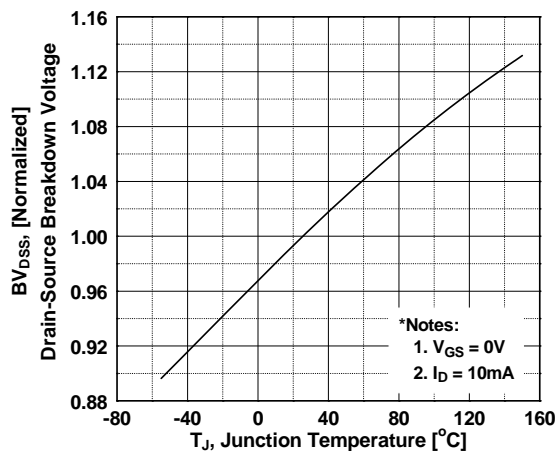


Figure 8. On-Resistance Variation vs. Temperature

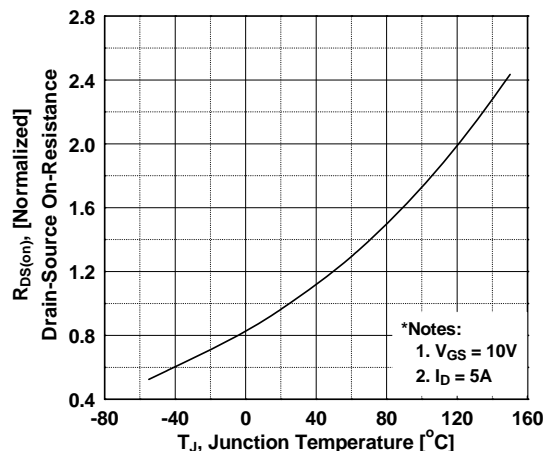


Figure 9. Maximum Safe Operating Area vs. Case Temperature

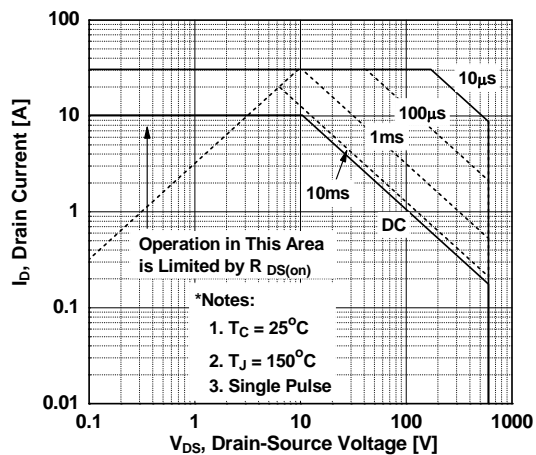


Figure 10. Maximum Drain Current

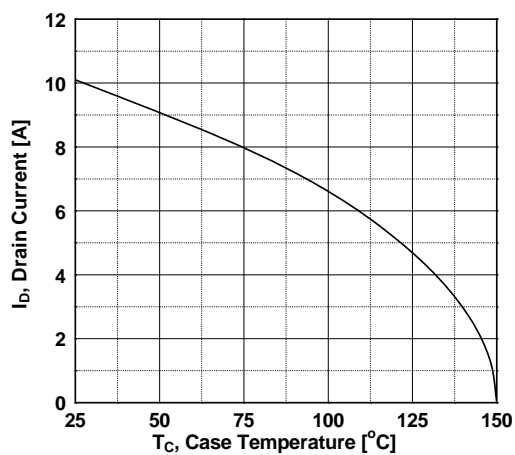
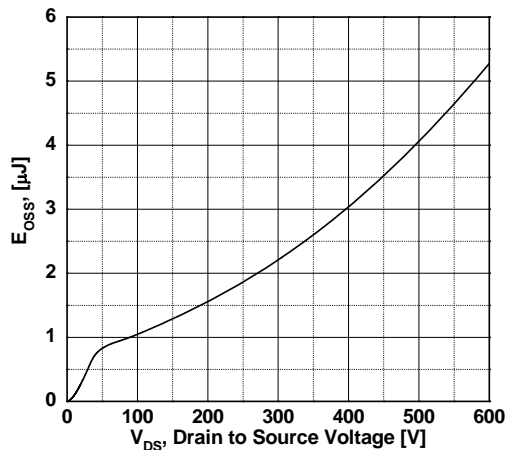
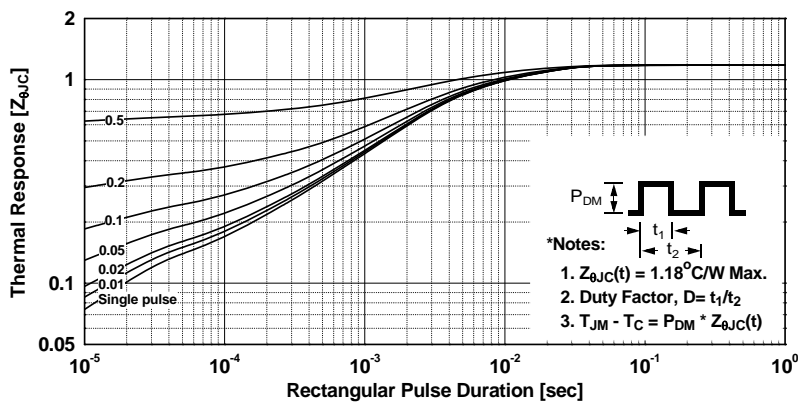


Figure 11. E_oss vs. Drain to Source Voltage Switching Capability

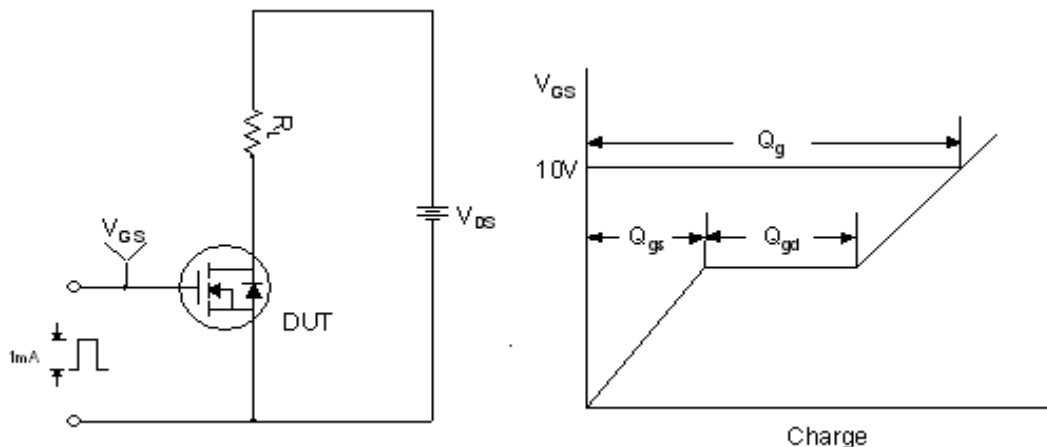


Typical Performance Characteristics (Continued)

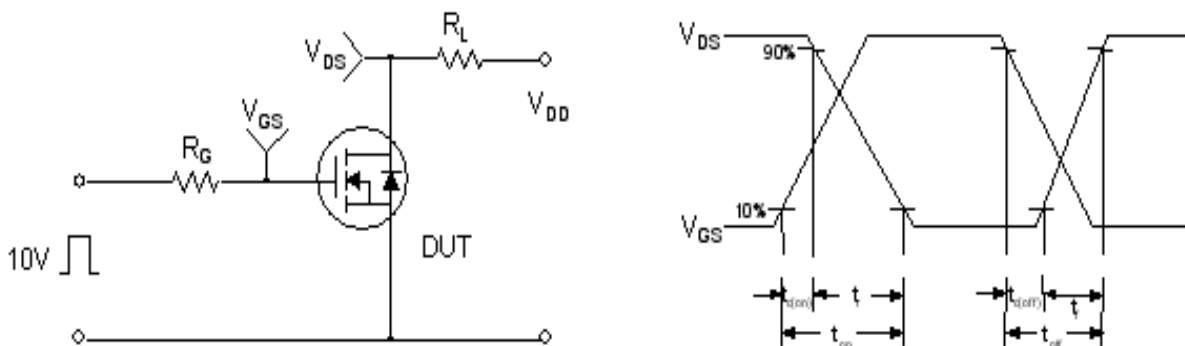
Figure 12. Transient Thermal Response Curve



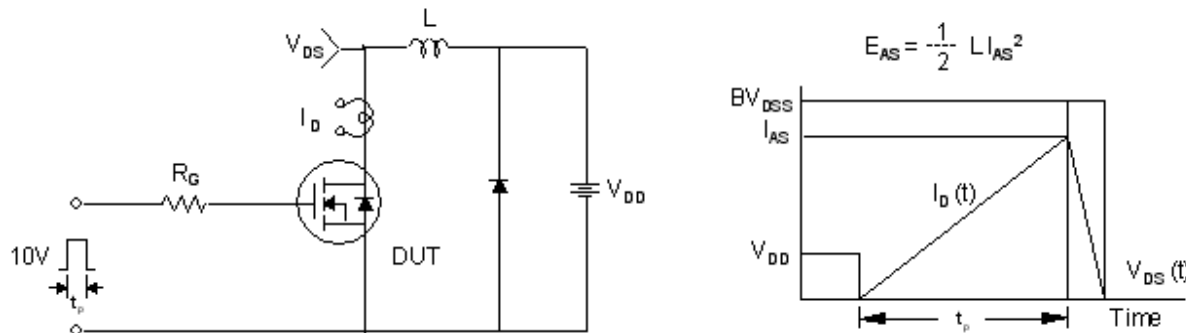
Gate Charge Test Circuit & Waveform



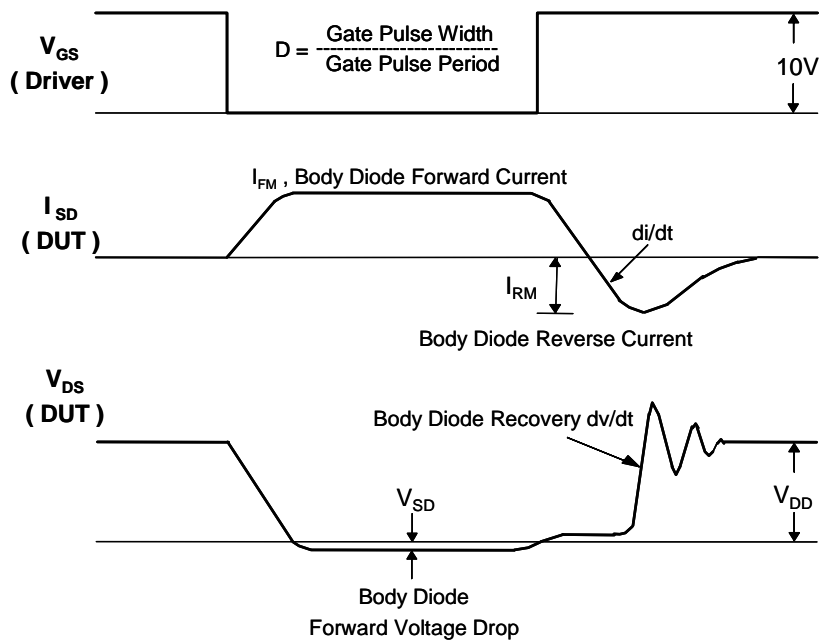
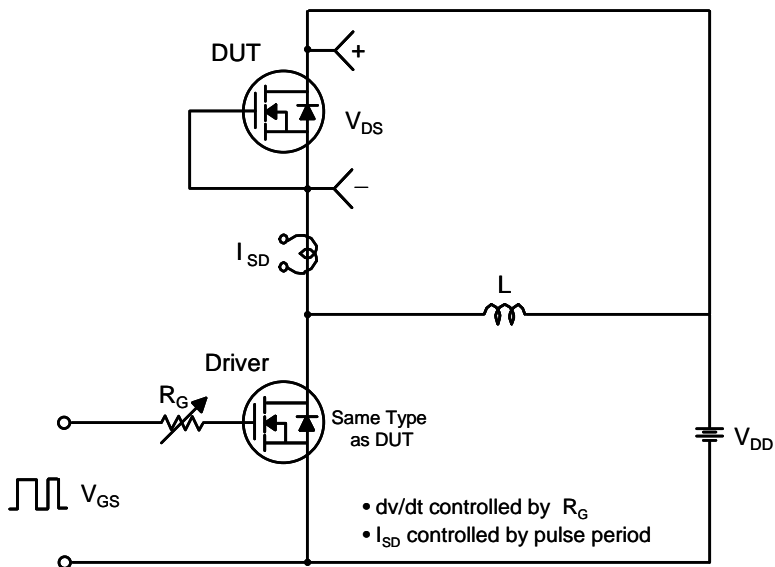
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

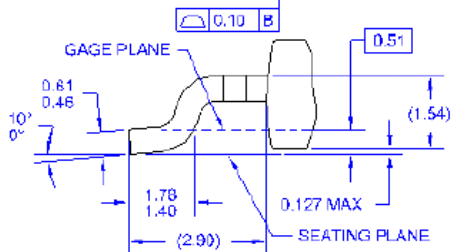
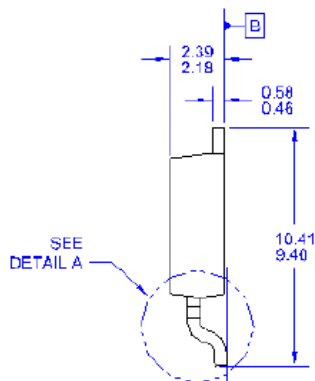
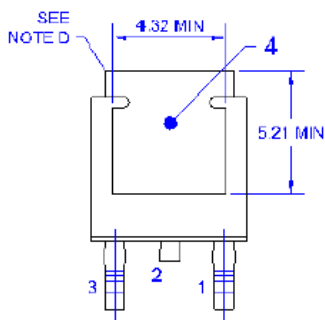
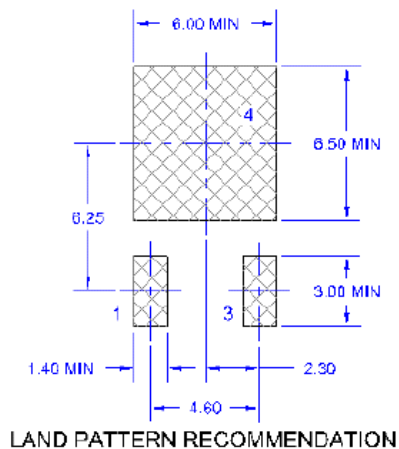
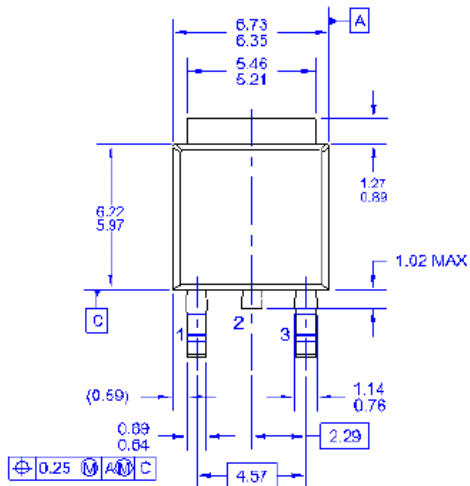


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252 ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A, STD TO220P1003X238-3N.
 H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Dimensions in Millimeters



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| AX-CAP™* | Global Power ResourceSM | Programmable Active Droop™ | franchise® |
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| Build it Now™ | Green FPS™ | QS™ | TinyBuck™ |
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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I61