



FAN48630 — 2.5 MHz, 1500 mA, Synchronous TinyBoost™ Regulator with Bypass Mode

Features

- Few External Components: 0.47 μ H Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range: 2.35 V to 5.5 V
- Fixed Output Voltage Options: 3.0 V to 5.0 V
- Maximum Continuous Load Current: 1500 mA at V_{IN} of 2.6 V Boosting V_{OUT} to 3.5 V
- Up to 96% Efficient
- True Bypass Operation when $V_{IN} >$ Target V_{OUT}
- Internal Synchronous Rectifier
- Soft-Start with True Load Disconnect
- Forced Bypass Mode
- V_{SEL} Control to Optimize Target V_{OUT}
- Short-Circuit Protection
- Low Operating Quiescent Current
- 16-Bump, 0.4 mm Pitch WLCSP

Applications

- Boost for Low-Voltage Li-ion Batteries, Brownout Prevention, Boosted Audio, USB OTG, and LTE / 3G RF Power
- Cell Phones, Smart Phones, Portable Instruments

Description

The FAN48630 allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The FAN48630 is a boost regulator designed to provide a minimum output voltage ($V_{OUT(MIN)}$) from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. Output voltage regulation is guaranteed to a maximum load current of 1500 mA. Quiescent current in Shutdown Mode is less than 3 μ A, which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The FAN48630 is available in a 16-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

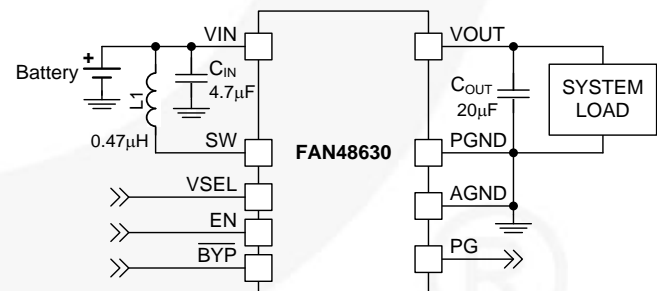


Figure 1. Typical Application

Ordering Information

Part Number	Output Voltage ⁽¹⁾ V _{SEL0} / V _{SEL1}	Soft-Start	Forced Bypass	Operating Temperature	Package	Packing
FAN48630UC315X	3.15 / 3.33	FAST	Low I _Q	-40°C to 85°C	16-Ball, 4x4 Array, 0.4 mm Pitch, 250 μm Ball, Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel
FAN48630BUC315X ⁽²⁾	3.15 / 3.33	FAST	Low I _Q			
FAN48630UC33X	3.30 / 3.49	FAST	Low I _Q			
FAN48630UC35X	3.50 / 3.70	FAST	Low I _Q			
FAN48630UC37AX	3.70 / 3.77	FAST	Low I _Q			
FAN48630UC45X	4.50 / 4.76	SLOW	OCP On			
FAN48630UC50X	5.00 / 5.29	SLOW	OCP On			

Notes:

- Other output voltages are available on request. Please contact a Fairchild Semiconductor representative.
- The FAN48630BUC315X includes backside lamination.

Typical Application

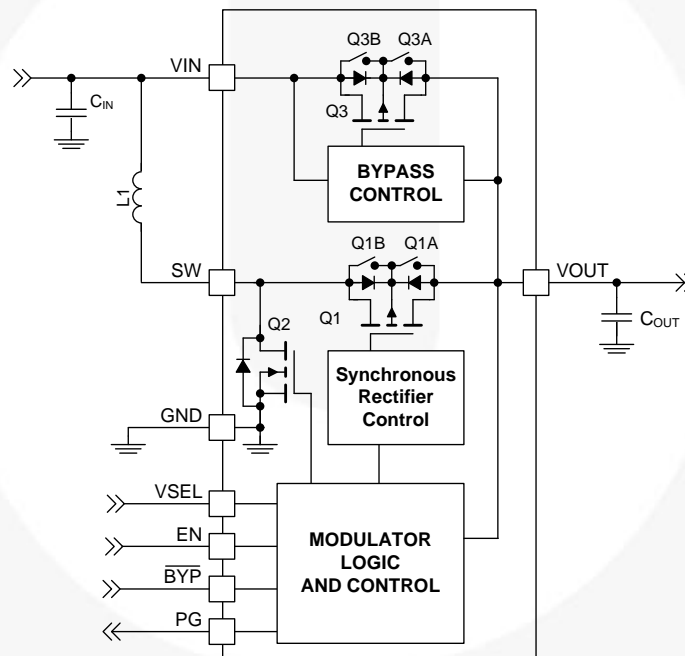


Figure 2. Block Diagram

Table 1. Recommended Components

Component	Description	Vendor	Parameter	Typ.	Unit
L1	0.47 μH, 30%	Toko: DFE201612C DFR201612C Cyntec: PIFE20161B	L	0.47	μH
			DCR (Series R)	40	mΩ
C _{IN}	4.7 μF, 10%, 6.3 V, X5R, 0603	Murata: GRM188R60J475K TDK: C1608X5R0J475K	C	4.7	μF
C _{OUT}	2 x 10 μF, 20%, 10 V, X5R, 0603	TDK: C1608X5R1A106M	C	20	μF

Pin Configuration

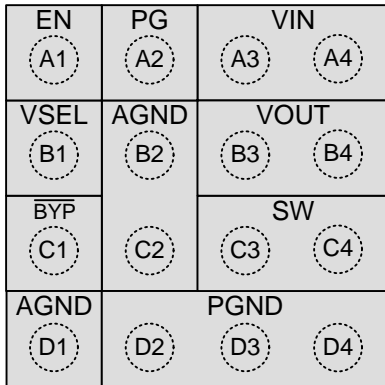


Figure 3. Top Through View (Bumps Down)

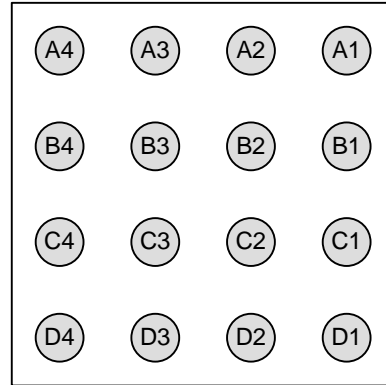


Figure 4. Bottom View (Bumps Up)

Pin Definitions

Pin #	Name	Description
A1	EN	Enable. When this pin is HIGH, the circuit is enabled. ⁽³⁾
A2	PG	Power Good. This is an open-drain output. PG is actively pulled LOW if output falls out of regulation due to overload or if thermal protection threshold is exceeded.
A3–A4	VIN	Input Voltage. Connect to Li-Ion battery input power source. ⁽³⁾
B1	VSEL	Output Voltage Select. When boost is running, this pin can be used to select output voltage.
B2, C2 D1	AGND	Analog Ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
B3–B4	VOUT	Output Voltage. Place C _{OUT} as close as possible to the device.
C1	$\overline{\text{BYP}}$	Bypass. This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches (Q3 and Q1) are turned on and the IC is otherwise inactive.
C3–C4	SW	Switching Node. Connect to inductor.
D2–D4	PGND	Power Ground. This is the power return for the IC. The C _{OUT} bypass capacitor should be returned with the shortest path possible to these pins.

Note:

- Do not connect the EN pin to VIN. A logic voltage of 1.8 V should control the EN pin and enable / disable the device.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN} Input Voltage		-0.3	6.5	V
V_{OUT}	V_{OUT} Output Voltage			6.0	V
	SW Node	DC	-0.3	8.0	V
		Transient: 10 ns, 3 MHz	-1.0	8.0	V
	Other Pins		-0.3	6.5 ⁽⁴⁾	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	3.0		kV
		Charged Device Model per JESD22-C101	1.5		kV
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

4. Lesser of 6.5 V or $V_{IN} + 0.3$ V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.35	5.50	V
I_{OUT}	Output Current	0	1500	mA
T_A	Ambient Temperature	-40	+85	°C
T_J	Junction Temperature	-40	+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer Fairchild evaluation boards (1 oz copper on all layers). Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A .

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	80	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	42	

Electrical Specifications

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, $V_{IN} = 2.35\text{ V}$ to V_{OUT} , $T_A = -40^\circ\text{C}$ to 85°C . Typical values are given $V_{IN} = 3.0\text{ V}$ and $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_Q	V_{IN} Quiescent Current	Bypass Mode $V_{OUT}=3.5\text{ V}$, $V_{IN}=4.2\text{ V}$		140	190	μA
		Boost Mode $V_{OUT}=3.5\text{ V}$, $V_{IN}=2.5\text{ V}$		150	250	μA
		Shutdown: $\text{EN}=0$, $V_{IN}=3.0\text{ V}$		1.5	5.0	μA
		Forced Bypass Mode $V_{OUT}=3.5\text{ V}$, $V_{IN}=3.5\text{ V}$	Low I_Q		4	10
OCP On			45	90	μA	
I_{LK}	V_{OUT} to V_{IN} Reverse Leakage	$V_{OUT}=5\text{ V}$, $\text{EN}=0$		0.2	1.0	μA
I_{LK_OUT}	V_{OUT} Leakage Current	$V_{OUT}=0$, $\text{EN}=0$, $V_{IN}=4.2\text{ V}$		0.1	1.0	μA
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising		2.20	2.35	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			200		mV
$V_{PG(OL)}$	PG Low	$I_{PG}=5\text{ mA}$			0.4	V
I_{PG_LK}	PG Leakage Current	$V_{PG}=5\text{ V}$			1	μA
V_{IH}	Logic Level High EN , VSEL , BYP		1.2			V
V_{IL}	Logic Level Low EN , VSEL , BYP				0.4	V
R_{LOW}	Logic Control Pin Pull Downs (LOW Active)	BYP , VSEL , EN		300		$\text{k}\Omega$
I_{PD}	Weak Current Source Pull-Down	BYP , VSEL , EN		100		nA
V_{REG}	Output Voltage Accuracy	Referred to GND, DC, $V_{OUT}-V_{IN} > 100\text{ mV}$	-2		4	%
V_{TRSP}	Load Transient Response	500 – 1250 mA, $V_{IN}=3.6\text{ V}$, $V_{OUT}=5.0\text{ V}$		± 4		%
t_{ON}	On-Time	$V_{IN}=3.0\text{ V}$, $V_{OUT}=3.5\text{ V}$, Load $>1000\text{ mA}$		80		ns
f_{SW}	Switching Frequency	$V_{IN}=3.6\text{ V}$, $V_{OUT}=5.0\text{ V}$, Load=1000 mA	2.0	2.5	3.0	MHz
I_{V_LIM}	Boost Valley Current Limit	$V_{IN}=2.6\text{ V}$	2.6	2.9	3.1	A
$I_{V_LIM_SS}$	Boost Valley Current Limit During SS	$V_{IN}=2.6\text{ V}$		1.6		A
$V_{MIN_1.5A}$	Minimum V_{IN} for 1500 mA Load (Short Term)	$V_{OUT}=5.0\text{ V}$, $T_J < 120^\circ\text{C}$		3.0		V
		$V_{OUT}=4.5\text{ V}$, $T_J < 120^\circ\text{C}$		2.8		V
		$V_{OUT}=3.5\text{ V}$, $T_J < 120^\circ\text{C}$		2.35		V
		$V_{OUT}=3.15\text{ V}$, $T_J < 120^\circ\text{C}$		2.35		V
I_{SS_PK}	Soft-Start Input Peak Current Limit	LIN1	Slow		350	mA
			Fast		800	mA
		LIN2	Slow		700	mA
			Fast		1600	mA
t_{SS}	Soft-Start EN HIGH to Regulation	Slow, $50\ \Omega$ Load		1300		μs
		Fast, $50\ \Omega$ Load		600		μs
V_{OCP}	OCP Comparator Threshold	$V_{IN}=5.0\text{ V}$, $V_{IN}-V_{OUT}$		200		mV
V_{OVP}	Output Over-Voltage Protection Threshold			6.0	6.3	V
V_{OVP_HYS}	Output Over-Voltage Protection Hysteresis			300		mV

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Electrical Specifications (Continued)

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, $V_{IN} = 2.35\text{ V}$ to V_{OUT} , $T_A = -40^\circ\text{C}$ to 85°C . Typical values are given $V_{IN} = 3.0\text{ V}$ and $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)N}$	N-Channel Boost Switch $R_{DS(ON)}$	$V_{IN}=3.5\text{ V}$, $V_{OUT}=3.5\text{ V}$		85	120	m Ω
$R_{DS(ON)P}$	P-Channel Sync Rectifier $R_{DS(ON)}$	$V_{IN}=3.5\text{ V}$, $V_{OUT}=3.5\text{ V}$		65	85	m Ω
$R_{DS(ON)P_BYP}$	P-Channel Bypass Switch $R_{DS(ON)}$	$V_{IN}=3.5\text{ V}$, $V_{OUT}=3.5\text{ V}$		65	85	m Ω
T_{120A}	T120 Activation Threshold			120		$^\circ\text{C}$
T_{120R}	T120 Release Threshold			100		$^\circ\text{C}$
T_{150T}	T150 Threshold			150		$^\circ\text{C}$
T_{150H}	T150 Hysteresis			20		$^\circ\text{C}$
t_{RST}	FAULT Restart Timer			20		ms

Typical Characteristics

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, and $V_{OUT} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1.

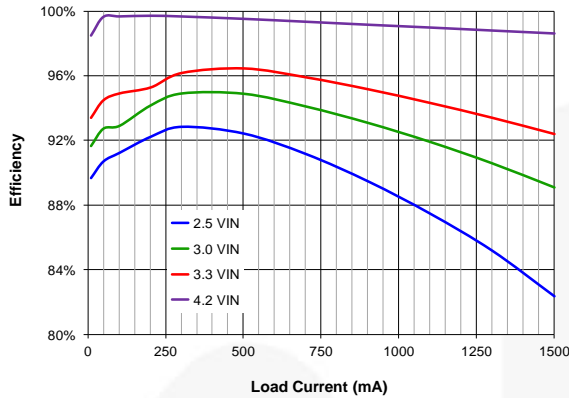


Figure 5. Efficiency vs. Load Current and Input Voltage, $V_{OUT}=3.5\text{ V}$

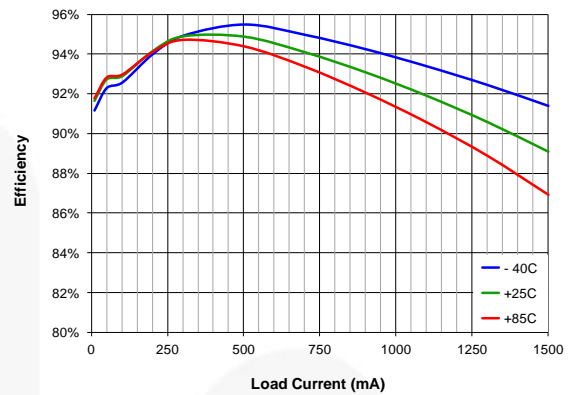


Figure 6. Efficiency vs. Load Current and Temperature, $V_{IN}=3.0\text{ V}$, $V_{OUT}=3.5\text{ V}$

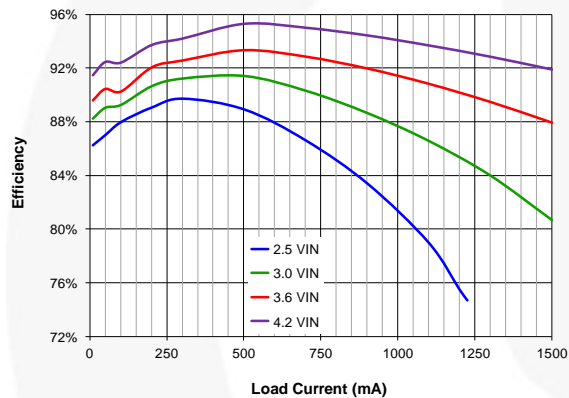


Figure 7. Efficiency vs. Load Current and Input Voltage

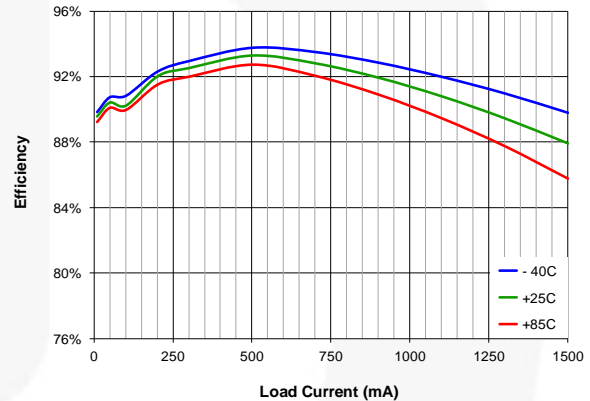


Figure 8. Efficiency vs. Load Current and Temperature

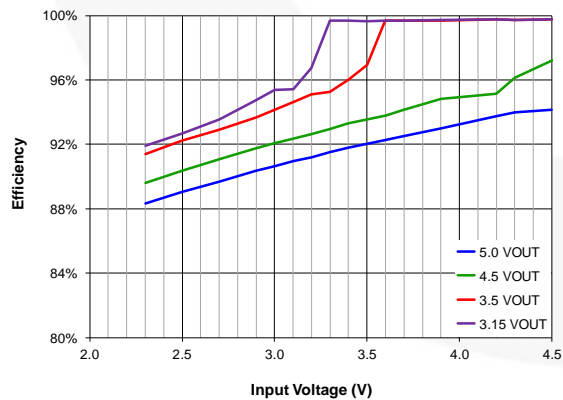


Figure 9. Efficiency vs. Input Voltage and Output Voltage, 200 mA Load

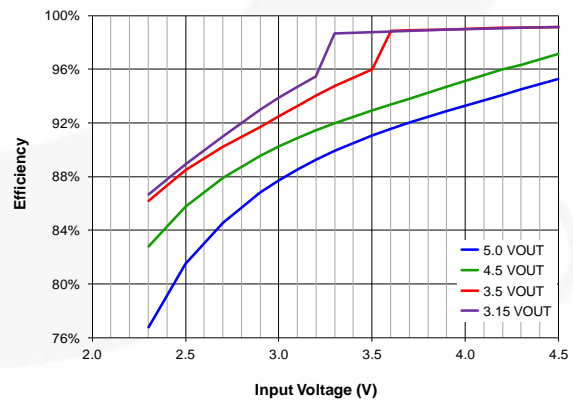


Figure 10. Efficiency vs. Input Voltage and Output Voltage, 1000 mA Load

Typical Characteristics (Continued)

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1.

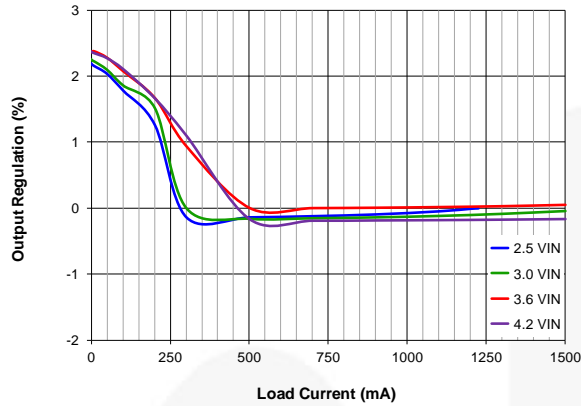


Figure 11. Output Regulation vs. Load Current and Input Voltage (Normalized to 3.6 V_{IN} , 500 mA Load)

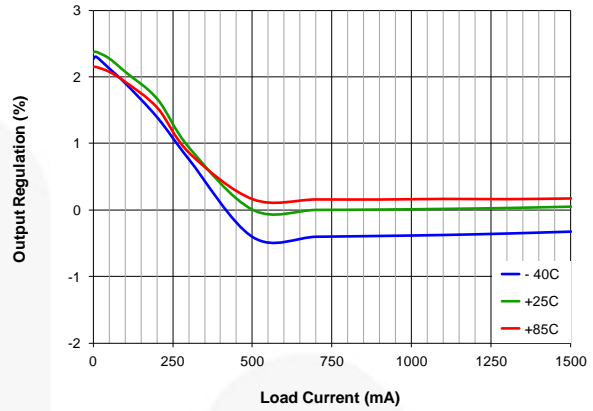


Figure 12. Output Regulation vs. Load Current and Temperature (Normalized to 3.6 V_{IN} , 500 mA Load, $T_A=25^\circ\text{C}$)

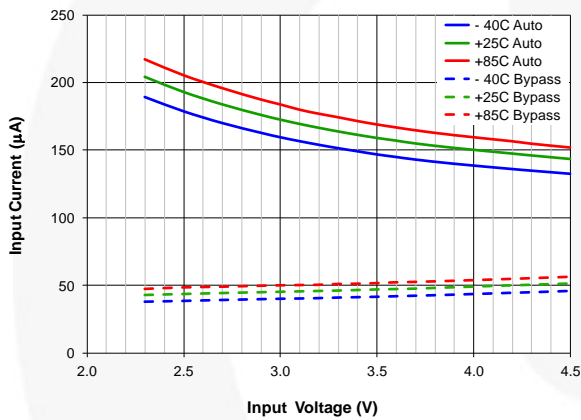


Figure 13. Quiescent Current vs. Input Voltage, Temperature and Mode, $V_{OUT}=5.0\text{ V}$, Forced Bypass, OCP Active

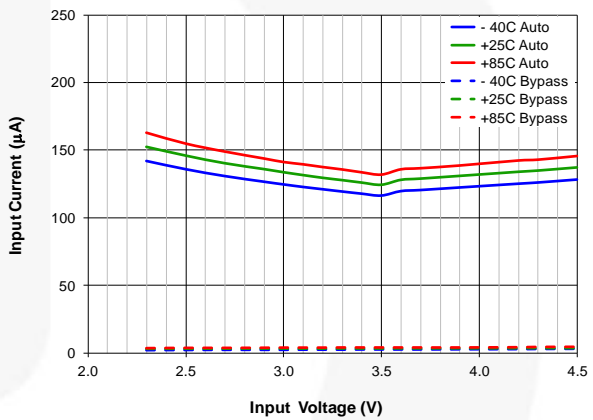


Figure 14. Quiescent Current vs. Input Voltage, Temperature and Mode, $V_{OUT}=3.5\text{ V}$, Forced Bypass, Low I_Q

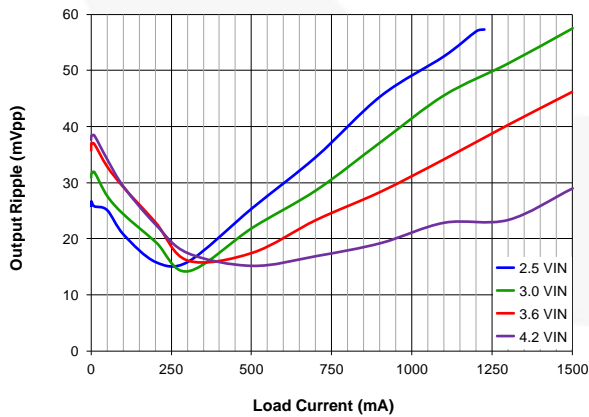


Figure 15. Output Ripple vs. Load Current and Input Voltage

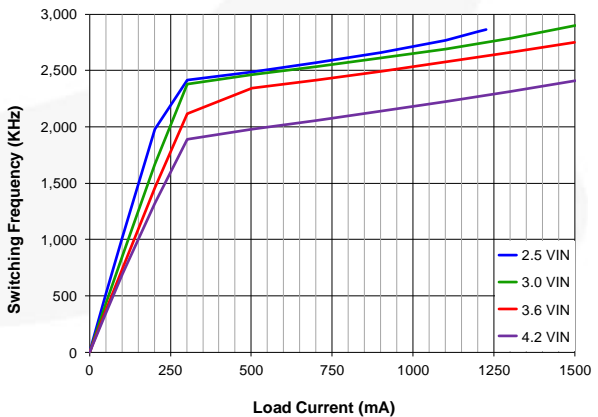
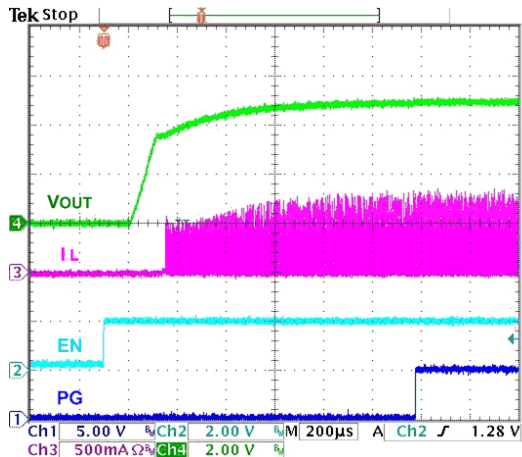


Figure 16. Frequency vs. Load Current and Input Voltage

Typical Characteristics (Continued)

Unless otherwise specified, $V_{IN} = 3.6\text{ V}$; $V_{OUT} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1.



■ Figure 17. Startup, 50 Ω Load

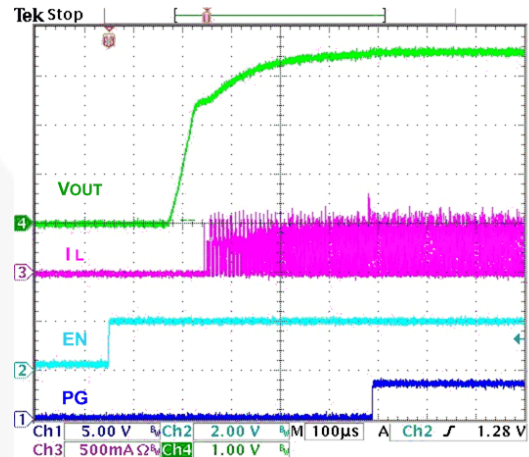


Figure 18. Startup, 50 Ω Load, $V_{IN}=2.5\text{ V}$, $V_{OUT}=3.5\text{ V}$

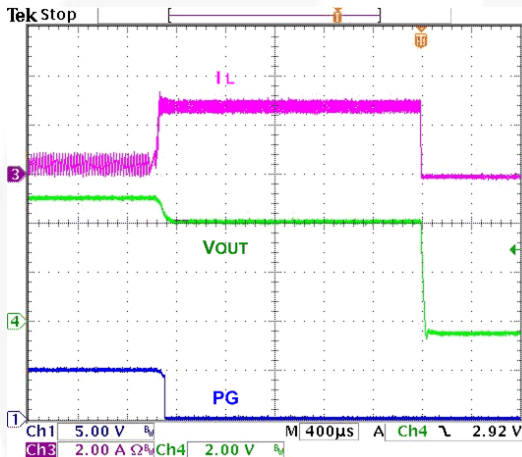


Figure 19. Overload Protection

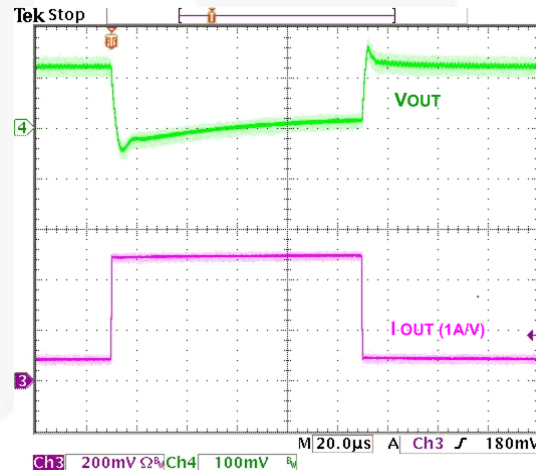


Figure 20. Load Transient, 100-500 mA, 100 ns Edge

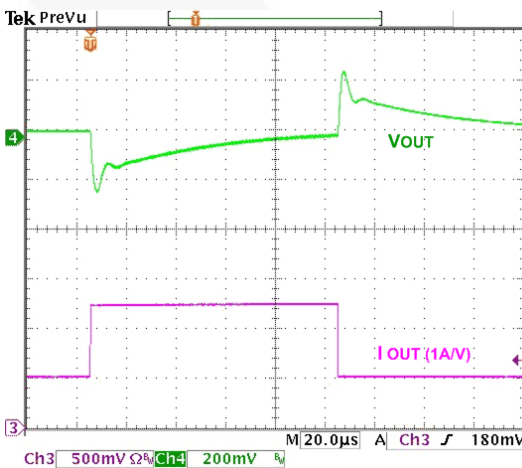


Figure 21. Load Transient, 500-1250 mA, 100 ns Edge

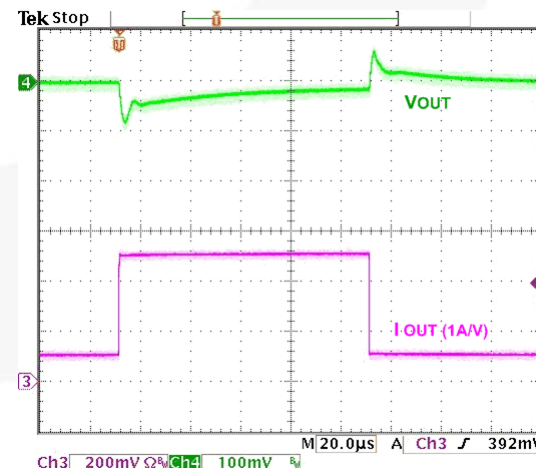


Figure 22. Load Transient, 100-500 mA, 100 ns Edge, $V_{IN}=3\text{ V}$, $V_{OUT}=3.5\text{ V}$

Typical Characteristics (Continued)

Unless otherwise specified, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 5\text{ V}$, $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1.

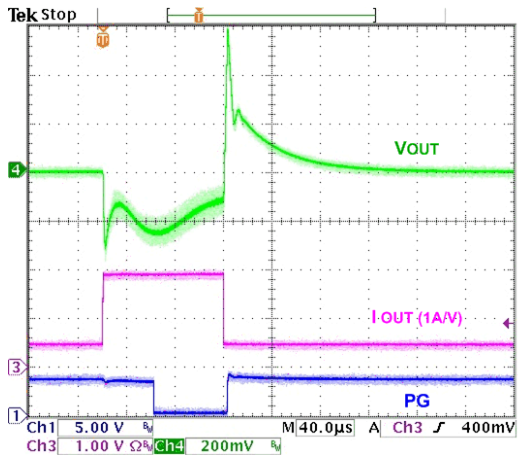


Figure 23. Transient Overload, 500-1950 mA, 100 ns Edge, $V_{IN}=3\text{ V}$, $V_{OUT}=3.5\text{ V}$

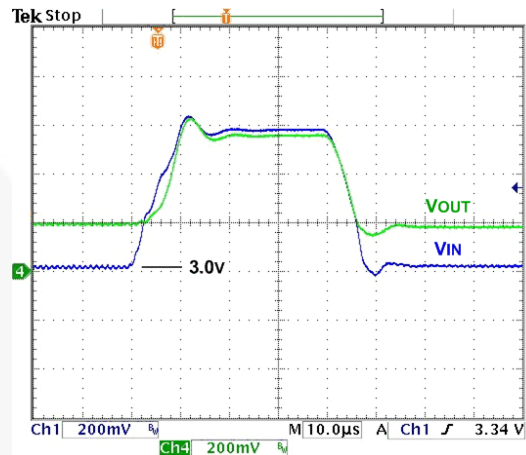


Figure 24. Line Transient, 3.0-3.6 V_{IN} , 10 μs Edge, 500 mA Load, $V_{OUT}=3.15\text{ V}$

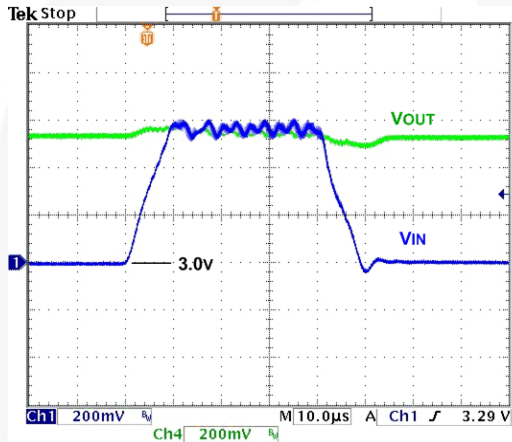


Figure 25. Line Transient, 3.0-3.6 V_{IN} , 10 μs Edge, 1,000 mA Load, $V_{OUT}=3.5\text{ V}$

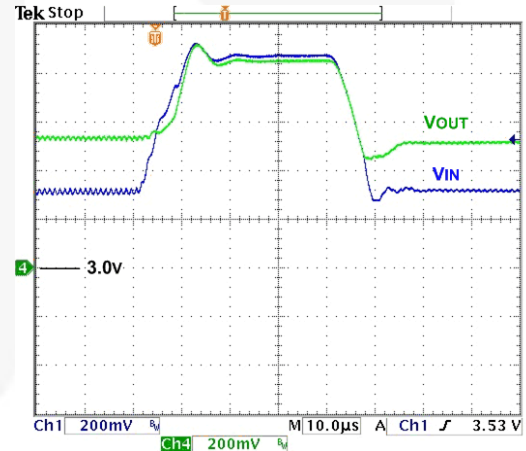


Figure 26. Line Transient, 3.3-3.9 V_{IN} , 10 μs Edge, 500 mA load, $V_{OUT}=3.5\text{ V}$

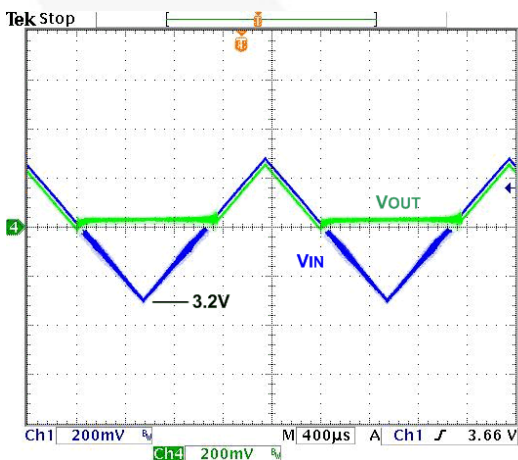


Figure 27. Bypass Entry / Exit, Slow V_{IN} Ramp 1 ms Edge, 500 mA Load, $V_{OUT}=3.5\text{ V}$, 3.2 - 3.8 V_{IN}

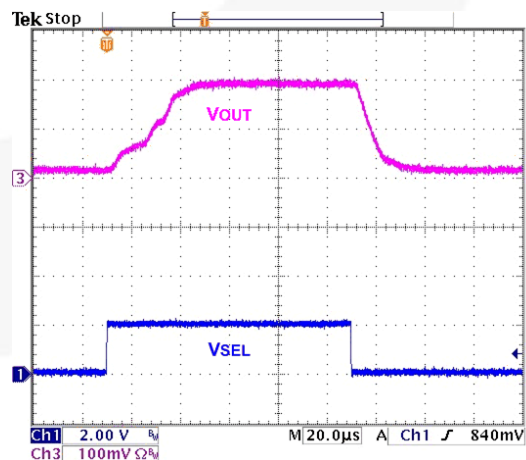


Figure 28. V_{SEL} Step, $V_{IN}=3\text{ V}$, $V_{OUT}=3.5\text{ V}$, 500 mA Load

Circuit Description

FAN48630 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltages. The regulator includes a Bypass Mode that activates when V_{IN} is above the boost regulator's setpoint.

In anticipation of a heavy load transition, the setpoint can be adjusted upward by fixed amounts with the VSEL pin to reduce the required system headroom during lighter-load operation to save power.

Table 2. Operating States

Mode	Description	Invoked When
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{OUT} < V_{OUT(MIN)}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT(MIN)}$
BPS	True Bypass Mode	$V_{IN} > V_{OUT(MIN)}$

Boost Mode

The FAN48630 uses a current-mode modulator to achieve excellent transient response and smooth transitions between CCM and Discontinuous Conduction Mode (DCM) operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In light-load operation (DCM), frequency is reduced to maintain high efficiency.

Table 3. Boost Startup Sequence

Start State	Entry	Exit	End State	Timeout (μs)
LIN1	$V_{IN} > UVLO$, EN=1	$V_{OUT} > V_{IN} - 300$ mV	SS	
			LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT(MIN)}$	BST	
		OVERLOAD TIMEOUT	FAULT	64

Shutdown and Startup

If EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from V_{IN} to V_{OUT} , as well as reverse flow from V_{OUT} to V_{IN} . During startup, it is recommended to keep DC current draw below 500 mA.

LIN State

When EN is HIGH and $V_{IN} > UVLO$, the regulator attempts to bring V_{OUT} within 300 mV of V_{IN} using the internal fixed current source from V_{IN} (Q3). The current is limited to LIN1 set point.

If V_{OUT} reaches $V_{IN} - 300$ mV during LIN1 Mode, the SS state is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 2A. If V_{OUT} fails to reach $V_{IN} - 300$ mV after 1024 μs, a fault condition is declared.

SS State

Upon the successful completion of the LIN state ($V_{OUT} \geq V_{IN} - 300$ mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS state, V_{OUT} is ramped up by stepping the internal reference. If V_{OUT} fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault condition is declared. If large C_{OUT} is used, the reference is automatically stepped slower to avoid excessive input current draw.

BST State

This is a normal operating state of the regulator.

BPS State

If V_{IN} is above V_{REG} when the SS Mode successfully completes, the device transitions directly to BPS Mode.

FAST and SLOW Soft-Start Options

FAN48630UC315X, FAN48630UC33X, FAN48630UC35X, and FAN48630UC37AX feature fast startup with EN to regulation time of 600 μs. LIN1 and LIN2 phase currents are doubled compared to SLOW options, SS phase is also faster.

FAN48630UC45X and FAN48630UC50X feature slow startup with EN to regulation time of 1300 μs to reduce inrush current.

FAULT State

The regulator enters the FAULT state under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN state to SS state.
- V_{OUT} fails to achieve the voltage required to advance from SS state to BST state.
- Boost current limit triggers for 2 ms during the BST state.
- V_{DS} protection threshold is exceeded during BPS state.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between V_{IN} and V_{OUT} . After waiting 20 ms, a restart is attempted.

Power Good

Power good is 0 FAULT, 1 POWER GOOD, open-drain output.

The Power good pin is provided for signaling the system when the regulator has successfully completed soft-start and no faults have occurred. Power good also functions as an early warning flag for high die temperature and overload conditions.

- PG is released HIGH when the soft-start sequence is successfully completed.
- PG is pulled LOW when PMOS current limit has triggered for 64 μs OR the die the temperature exceeds 120°C. PG is re-asserted when the device cools below to 100°C.
- Any FAULT condition causes PG to be de-asserted.

Over-Temperature

The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Bypass Operation

In normal operation, the device automatically transitions from Boost Mode to Bypass Mode, if V_{IN} goes above target V_{OUT} . In Bypass Mode, the device fully enhances both Q1 and Q3 to provide a very low impedance path from V_{IN} to V_{OUT} . Entry to the Bypass Mode is triggered by condition where $V_{IN} > V_{OUT}$ and no switching has occurred during past 5 μ s. To soften the entry to Bypass Mode, Q3 is driven as a linear current source for the first 5 μ s. Bypass Mode exit is triggered when V_{OUT} reaches the target V_{OUT} voltage. During Automatic Bypass Mode, the device is short-circuit protected by voltage comparator tracking the voltage drop from V_{IN} to V_{OUT} ; if the drop exceeds 200 mV, FAULT is declared.

With sufficient load to enforce CCM operation, the Bypass Mode to Boost Mode transition occurs at the target V_{OUT} . The corresponding input voltage at the transition point is:

$$V_{IN} \leq V_{OUT} + I_{LOAD} \bullet (DCR_L + R_{DS(ON)P}) \parallel R_{DS(ON)BYP} \text{ EQ. 1}$$

The Bypass Mode entry threshold has 25 mV hysteresis imposed at V_{OUT} to prevent cycling between modes. The transition from Boost Mode to Bypass Mode occurs at the target $V_{OUT} + 25$ mV. The corresponding input voltage is:

$$V_{IN} \geq V_{OUT} + 25mV + I_{LOAD} \bullet (DCR_L + R_{DS(ON)P}) \text{ EQ. 2}$$

Forced Bypass

Entry to Forced Bypass Mode initiates with a current limit on Q3 and then proceeds to a true bypass state. To prevent reverse current to the battery, the device waits until output discharges below V_{IN} before entering Forced Bypass Mode.

Low-IQ Forced Bypass Mode is available for FAN48630UC315X, FAN48630UC33X, FAN48630UC35X, and FAN48630UC37AX. After the transition is complete, most of the internal circuitry is disabled to minimize quiescent current draw. Short-circuit, UVLO, output OVP and over-temperature protections are inactive in Forced Bypass Mode.

OCP in Forced Bypass Mode is available for FAN48630UC45X and FAN48630UC50X. During Forced Bypass Mode, the device is short-circuit protected by a voltage comparator tracking the voltage drop from V_{IN} to V_{OUT} . If the drop exceeds 200 mV, a FAULT is declared. The over-temperature protection is also active.

In Forced Bypass Mode, V_{OUT} can follow V_{IN} below $V_{OUT(MIN)}$.

VSEL

V_{SEL} can be asserted in anticipation of a positive load transient. Raising V_{SEL} increases $V_{OUT(MIN)}$ by a fixed amount and V_{OUT} is stepped to the corresponding target output voltage in 20 μ s. The functionality can also be utilized to mitigate undershoot during severe line transients, while minimizing V_{OUT} during more benign operating conditions to save power.

EN

Setting the EN pin voltage below 0.4 V disables the part. Placing the voltage above 1.2 V enables the part. Do not connect the EN pin to V_{IN} . A logic voltage of 1.8 V should control the EN pin and enable / disable the device. The EN pin should be pulled HIGH after the V_{IN} voltage has reached a minimum voltage of 2.3 V.

Application Information

Output Capacitance (C_{OUT})

Stability

The effective capacitance (C_{EFF}) of small, high-value, ceramic capacitors decreases as bias voltage increases.

FAN48630 is guaranteed for stable operation with the minimum value of C_{EFF} (C_{EFF(MIN)}) outlined in Table 4 below.

Table 4. Minimum C_{EFF} Required for Stability

Operating Conditions		C _{EFF(MIN)} (μF)
V _{OUT} (V)	I _{LOAD} (mA)	
3.15	0 to 1500	12
3.5	0 to 1500	9
4.5 and 5	0 to 1500	6

C_{EFF} varies with manufacturer, material, and case size.

Inductor Selection

Recommended nominal inductance value is 0.47 μH.

FAN48630 employs valley-current limiting; peak inductor current can reach 3.8 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading as only valley of the inductor current ripple is controlled.

For FAN48630UC315X and FAN48630UC33X, a 0.33 μH inductor can be used for improved transient performance.

Startup

Input current limiting is in effect during soft-start, which limits the current available to charge C_{OUT} and any additional capacitance on the V_{OUT} line. If the output fails to achieve regulation within the limits described in the Startup section, a FAULT occurs, causing the circuit to shut down then restart after a significant time period. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high-current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempts soft-start, only to have the output capacitance discharged by the load when in a FAULT state.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}. Output ripple is calculated as:

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{EQ. 3}$$

and

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{EQ. 4}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{EQ. 5}$$

and

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{EQ. 6}$$

As can be seen from EQ. 5, the maximum V_{RIPPLE} OCCURS when V_{IN} is at minimum and I_{LOAD} is at maximum.

Layout Recommendations

The layout recommendations below highlight various top-copper pours using different colors.

To minimize spikes at V_{OUT}, C_{OUT} must be placed as close as possible to PGND and V_{OUT}, as shown in Figure 29.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

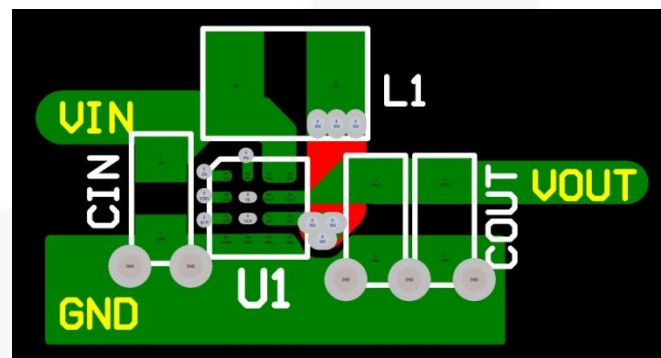


Figure 29. Layout Recommendation

Physical Dimensions

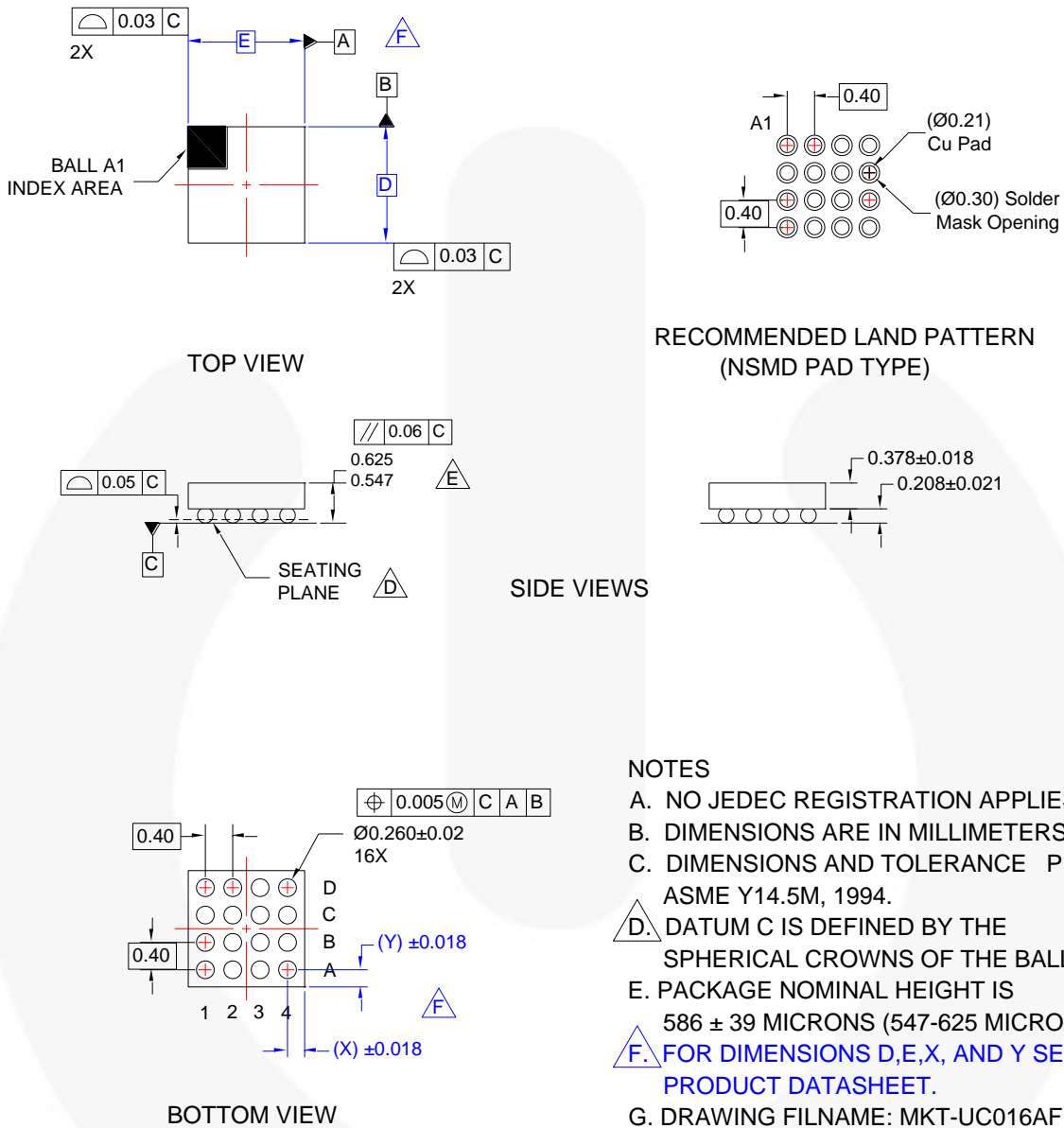


Figure 30. 16-Ball, 4x4 Array, 0.4 mm Pitch, 250 µm Ball, Wafer-Level Chip-Scale Package (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FAN48630UCxxxX	1.780 ± 0.030	1.780 ± 0.030	0.290	0.290
FAN48630BUC315X	1.780 ± 0.030	1.780 ± 0.030	0.290	0.290






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