AL460A HD-FIFO Evaluation Board

Fulfill your FIFO potential!

High-Speed First-In-First-Out memory buffer for HD Video applications

Introduction

This EVB board is designed for evaluating the AL460A HD-FIFO integrated chip. It has two embedded AL460A-7(-13)-PBF chips operating in parallel, expanding the bus width to 32-bits. Control signals and data bus signals are available on two 50-pin connectors; one connector is reserved for write controls and the input data bus; the other one is for read controls and the output data bus. A separate socket board is available to the user for connecting the module directly to an Altera Cyclone III FPGA board for any necessary solution verification/validation.

The AL460A is designed with a straightforward bus interface, reducing implementation and debugging efforts, and helping customers develop faster and more efficiently. This board is especially designed and optimized to be easily integrated as an add-on module on existing systems, significantly reducing interface engineering issues commonly found in retrofit efforts. This allows designers the luxury of being able to focus on core functionality and product quality.

Applications

- ❑ HD video capturing and editing systems
- ❑ Switcher or format converter box
- ❑ Scan rate converters
- ❑ Time base correction (TBC)
- ❑ Frame synchronizer
- ❑ HD digital video camera buffering
- ❑ Up to 1080p video stream data

AL460A HD-FIFO Advantages

HD-FIFO is a proprietary design technology used to overcome issues commonly hindering and limiting other frame buffer devices (e.g. SDRAM, DDR…etc) found in FPGA solutions. Traditional FPGA implementations require higher I/O pin totals and place heavy demands on logic resources and property memory controllers, forcing a designer to move up to higher grade FPGAs. In contrast, AverLogic's HD-FIFO requires significantly less in I/O pins and logic resources, at the same time overcoming latency issues therein. The programmable I/O controls and double buffer mode increase design flexibility and reduce FPGA overhead.

Evaluation Board Specifications

The AL460 Evaluation Board is RoHS compliant.

- **AL460 EVB specs**
  - AL460A-7(-13)-PBF (x2)
  - Dimensions: 80 mm x 80 mm
  - Configuration
    Parallel AL460A chips provide a 32-bit I/O bus
  - Power and analog device
    3.3V input from existing system or external power supply
    2.5V Ultra low dropout linear regulator LP3852
  - Clocking
    14.31818 MHz on-board Crystal
  - Connectors
    Low profile 25x2 2.0 mm male header (x2)
- **AL460 FPGA Socket Board (*Available upon request)**
  - Dimensions: 80 mm x 80 mm
  - Connectors
    Low profile 25x2 2.0 mm female header (x2)
    HSMC

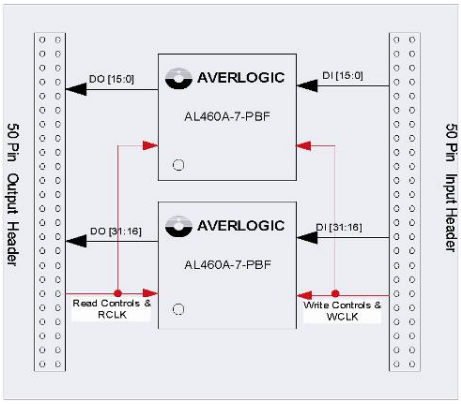
AL460A HD-FIFO EVB Flyer

General Features

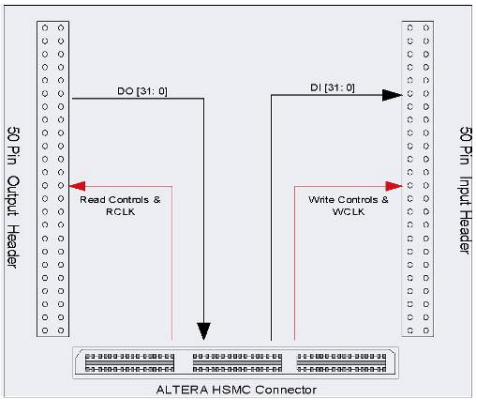
- 256 Mbit density, 8M x 32-bit FIFO memory
- Maximum 150 MHz, 32-bit synchronous sequential read/write operations
- Maximum 4.8 Gbps throughput
- 3.3V power supply
- Programmable I/O control
- Supports double buffer mode (4M x32-bit upper and lower frames access)
- Selectable Polarity control

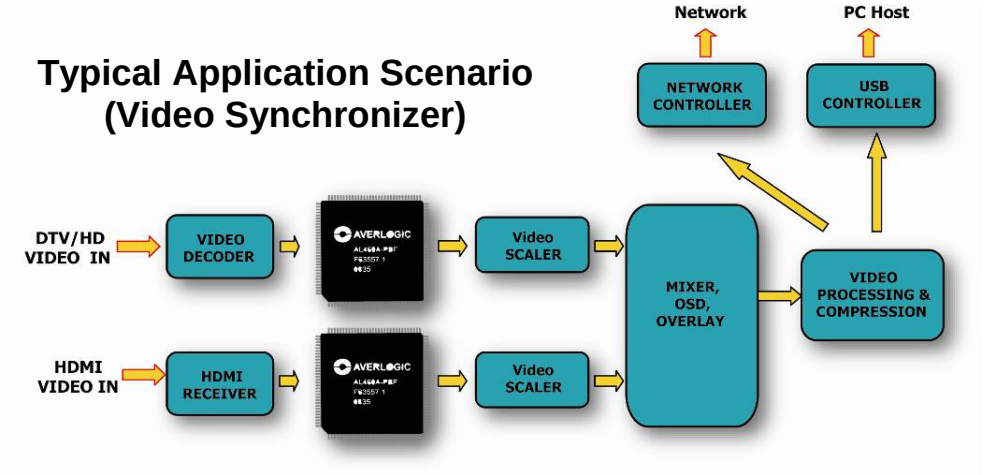
Block Diagrams

AL460 EVB Block Diagram



AL460 FPGA Socket Board Block Diagram





Ordering Information

Part number	Speed	Data Bus	Power
AL460A-7-EVB-A0	150 MHz	32-bit	+3.3V
AL460A-13-EVB-A0	75 MHz	32-bit	+3.3V
BB-AL460FSB1-EVB-D0*	N/A	N/A	N/A