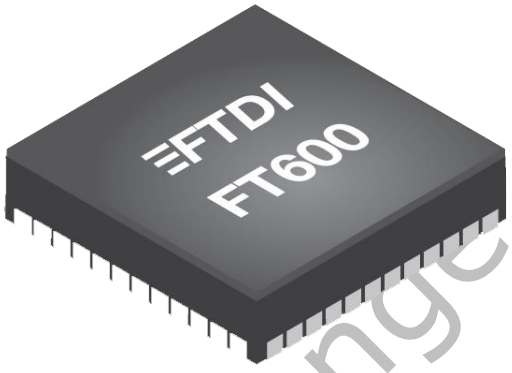
Future Technology Devices International Ltd.

FT600/FT601

(USB 3.0 to FIFO Bridge)



The FT600/FT601 is a USB 3.0 to FIFO interface bridge chip with the following advanced features:

- Supports USB 3.0 Super Speed (5Gbps)/USB 2.0 High Speed (480Mbps)/USB 2.0 Full Speed (12Mbps) transfer.
- Supported USB Transfer Type: Control/Bulk/Interrupt
- Up to 8 configurable endpoints (PIPEs).
- Supports 2 parallel slave FIFO bus protocols, data bursting rate is up to 400MB/s.
- Supports 4 IN channels and 4 OUT channels on FIFO bus connectivity.
- Built-in 16kB FIFO data buffer RAM.
- Supports Remote Wakeup capability.
- Supports multi voltage I/O: 1.8V, 2.5V and 3.3V.
- Configurable GPIO support.
- Internal LDO 1.0V regulator.
- Integrated power-on-reset circuit.
- User programmable USB descriptors.
- Supports Battery Charging spec. BC1.2.
- Available as FT600-16bit/FT601-32bit FIFO interface.
- Industrial operating temperature range: -40 to 85ºC.
- Available in compact Pb-free QFN-76(32bit) and QFN-56(16bit) packages (both RoHS compliant).

1 Typical Applications

- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing PLD/FPGA based designs to USB 3.0
- USB 3.0 Digital Video Camera Interface
- USB 3.0 Digital Camera
- USB 3.0 Interface for Printer/Scanner
- Medical/Industrial imaging devices
- USB 3.0 Instrumentation

1.1 Driver Support

Royalty free D3XX *Direct* Drivers
(USB Drivers + DLL S/W Interface)

- Windows 8
- Mac OS-X
- Linux

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details. For driver installation, please refer to the application note AN232B-10.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT600Q	56 Pin QFN 0.4mm Pitch
FT601Q	76 Pin QFN 0.4mm Pitch

1.3 USB Compliant

At the time of writing this datasheet, USB compliance testing is still pending for the FT600Q/FT601Q.

2 Block Diagram

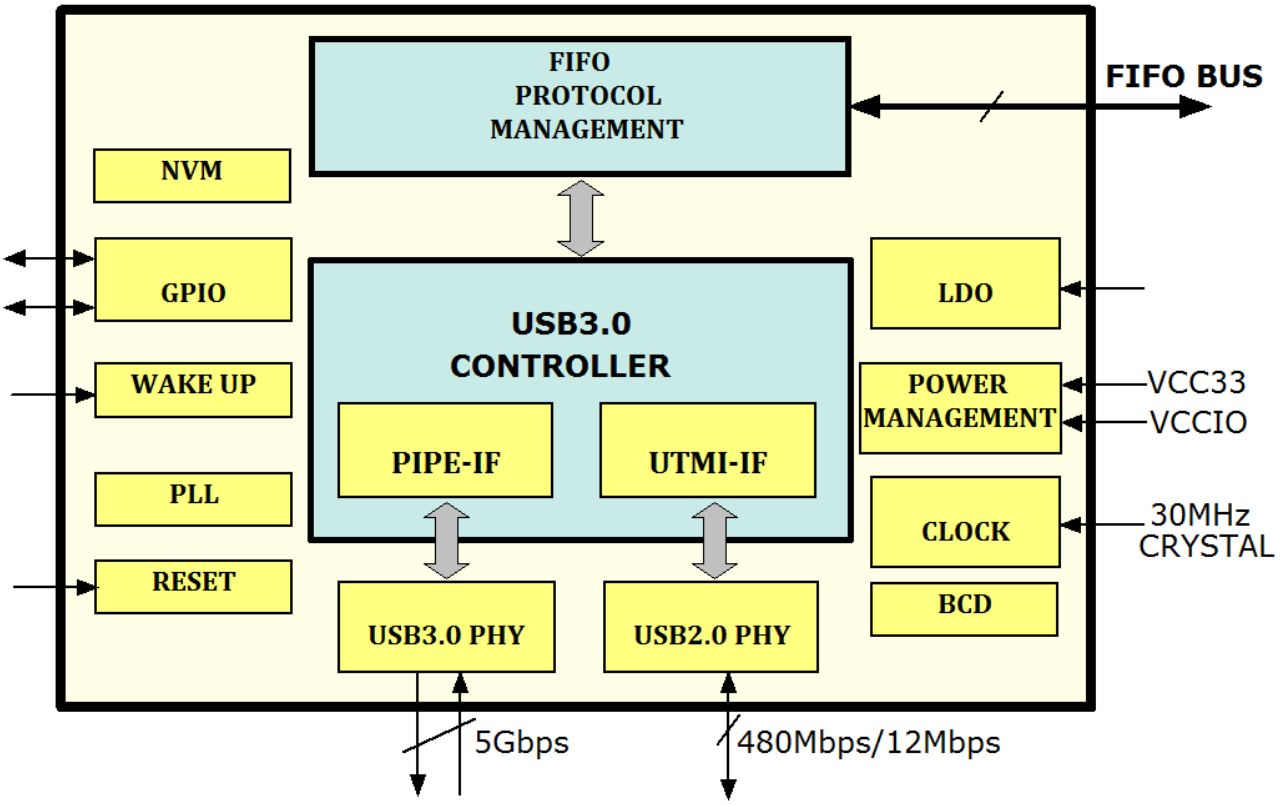


Figure 2.1 Block Diagram

Notes: FT600Q(QFN-56) has a 16-bit FIFO bus interface and FT601Q(QFN-76) has a 32-bit FIFO bus interface.

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 Device Pin Out

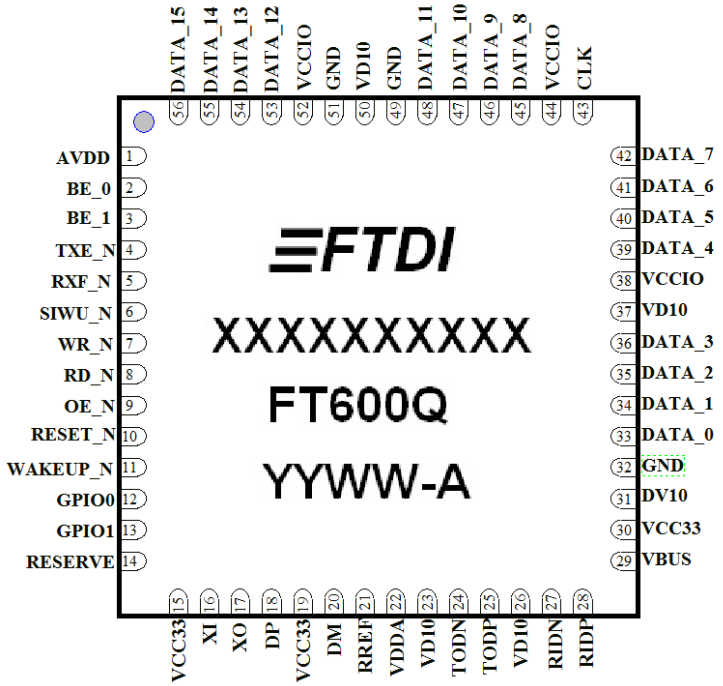


Figure 3.1 QFN56 Package Pin Out

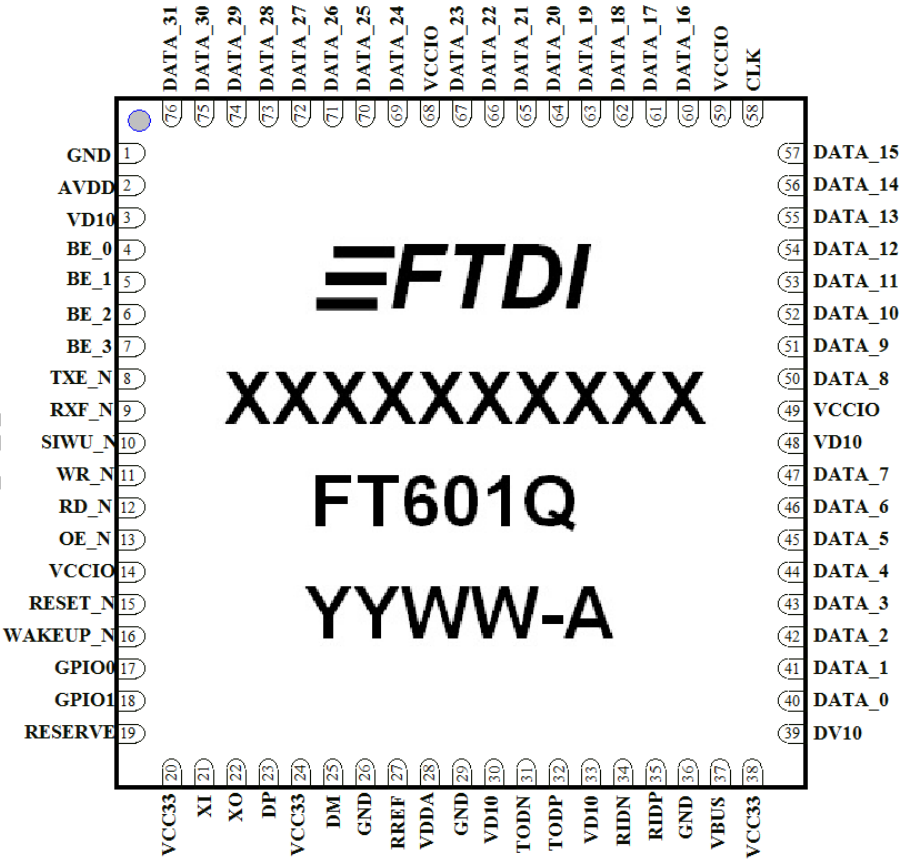


Figure 3.2 QFN76 Package Pin Out

3.2 Device Pin Out Signal Description

Pin Name	Description	Type	Pin No.	
			QFN76	QFN56
CLK	Parallel FIFO bus clock output pin to FIFO bus master, the Frequency can configure as 66Mhz or 100Mhz at both FIFO bus modes.	O	58	43
DATA_0	Parallel FIFO bus data I/O bit 0.	I/O	40	33
DATA_1	Parallel FIFO bus data I/O bit 1.	I/O	41	34
DATA_2	Parallel FIFO bus data I/O bit 2.	I/O	42	35
DATA_3	Parallel FIFO bus data I/O bit 3.	I/O	43	36
DATA_4	Parallel FIFO bus data I/O bit 4.	I/O	44	39
DATA_5	Parallel FIFO bus data I/O bit 5.	I/O	45	40
DATA_6	Parallel FIFO bus data I/O bit 6.	I/O	46	41
DATA_7	Parallel FIFO bus data I/O bit 7.	I/O	47	42
DATA_8	Parallel FIFO bus data I/O bit 8.	I/O	50	45
DATA_9	Parallel FIFO bus data I/O bit 9.	I/O	51	46
DATA_10	Parallel FIFO bus data I/O bit 10.	I/O	52	47
DATA_11	Parallel FIFO bus data I/O bit 11.	I/O	53	48
DATA_12	Parallel FIFO bus data I/O bit 12.	I/O	54	53
DATA_13	Parallel FIFO bus data I/O bit 13.	I/O	55	54
DATA_14	Parallel FIFO bus data I/O bit 14.	I/O	56	55
DATA_15	Parallel FIFO bus data I/O bit 15.	I/O	57	56
DATA_16	Parallel FIFO bus data I/O bit 16.	I/O	60	N/A
DATA_17	Parallel FIFO bus data I/O bit 17.	I/O	61	N/A
DATA_18	Parallel FIFO bus data I/O bit 18.	I/O	62	N/A
DATA_19	Parallel FIFO bus data I/O bit 19.	I/O	63	N/A
DATA_20	Parallel FIFO bus data I/O bit 20.	I/O	64	N/A
DATA_21	Parallel FIFO bus data I/O bit 21.	I/O	65	N/A
DATA_22	Parallel FIFO bus data I/O bit 22.	I/O	66	N/A
DATA_23	Parallel FIFO bus data I/O bit 23.	I/O	67	N/A
DATA_24	Parallel FIFO bus data I/O bit 24.	I/O	69	N/A

DATA_25	Parallel FIFO bus data I/O bit 25.	I/O	70	N/A
DATA_26	Parallel FIFO bus data I/O bit 26.	I/O	71	N/A
DATA_27	Parallel FIFO bus data I/O bit 27.	I/O	72	N/A
DATA_28	Parallel FIFO bus data I/O bit 28.	I/O	73	N/A
DATA_29	Parallel FIFO bus data I/O bit 29.	I/O	74	N/A
DATA_30	Parallel FIFO bus data I/O bit 30.	I/O	75	N/A
DATA_31	Parallel FIFO bus data I/O bit 31.	I/O	76	N/A
BE_0	Parallel FIFO bus byte enable I/O bit 0.	I/O	4	2
BE_1	Parallel FIFO bus byte enable I/O bit 1.	I/O	5	3
BE_2	Parallel FIFO bus byte enable I/O bit 2.	I/O	6	N/A
BE_3	Parallel FIFO bus byte enable I/O bit 3.	I/O	7	N/A
TXE_N	245 Synchronous FIFO mode: Transmit FIFO Empty output signal. Multi-Channel FIFO mode: Status Valid output signal (optional).	O	8	4
RXF_N	245 Synchronous FIFO mode: Receive FIFO Full output signal. Multi-Channel FIFO mode: Data Receive Acknowledge output signal.	O	9	5
SIWU_N	245 Synchronous FIFO mode: Send Immediate/Wake Up input signal.	I	10	6
WR_N	245 Synchronous FIFO mode: Write Enable input signal. Multi-Channel FIFO mode: Data Transaction Request input signal.	I	11	7
RD_N	245 Synchronous FIFO mode: Read Enable input signal.	I	12	8
OE_N	245 Synchronous FIFO mode: Data Output Enable input signal.	O	13	9
RESET_N	Chip Reset input, Active low.	I	15	10
WAKEUP_N	Suspend/Remote Wakeup pin. Active low.	I	16	11
Reserved	Do not connect.	I/O	19	14
GPIO0	Configurable GPIO port0.	I/O	17	12
GPIO1	Configurable GPIO port1.	I/O	18	13
VBUS	USB BUS power input.	I	37	29
XI	Crystal input. This terminal is the crystal input for the internal oscillator.	I	21	16

XO	Crystal Output. This terminal is the crystal output for the internal oscillator.	O	22	17
DP	High-speed USB differential transceiver (positive)	I/O	23	18
DM	High-speed USB differential transceiver (negative)	I/O	25	20
RREF	PHY reference resistor input pin. Connect 1.6K Ω 1% resistor to ground, provides reference voltage to USB2 PHY.	I	27	21
TODN	Super Speed USB transmitter differential pair (negative)☐	O	31	24
TODP	Super Speed USB transmitter differential pair (positive)☐	O	32	25
RIDN	Super Speed USB receiver differential pair (negative)	I	34	27
RIDP	Super Speed USB receiver differential pair (positive)	I	35	28
VCC33	+3.3V power input for chip and internal LDO.	PWR	20,24, 38	15,19, 30
DV10	+1.0V power output from internal LDO. Connecting to VD10 and AVDD, with a 4.7uF cap to ground is recommended.	O	39	31
VD10	+1.0V core voltage input.	PWR	3,30,3 3,48	23,26, 37,50
VCCIO	Power input for I/O block, supports +1.8/+2.5/+3.3V.	PWR	14,49, 59,68	38,44, 52
VDDA	+3.3V power input for USB2.0 and USB3.0 PHYs.	PWR	28	22
AVDD	+1.0V power input for PLL.	PWR	2	1
GND	Ground	GND	1,26, 29,36	1,32, 49,51

Table 3.1 Device pin out Signal descriptions

3.3 Multi-Channel FIFO mode Protocols

This is a Slave bus and is designed to handle multi-channel connectivity. The bus protocol supports a total of 8 channels (4 INs and 4 OUTs). CLK is the clock output from the bus slave to the bus master.

WR_N is the bus master to bus slave data transaction request signal, and it is active low.

RXF_N is the bus slave to bus master data receive acknowledge signal, and it is active low.

TXE_N (optional signal) is the bus slave to bus master FIFO status valid signal, and it is low active.

DATA[31:0] is used as the 32-bit data bus during the data transfer phase. When the bus is in the idle state DATA[31:16], DATA[7:0] and BE[3:0] are driven to logic"1" by the bus master, and DATA[15:8] is driven by the bus slave to provide the FIFO status to the bus master. The upper nibble (DATA[15:12]) provides the 4 OUT channels FIFO status while the lower nibble (DATA[11:8]) provides the 4 IN channels FIFO status. They are all active low.

For example, at idle, DATA[12] is logic"0" and DATA[8] is logic"0", which indicates OUT channel 1 FIFO data is available to send and IN channel 1 FIFO space is empty to receive data respectively. The external bus master will start a transfer cycle by asserting WR_N based on the channel FIFO status. The first cycle after WR_N is asserted is the command phase, followed by the data phase when RXF_N is asserted. At the command phase, the bus master will send the channel number which it intends to transfer data with on DATA[7:0] and the Read/Write command on BE[3:0]. BE[3:0] = 'h0 and BE[3:0] = 'h1 indicate a master read or write respectively. There may also be required a turn-a-round for DATA[31:0] and BE[3:0] after the command phase and at the end of data transaction.

Table 3.2 shows Multi-Channel FIFO mode command phase master read/write and channel address setting.

Command Phase	FT600 Command BE[1:0]	FT601 Command BE[3:0]	Channel Address DATA[7:0]
Master Read	00	0000	8'h1=Channel 1 8'h2=Channel 2 8'h3=Channel 3 8'h4=Channel 4
Master Write	01	0001	

Table 3.2 Multi-Channel FIFO mode Command phase

The waveform below shows a master read transaction with FIFO data exhausted first. There are turn-a-round cycles for DATA[7:0], DATA[31:16] and BE[3:0] after command phase and at the end of the data transaction.

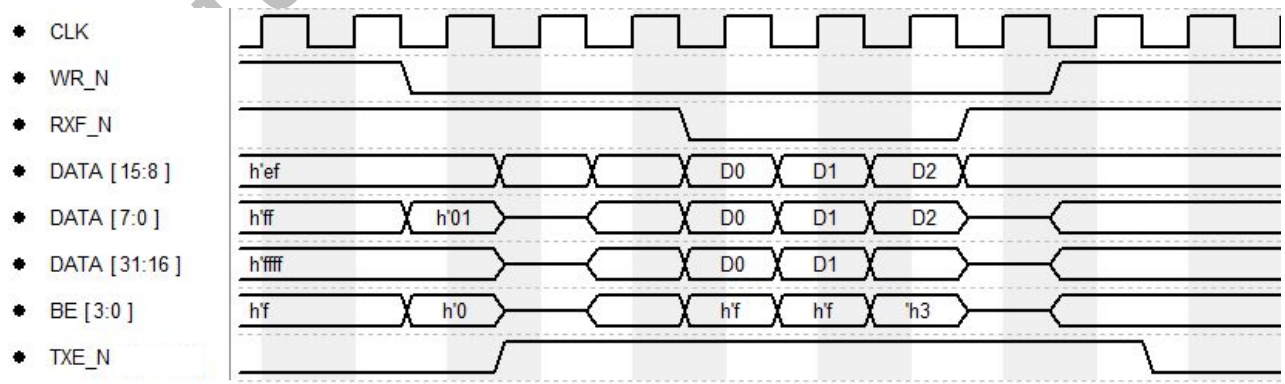


Figure 3.3 Multi-Channel FIFO mode master read transaction 1

The waveform below shows a master read transaction where the bus master terminates the transaction. There are turn-a-round cycles for DATA[7:0], DATA[31:16] and BE[3:0] after the command phase and at the end of the data transaction.

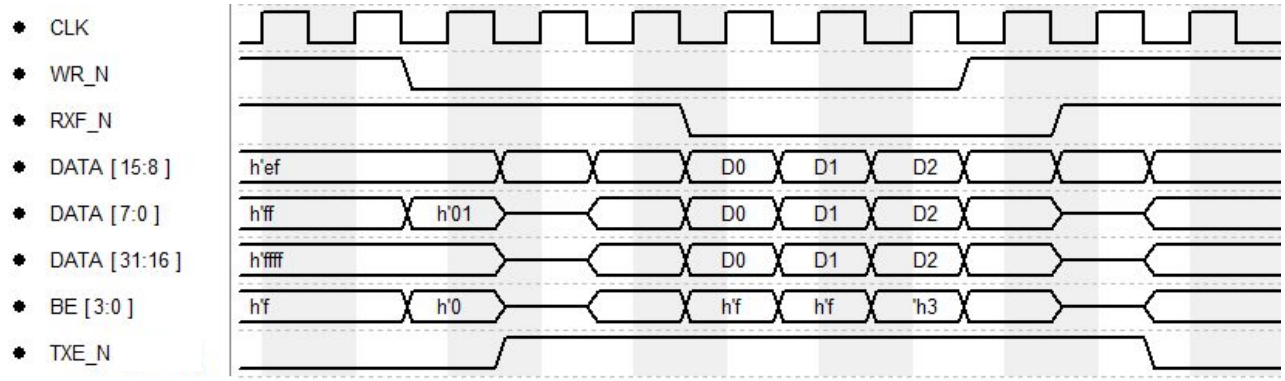


Figure 3.4 Multi-Channel FIFO mode master read transaction 2

The waveform below shows a master write transaction with bus master terminating the transaction. There are turn-a-round cycles for DATA[15:8] after the command phase and at the end of the data transaction.

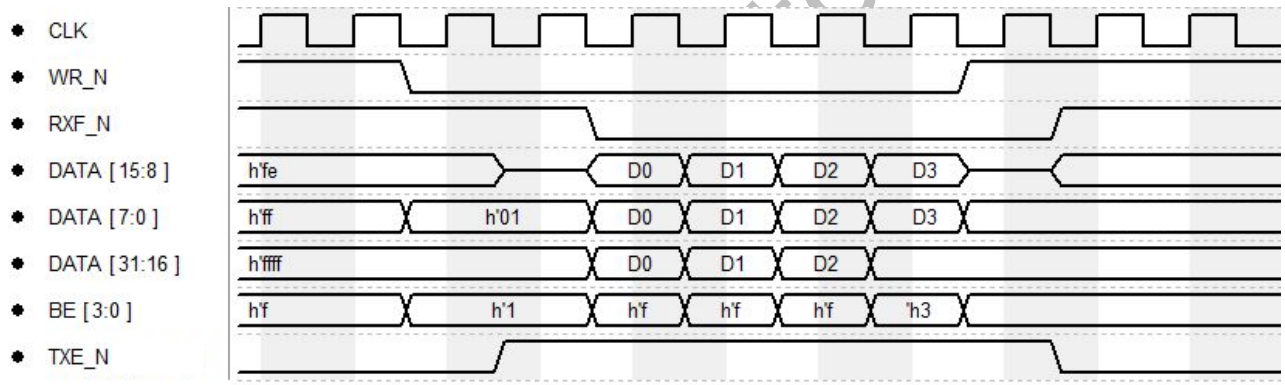


Figure 3.5 Multi-Channel FIFO mode master write transaction 1

The waveform below shows a master write transaction where the FIFO uses all data space first. There are turn-a-round cycles for DATA[15:8] after the command phase and at the end of the data transaction.

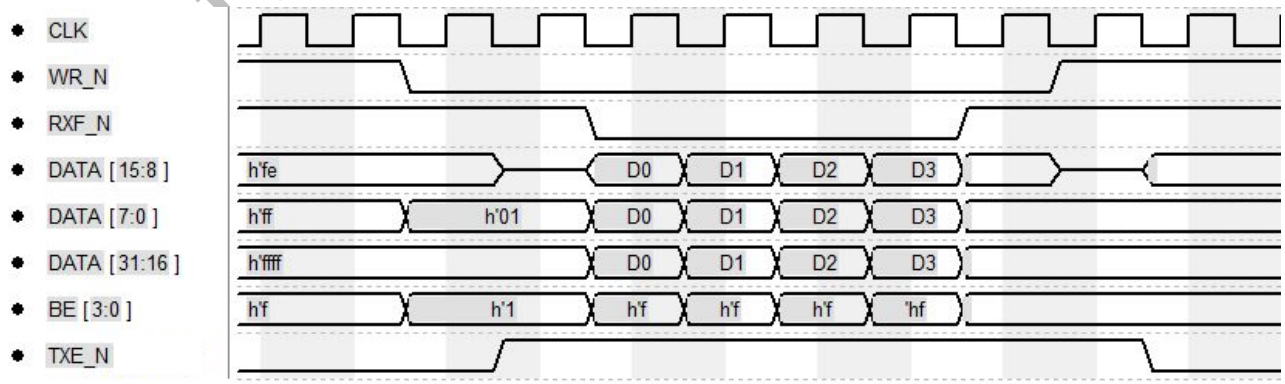


Figure 3.6 Multi-Channel FIFO mode master write transaction 2

3.4 245 Synchronous FIFO mode Protocols

This slave bus uses one IN and one OUT FIFO channel while in this mode.

CLK is the clock output to bus master, can be configured as 66Mhz or 100Mhz.

TXE_N is an output signal, Transmit FIFO Empty, it is active low, when active it indicates the Transmit FIFO is empty and it is ready to receive data.

RXF_N is an output signal, Receive FIFO Full, it is active low, when active it indicates the Receive FIFO is full with data and it is ready to be sent.

OE_N is an input signal, Output Enable, it is active low, when it is driven low by the bus master, the slave will drive the data and byte enable buses.

WR_N is an input signal, Write Enable, it is active low, when it is driven low by the bus master, the master has write cycle access.

RD_N is an input signal, Read Enable, it is active low, when it is driven low by the bus master, the master has read cycle access.

SIWU_N is an input signal, Send Immediate/WakeUp, it is active low, when it is driven by the bus master during a master write cycle to indicate no more pending data for the whole transfer after this transaction. This signal is also used as wake up signal when slave is in sleep mode.

There are 2 waveforms below to show 245 synchronous FIFO bus master write and read cycles.

The waveforms below show 245 synchronous FIFO bus master read and write access cycle.

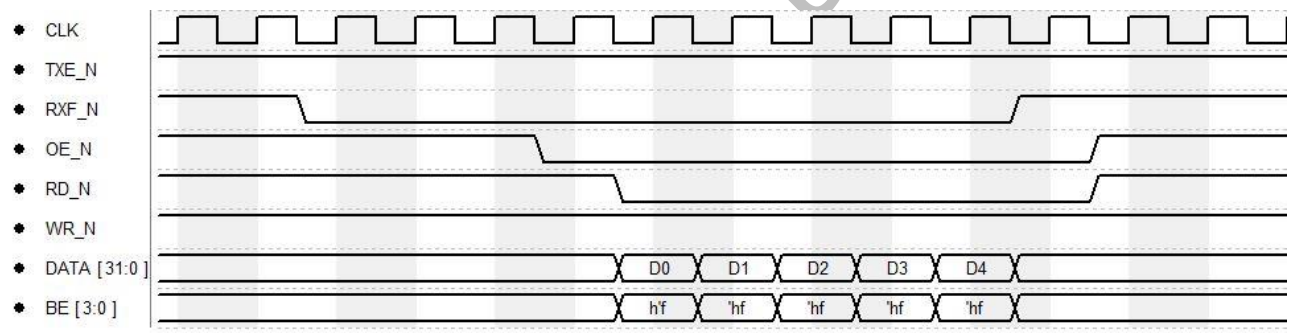


Figure 3.7 245 Synchronous FIFO mode bus master read cycle

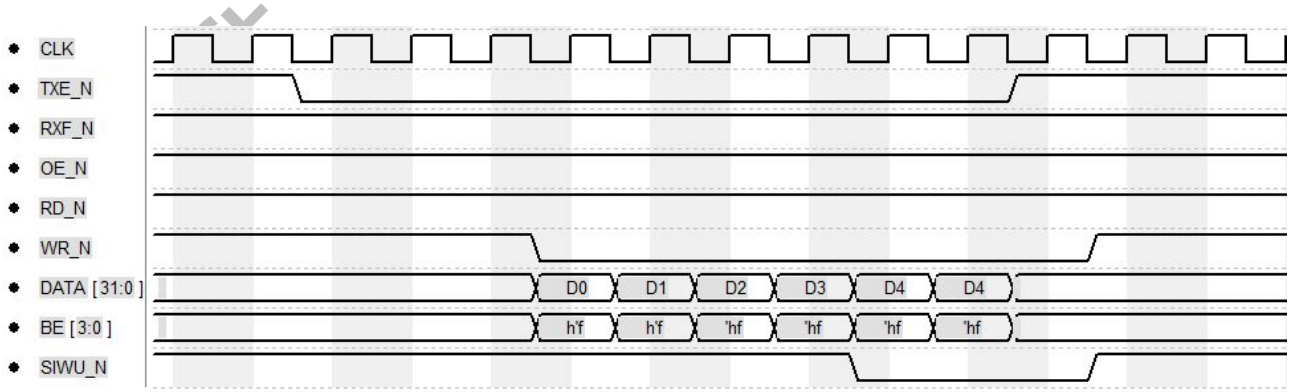


Figure 3.8 245 Synchronous FIFO mode bus master write cycle

4 Function Description

FT600 is a high performance USB 3.0-to-FIFO interface bridge chip. This device can be used in those applications which require high data throughput such as imaging device and Multi-Channel FIFO ADC or DAC devices etc.

The FIFO interface can support multivoltage I/O (1.8V, 2.5V, 3.3V) and an operating frequency of 66.67MHz or 100MHz. 100MHz only for 2.5V and 3.3V.

There are 2 different proprietary synchronous bus protocols supported; one FIFO bus protocol is called Multi-Channel FIFO bus protocol and the other is 245 Synchronous FIFO bus protocol.

4.1 Key Features and Function Description

Functional Integration.

FIFO protocol management, USB 3.0 controller, clock generation, power-on-reset (POR) and LDO regulator.

USB 3.0 Protocol Controller.

The USB 3.0 Protocol Controller manages the data stream from the device USB control endpoint. It handles the USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the FIFO in accordance with the USB 3.0 specification.

FIFO Management.

This unit is used to manage all PIPE data or buffers in the FIFO memory; the data is sent or received through the FIFO protocol layer. Through this block the FIFO memory can be allocated to each PIPE with any size of memory as long as the total memory allocated to all PIPEs does not exceed the maximum FIFO memory size which is 16kB. Additionally, the FIFO signals have a configurable high drive strength capability and can be set to 18Ω, 25Ω, 35Ω and 50Ω.

FIFO Bus Clock Options.

The device provides 2 frequency FIFO bus clock options: 66.67MHz and 100MHz.

Multi-Channel FIFO Bus protocol.

The multi-Channel FIFO bus is a slave bus and is designed to handle Multi-Channel FIFO connectivity. The bus protocol supports a total of 8 channels (4 INs and 4 OUTs). CLK is the clock output to the FIFO bus master.

245 Synchronous FIFO Bus protocol.

The 245 Synchronous FIFO bus is a slave bus with one IN and one OUT FIFO channel supported by this bus protocol. CLK is the clock output to FIFO bus master.

FIFO RX/TX Buffer (16k bytes).

Data sent from the USB host controller to the FIFO via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer and is removed from the buffer by reading the contents of the FIFO using the RD# pin. (RX relative to the USB interface).

Data written into the FIFO using the WR pin is stored in the FIFO TX (transmit) Buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (TX relative to the USB interface).

Internal LDO Regulator.

The LDO regulator generates the +1.0V power supply for driving the internal core of the device. Not to be used for external devices.

Reset Generator.

The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET_N input pin allows an external device to reset the FT600. Active low.

Remote Wake Up Function.

If USB is in suspend mode, and remote wake up has been enabled, driving the WAKEUP_N pin to low will cause the FT600 device to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend.

BCD(Battery Charge Detection) Function.

Supports Battery Charging spec revision1.2, it is optional for mapping the GPIO pin to indicate the detect results.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT600 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
VCC33/VDDA Supply Voltage	-0.3 to +4.6	V
VCCIO Supply Voltage	-0.3 to +4.0	V
VD10 Core Supply Voltage	-0.5 to +1.4	V
AVDD PLL Supply Voltage	-0.5 to +1.4	V
IOs DC Input Voltage	-0.5 to +VCCIO+0.5	V

Table 5.1 Absolute Maximum Ratings

5.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	**TBC**
Machine mode (MM)	**TBC**
Charged Device Mode (CDM)	**TBC**
Latch-up	**TBC**

Table 5.2 ESD and Latch-Up Specifications

5.3 DC Characteristics

5.3.1 DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC33/VDDA	VCC Operating Supply Voltage	3.0	3.3	3.6	V	
VCCIO_1	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	VCCIO=3.3V
VCCIO_2	VCCIO Operating Supply Voltage	2.3	2.5	2.7	V	VCCIO=2.5V
VCCIO_3	VCCIO Operating Supply Voltage	1.65	1.8	1.95	V	VCCIO=1.8V
VD10/AVDD	Core/PLL Operating Supply Voltage	0.9	1.0	1.1	V	
Icc_1	VCC Operating Supply Current	-	70	-	mA	Idle, SuperSpeed
Icc_2	VCC Operating Supply Current	-	65	-	mA	Idle, High Speed
Icc_3	VCC Operating Supply Current	-	185	-	mA	Active, SuperSpeed, Multi-Channel FIFO mode
Icc_3	VCC Operating Supply Current	-	4	-	mA	USB Suspend
Iccio_1	VCCIO Operating Supply Current	-	4.5	-	mA	No data transfer
Iccio_2	VCCIO Operating Supply Current		9.5		mA	Data transfer
Iccio_3	VCCIO Operating Supply Current		70		µA	USB Suspend

Table 5.3 DC Characteristics

5.3.2 DC Characteristics for I/O Interface

Parameter	Description	Min	Typ	Max	Units	Conditions
VCCIO_3.3V	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	Normal Operation
VCCIO_2.5V		2.3	2.5	2.7	V	Normal Operation
VCCIO_1.8V		1.65	1.8	1.95	V	Normal Operation
VIH		VCCIO*0.7	-	-	V	Normal Operation
VIL		-	-	VCCIO*0.3	V	Normal Operation
Iin/Iout(3.3V)	Input/output Leakage	-10	-	10	uA	Without pull-up/down
Rpu/Rpd	Input pull-up/pull down resistance	30	50	75	KΩ	Vout=0~VCCIO
Iout(VCCIO=3.3V)	Output drive strength	10	-	-	mA	Total current
Iout(VCCIO=2.5V)	Output drive strength	9.4	-	-	mA	Total current
Iout(VCCIO=1.8V)	Output drive strength	5.0	-	-	mA	Total current
Cp	Pin Capacitance	-	-	2.0	pF	

Table 5.4 DC Characteristics for I/O Interface (Except USB PHY pins)

6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT600. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT600Q and FT601Q package options.

All USB power configurations illustrated apply to both package options for the FT600 device. Please refer to Section 3 for the package option pin-out and signal descriptions.

6.1 USB Bus-Powered Configuration

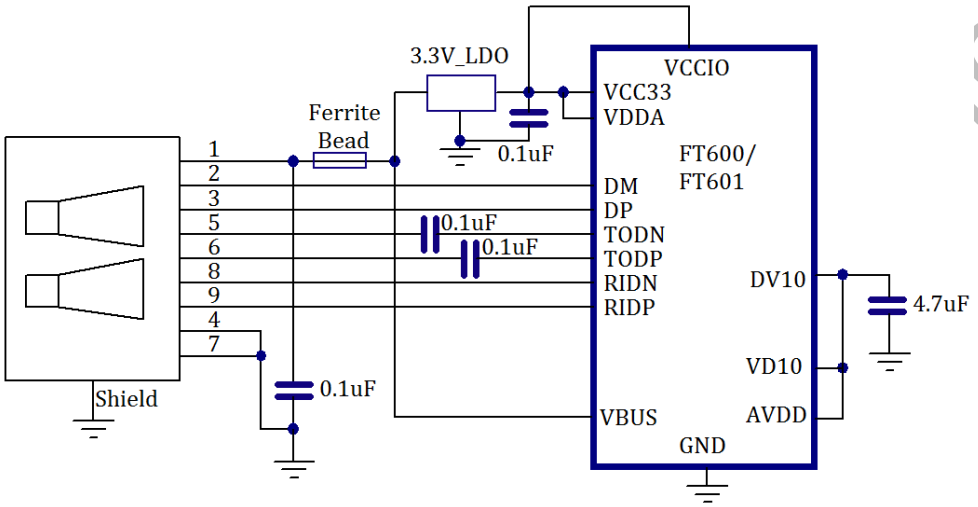


Figure 6.1 Bus-Powered Configuration-3.3V I/O

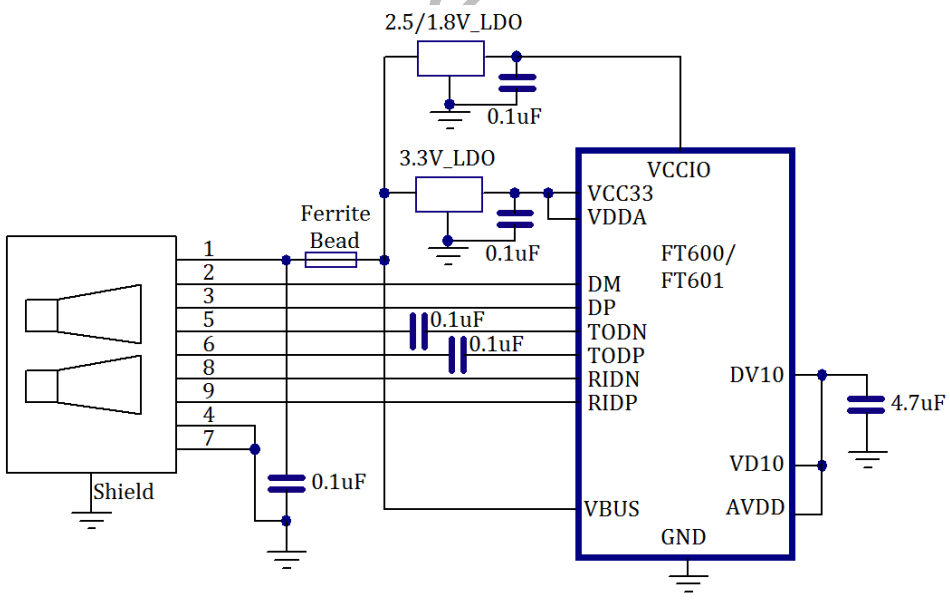


Figure 6.2 Bus-Powered Configuration-2.5V/1.8V I/O

Figure 6.1 & 6.2 illustrate the FT600 in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus via an external LDO stepping the voltage down to +3.3V.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT600 and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application.

6.2 Self-Powered Configuration

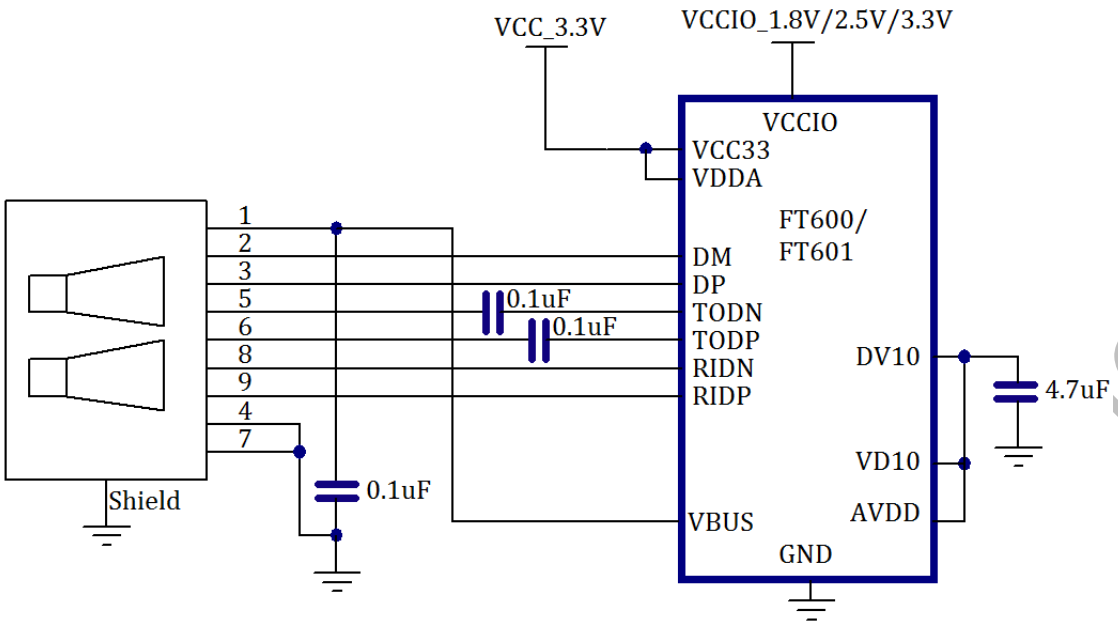


Figure 6.3 Self-Powered Configuration

Figure 6.3 illustrates the FT600 in a typical USB self-powered configuration. A USB self-powered device gets its power from its own power supply, VCC33 and VCCIO, and does not draw current from the USB bus. The basic rules for USB self-powered devices are as follows –

i) A self-powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self-powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self-powered device can be used with any USB host, a bus powered USB hub or a self-powered USB hub.

7 Application Example

The following sections illustrate possible applications of the FT600. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT600Q and FT601Q package options.

7.1 FT600/FT601 Connect to FIFO Master Interface

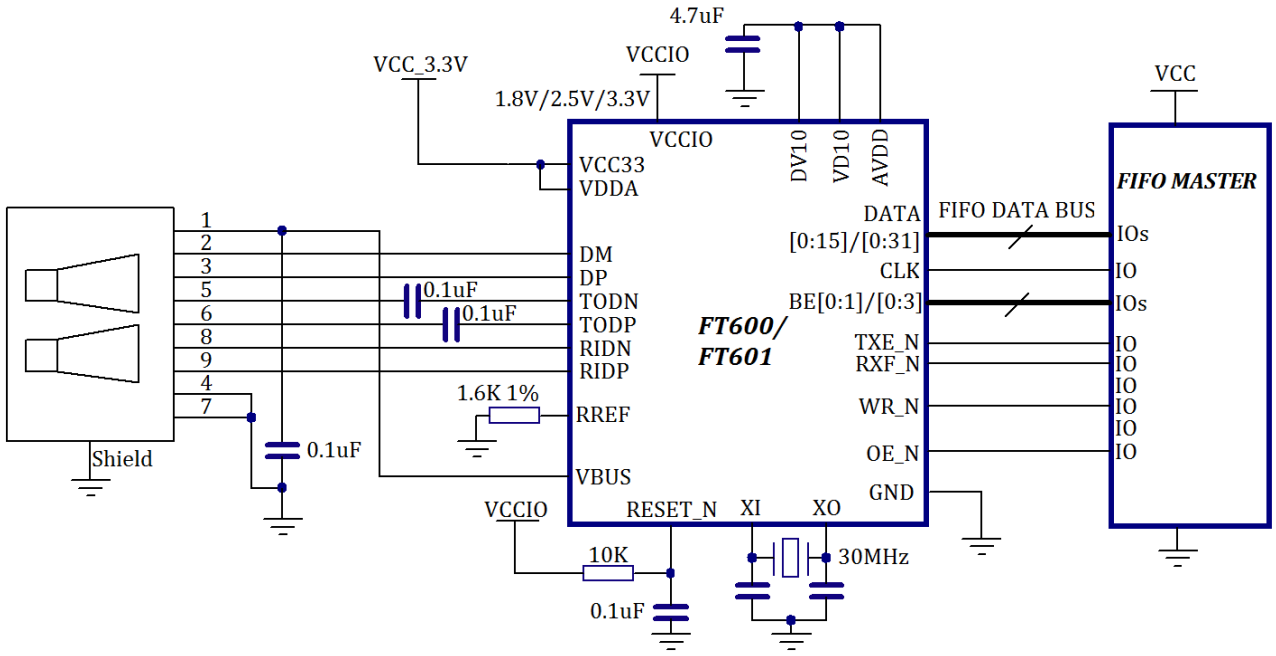


Figure 7.1 FT600/FT601 Connect to FIFO Master Interface (Multi-Channel FIFO Mode)

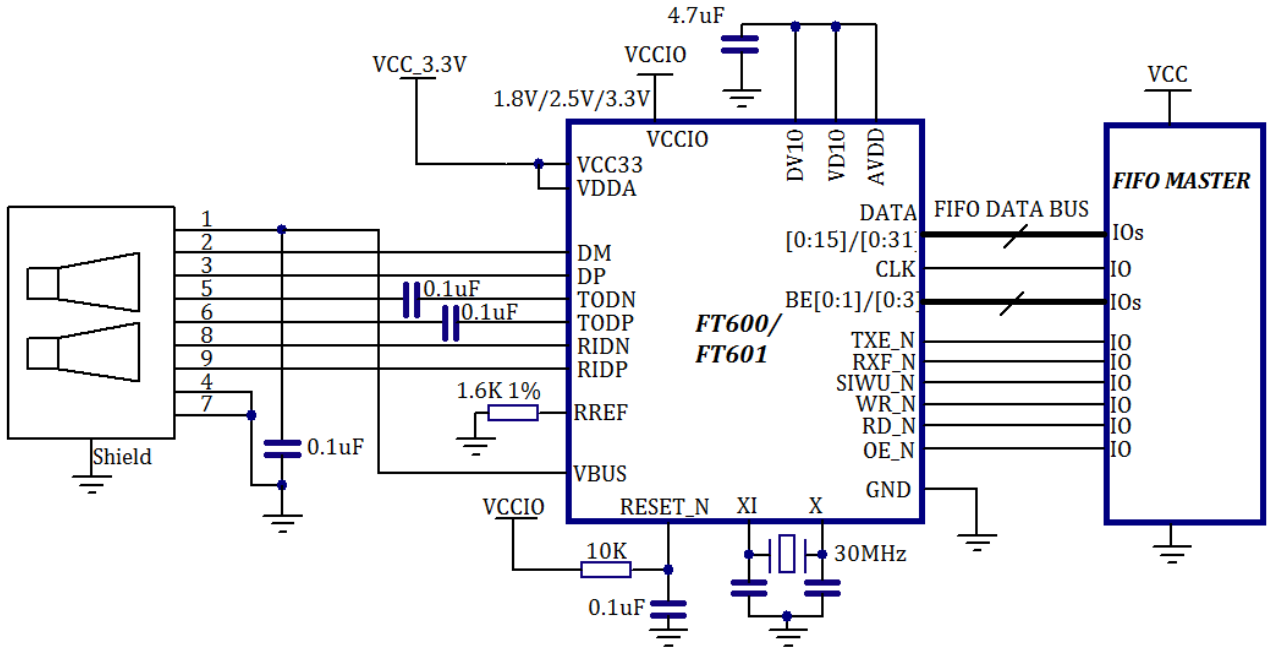


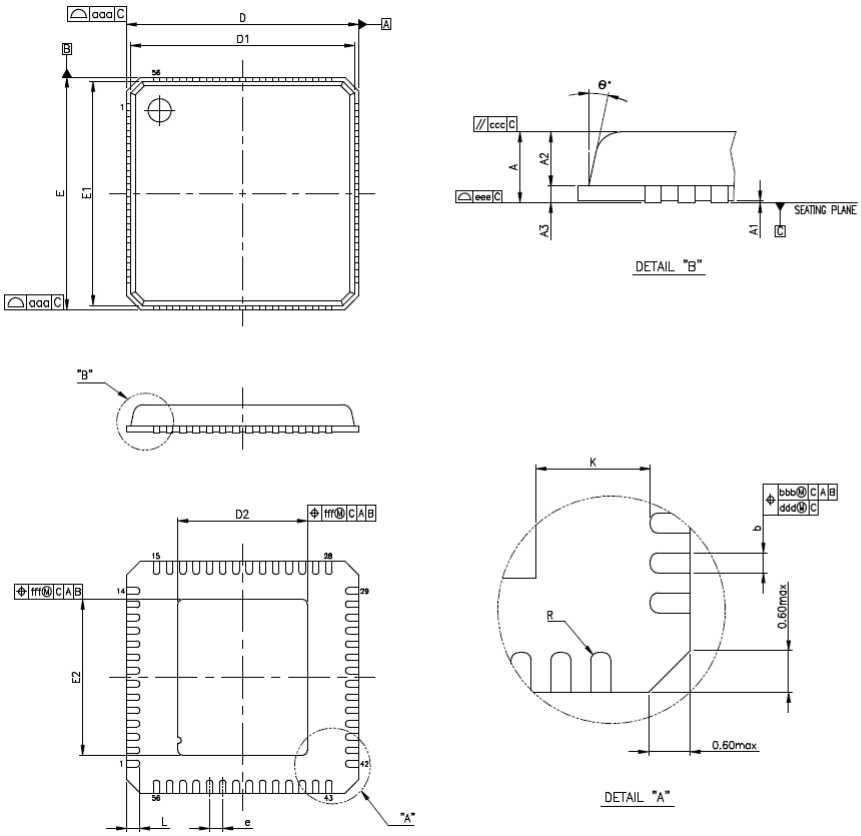
Figure 7.2 FT600/FT601 Connect to FIFO Master Interface (245 Synchronous FIFO Mode)

A typical example of using the FT600/FT601 as a USB3.0 to FIFO Master interface is illustrated in Figure 7.1. and Figure 7.2

8 Package Parameters

The FT600 is available in two different packages based on the FIFO bus interface. The FT600Q is the QFN-56 package 16-bit FIFO bus interface and the FT601Q is the QFN-76 package 32-bit FIFO interface.

8.1 QFN-56 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	6.65	6.75	6.85
E1	6.65	6.75	6.85
e		0.40 BSC	
L	0.30	0.40	0.50
θ°	0	—	12
R	0.075	—	—
K	0.20	—	—
aaa	—	—	0.10
bbb	—	—	0.07
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
fff	—	—	0.10

UNIT : mm

	D2			E2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
161X193MIL	3.75	3.90	4.05	4.55	4.70	4.85

UNIT : mm

NOTES :
1. JEDEC : MO-220 REV.K(VKKE)
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 8.1 QFN-56 Package Dimensions

The FT600Q is supplied in a RoHS compliant 56 pin QFN package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 7.0mm x 7.0 mm body and the pins are on a 0.4 mm pitch. The above mechanical drawing shows the QFN-56 package. All dimensions are in millimetres. The centre pad on the base of the FT600Q is internally connected to GND, the PCB should connect to ground and not have signal tracking on the same layer as the chip in this area.

8.2 QFN-56 Package Markings

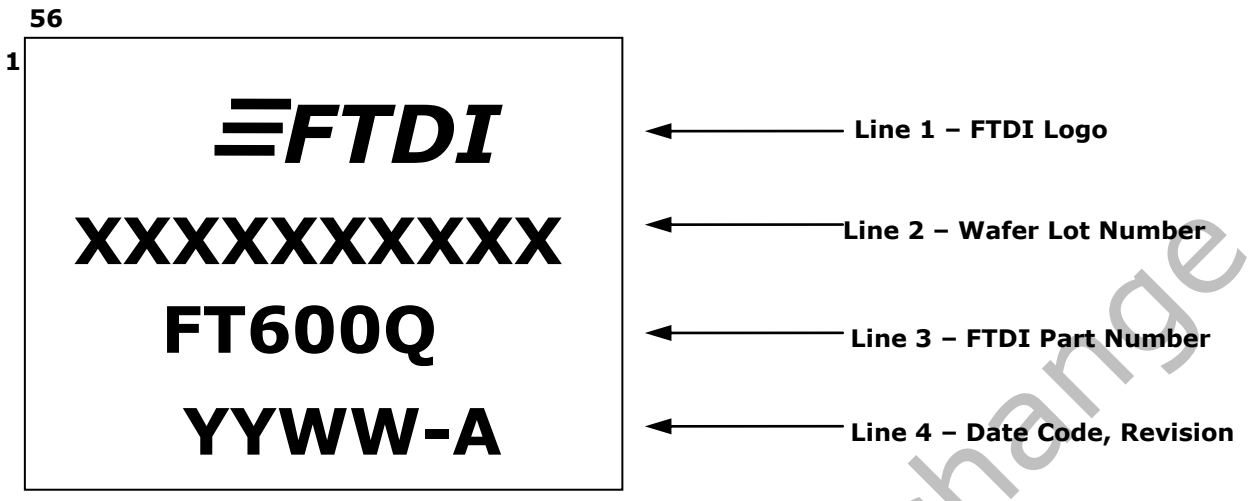
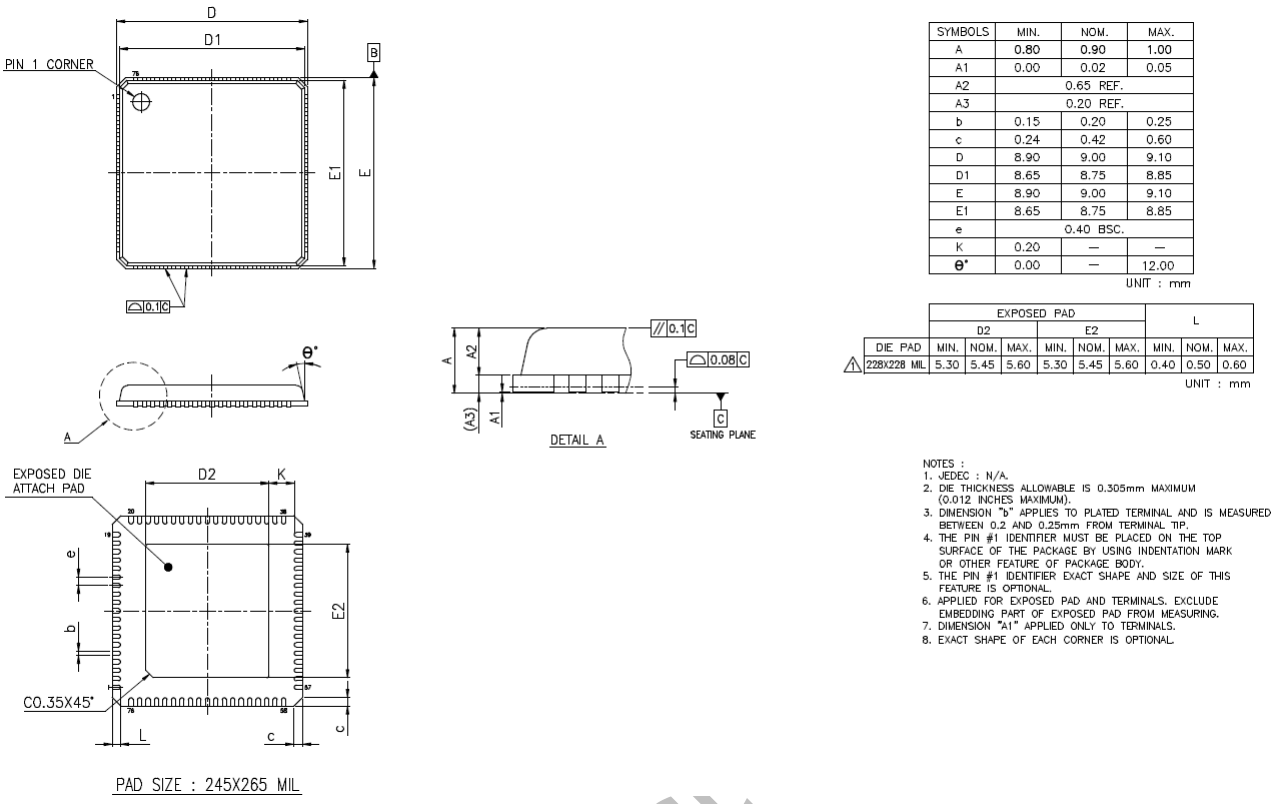


Figure 8.2 QFN-56 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex)

8.3 QFN-76 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

	EXPOSED PAD						L		
	D2			E2					
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
⚠1 228X228 MIL	5.30	5.45	5.60	5.30	5.45	5.60	0.40	0.50	0.60

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 8.3 QFN-76 Package Dimensions

The FT601Q is supplied in a RoHS compliant leadless QFN-76 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC. This package is nominally 9.0mm x 9.0mm body. The solder pads are on a 0.40mm pitch. The above mechanical drawing shows the QFN-76 package.
The centre pad on the base of the FT601Q is internally connected to GND, the PCB should connect to ground and not have signal tracking on the same layer as chip in this area.

8.4 QFN-76 Package Markings

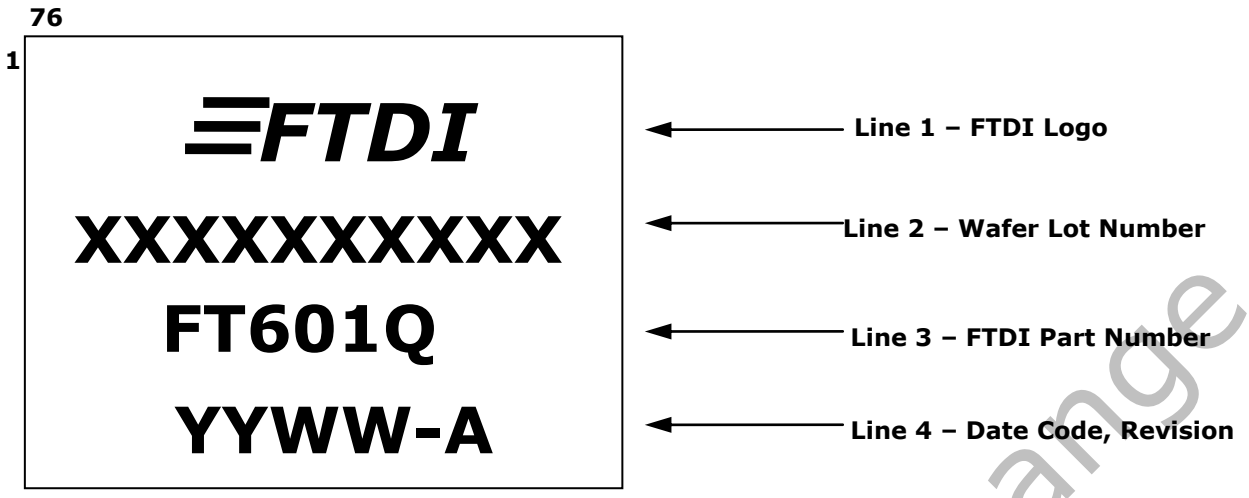


Figure 8.4 QFN-76 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Greatek standard font (Roman Simplex)

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Appendix A - List of Figures and Tables

List of Figures

List of Tables

Appendix B - Revision History

Document Title:	FT600 USB3.0 TO 16/32-BIT FIFO INTERFACE BRIDGE IC
Document Reference No.:	FT_001118
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Product Page:	
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