1.125Gbps to 6.25Gbps 2 Channel Signal Repeater

89HP0602Q
Data Sheet

Device Overview

The IDT 89HP0602Q (P0602Q) is a 1.125Gbps to 6.25Gbps Repeater featuring IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The device is optimized for differential high speed serial data streams and contains two data channels, each able to process 6.25Gbps transmission rates. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing and de-emphasis. Allowing for application specific optimization, the P0602Q, with its configurable receiver and transmitter features, is ideal for a variety of applications using a wide combination of cables and board trace materials.

All modes of active data transfer are designed with minimized power consumption. In addition, power is further reduced in the absence of input signals (loss of signal mode).

Applications

- Protocols:
  - PCIe, USB3, SAS, SATA, XAUI, SRIO, CX4, INFINIBAND, CPRI
- Systems:
  - Servers, Telecommunications, Storage, Instrumentation, Active Cabling

Features

- Compensates for cable and PCB trace attenuation and ISI jitter
- Programmable receiver equalization up to 24db
- Programmable transmitter swing and de-emphasis
- Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter
- Configurable via external pins
- No external bias resistors or reference clocks required
- Low operating power
- Available in a 20-pin QFN package (4.0 x 4.0mm, 0.5mm pitch)

Benefits

- Extends maximum cable length to over 8 meters and trace length over 48 inches
- Minimizes BER

Typical Application

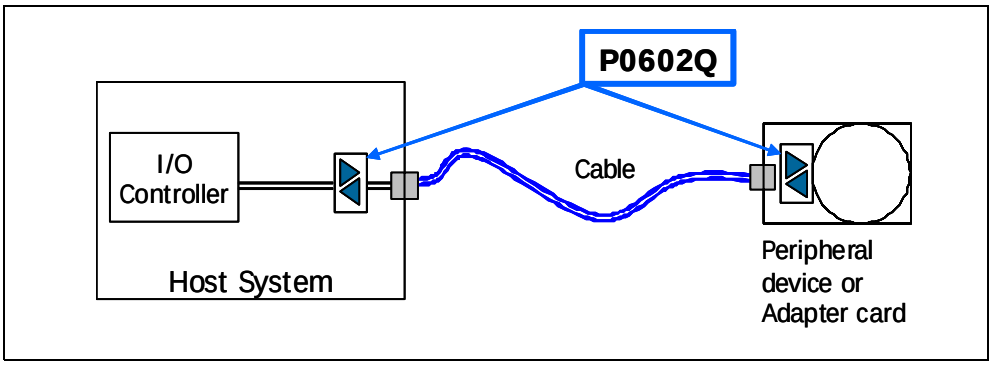

Figure 1 IDT Repeaters in Cabled Applications

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Block Diagram

The P0602Q contains two high speed channels as shown in Figure 2.

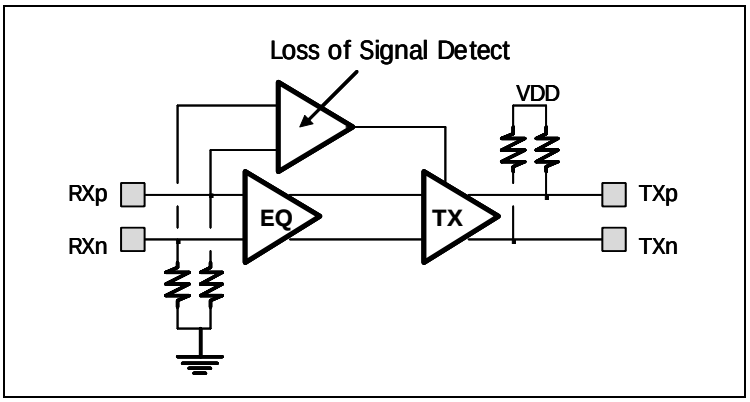


Figure 2 Block Diagram

IDT EyeBoost™ Technology

IDT EyeBoost™ technology is a method of data stream recovery even when the differential signal eye is completely closed due to cable or trace attenuation and ISI jitter. With IDT EyeBoost™ technology, the system designer can both recover the incoming data and retransmit it to target device with a maximized eye width and amplitude. An example of IDT EyeBoost™ usage in a system application and eye diagram results are shown in Figure 3. In this figure, the (a) diagram shows incoming differential signal (closed eye) after 62 inch FR4 connection from signal source and the (b) diagram shows differential signal at the output of repeater maximized eye opening with IDT EyeBoost™technology.

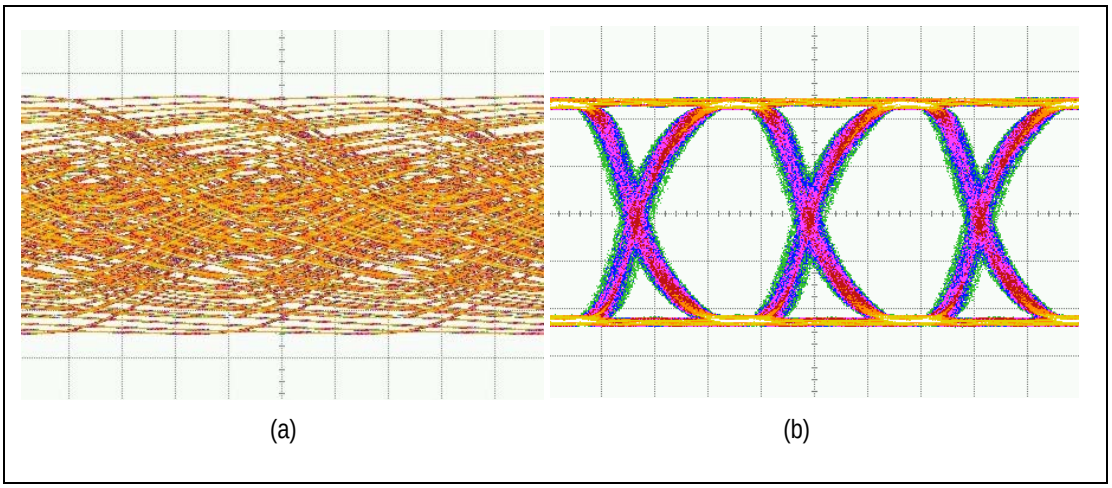


Figure 3 Eye Diagram

Functional Description

The P0602Q has 2 channels, each with the individually configurable features listed below. Figure 4 diagrams the high-speed channel.

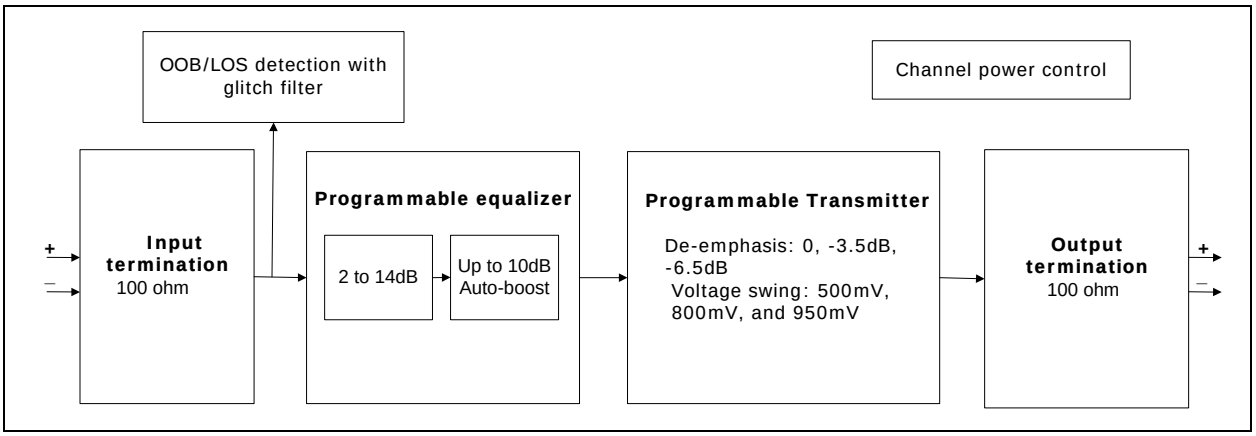


Figure 4 Channel Block Diagram with Channel Features

- Per-channel programmable features used at the Receive side.
  - Input equalization with 3 levels: 2, 6, or 14dB compensation for high frequency signal attenuation due to cables and board traces. Additionally, up to 10dB boost is added automatically by the equalizer for applications using long cables. The total equalization range is between 2dB and 24dB.
- Per-channel programmable features used at the Transmit side.
  - Output de-emphasis with 3 levels: 0, -3.5dB, or -6.5dB. The de-emphasis boosts the magnitude of higher frequencies sent by the transmitter to compensate for high frequency losses travelling through output side cable or output side board traces. This ensures that the final received signal has a wider eye opening.
  - Output differential swing with 3 levels: 0.5V, 0.8V, or 0.95V (peak-to-peak).
  - Loss of signal mode: The device enters this mode when the peak-peak differential input signal fall below 110 mV (typical).

Power-Up

After the power supplies reach recommended operating levels, the P0602Q powers up by setting all input and output pins to known states:

- All the device's input configuration pins are set internally to VDD/2 unless defined by external pull-up / pull-down resistors.
- High speed differential output pins will be determined by the input signal level.
- The power supply ramp time should be less than 1ms.

Power Sequencing

There are no power sequencing constraints for the P0602Q.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range VDD	–0.5 to 1.35	V
Voltage range Differential I/O	–0.5 to VDD +0.5	V
Control I/O	–0.5 to VDD + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±125	V
Storage ambient temperature	-55 to 150	°C

Table 1 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Notes	Min	Typical	Max	Unit
Power Supply Pin Requirements					
VDD	1.2V DC analog supply voltage	1.14	1.2	1.26	V
Temperature Requirements					
TA	Ambient operating temperature - Commercial	0	—	70	°C
	Ambient operating temperature - Industrial	-40	—	85	°C
TJUNCTION	Junction operating temperature	0	—	125	°C

Table 2 Operating Conditions

Power Consumption

Table 3 below lists power consumption values under typical and maximum operating conditions.

Parameter	Notes	Min	Typical	Max	Unit
Active Mode					
I_{VDD}	Current into VDD supply	—	165	250	mA
P_D	Full chip power[1]		200	300	mW
$P_{D\text{-}ch}$	Power per channel[1]		100	150	mW
$P_{D\text{-}IDLE}$	Full chip idle power		150	200	mW

Table 3 Power Consumption

1. Maximum power under all conditions. Power is reduced by selecting smaller de-emphasis settings (closer or equal to 0dB).

Package Thermal Considerations

The data in Table 4 below contains information that is relevant to the thermal performance of the 20-pin QFN package.

Parameter	Description	Value	Conditions	Units
$T_{J(max)}$	Junction Temperature	125	Maximum	^{0}C
$T_{A(max)}$	Ambient Temperature	70	Maximum for commercial-rated products	^{0}C
		85	Maximum for industrial-rated products	^{0}C
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	47.9	Zero air flow	^{0}C/W
		40.3	1 m/S air flow	^{0}C/W
		39.1	2 m/S air flow	^{0}C/W
		37.7	3 m/S air flow	^{0}C/W
		36.7	4 m/S air flow	^{0}C/W
		35.9	5 m/S air flow	^{0}C/W
θ_{JB}	Thermal Resistance, Junction-to-Board	14.5	NA	^{0}C/W
θ_{JC}	Thermal Resistance, Junction-to-Case	60.8	NA	^{0}C/W

Table 4 Thermal Specifications for P0602Q, 4.0x4.0mm 20-QFN Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 4. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 4), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board).

DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IL}	Digital Input Signal Voltage Low Level	-0.3	—	0.25*VDD-0.1	V
V_{IM}	Digital Input Signal Voltage Mid Level	0.25*VDD+ 0.1		0.75*VDD-0.1	V
V_{IH}	Digital Input Signal Voltage High Level	0.75*VDD+ 0.1		VDD+ 0.3	V
V_{HYS}	Hysteresis of Schmitt Trigger Input	0.1		—	V
I_{IL}	Input Current	—		180	µA
I_{IH}	Input Current	—		180	µA

Table 5 DC Specification

AC Specifications

Receiver Specifications

Parameter	Description	Min	Typical	Max	Unit
Receiver Input Jitter Specifications					
T_{RX-DDJ}	Receive Input Signal Data Dependent Jitter (Inter-Symbol Interference).	—	—	>1	UI
T_{RX-TJ}	Receive Input Signal Total Jitter	—	—	>1	UI
T_{RX-EYE}	Receiver eye time opening (can recover from closed eye due to trace attenuation and ISI jitter)	0	—	—	UI
Receiver Input Eye Specification					
$V_{RX-DIFF}$	Receiver Differential Peak-Peak Voltage[1]	0	—	2000	mV
$V_{RX-CM-DC}$	Receiver DC Common Mode Voltage	—	0	—	mV
V_{RX_IN}	Absolute Input Voltage (measured at device pins)	-0.1	—	VDD + 0.1	V
$V_{RX-CM-AC}$	Receiver AC Common Mode Voltage	—	—	100	mVp-p
$T_{skew-RX}$	RX Differential Skew (P-N skew)	—	—	30	ps
Receiver Return Loss					
$RL_{DD11,RX}$	RX Differential Mode Return Loss				
	0 MHz - 150 MHz	18	—	—	dB
	150 MHz - 300 MHz	18	—	—	
	300 MHz - 600 MHz	14	—	—	
	600 MHz - 1.2 GHz	12	—	—	
	1.2 GHz - 2.4 GHz	10	—	—	
	2.4 GHz - 3.125 GHz	8	—	—	
$RL_{RX-CM-DC}$	Receiver Common Mode Return Loss (0Hz - 3.125GHz)	8	—	—	dB
$C_{RX-CAPACITANCE}$	Receiver Input Capacitance for Return Loss	—	—	1.1	pF

Table 6 Receiver Electrical Specifications (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
Receiver DC Impedance					
$Z_{RX-DIFF-DC}$	DC differential impedance	85	—	115	Ohm
Receiver Signal Detection					
$V_{RX-Threshold}$	Signal Detection Threshold	70	110	150	mVppd
$V_{RX-CM-DC-ACTIVE-LOS-DELTA-P}$	RX AC Common Mode Voltage during the active to loss of signal state transition	—	—	200	mV
$T_{RX-LOS-DET-DIFF-ENTER-TIME}$	Loss of Signal Enter Detect Threshold Integration Time	—	—	10	ms
$T_{LOSS-EXIT}$	Loss of Signal Exit Time (Turn-on time)	—	—	15	ns
$T_{LOSS-ENTER}$	Loss of Signal Enter Time (Turn-off time)	—	—	15	ns
$T_{LOS-DECAY-MIS}$	Signal Detect Attack / Decay Time Mismatch	—	—	5	ns

Table 6 Receiver Electrical Specifications (Part 2 of 2)

1. The minimum value of 0 mV represents the case when Eye is completely closed.

Transmitter Specifications

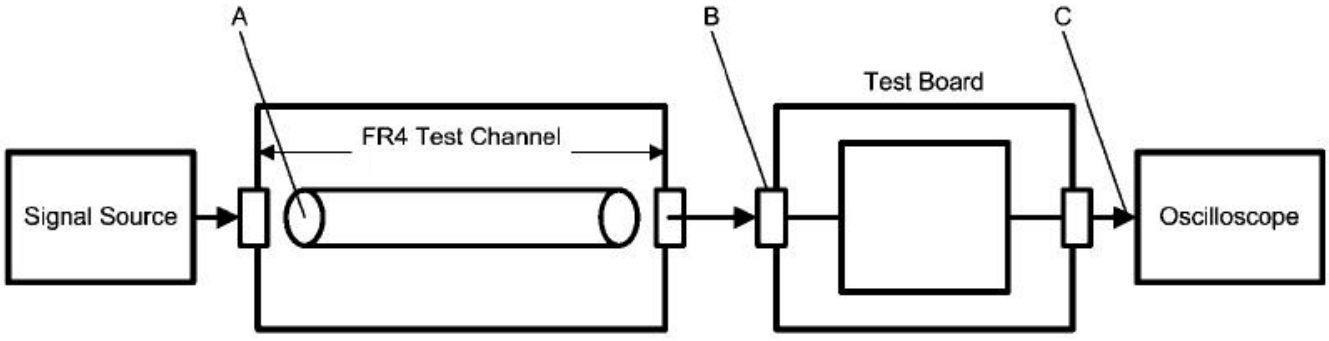
Parameter	Description	Min	Typical	Max	Unit
Output Eye and Common Voltage Specification					
$V_{TX-DIFF-PP}$	Differential Transmitter swing [A:B]TXSW=1 [A:B]TXSW=open [A:B]TXSW=0	 800 700 400	 950 800 500	 1100 950 650	mV
$V_{TX-DE-RATIO}$	Tx de-emphasis level ratio [A:B]TXSW=0 [A:B]TXSW=open [A:B]TXSW=1	 — -4.0 -7.5	 0 -3.5 -6.5	 — -3.0 -5.5	dB
$T_{RES-DJ-1}$	Residual Deterministic Jitter at output pins (1 inch FR4 trace before receiver input pins)[1]	—	—	<0.1	UI
$T_{RES-DJ-5GBPS-2}$	Residual Deterministic Jitter at output pins (40 inch FR4 trace before receiver input pins, 5Gbps)[1]	—	0.15	0.20	UI
$T_{RES-DJ-6GBPS-3}$	Residual Deterministic Jitter at output pins (40 inch FR4 trace before receiver input pins, 6Gbps)[1]	—	0.18	0.25	UI
$T_{20-80TX}$	TX Rise/Fall Time (20-80%)	33	—	90	ps
T_{skewTX}	TX Differential Skew (P-N skew)	—	—	20	ps
R/F_{bal}	TX Rise/Fall Imbalance	—	—	20	%
AMP_{bal}	TX Amplitude Balance	—	—	10	%
$T_{TX-RISE-FALL}$	Rise/Fall Time	0.125	—	—	UI
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	—	—	0.1	UI
$V_{TX-CM-AC-PP}$	Pk-Pk AC Common Mode Voltage Variation	—	—	50	mV
$V_{TX-CM-AC-P}$	Tx AC common mode voltage	—	—	20	mV

Table 7 Transmitter Electrical Requirements (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
$V_{TX-CM-RMS-AC}$	RMS AC Common Mode Voltage Variation	—	—	20	mV
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	—	VDD	V
$V_{TX-CM-DC-LINEDELTA}$	Absolute Delta of DC Common Mode Voltage between P and N	0	—	25	mV
Latency	Input to output signal propagation device	—	300	—	ps
$T_{TX-SKEW-LL}$	Lane-to-Lane Output Skew	—	5	10	ps
C_{TX}	AC Coupling Capacitor	12	—	200	nF
Transmitter DC Impedance					
$Z_{TX-DIFF-DC}$	Transmitter Output Differential DC Impedance	85	100	115	Ohm
$I_{TX-SHORT}$	Transmitter short-circuit current limit	—	—	60	mA
Transmitter Return Loss					
$RL_{TX-DIFF-F1}$	Transmitter Differential Return Loss (0 - 1.25GHz)	10	—	—	dB
$RL_{TX-DIFF-F2}$	Transmitter Differential Return Loss (1.25 - 3.125GHz)	8	—	—	dB
RL_{TX-CM}	TX Common Mode Return Loss				
	0 MHz - 300 MHz	8	—	—	dB
	300 MHz - 3.125 GHz	6	—	—	
$C_{TX-CAPACITANCE}$	Transmitter Input Capacitance for Return Loss	—	—	1.25	pF
Loss of Signal					
V_{TX-LOS}	Output Voltage when signal is lost (squelch)	—	—	20	mV
$V_{CM-DELTA-LOS}$	Maximum Common-Mode Step Entering/Exiting Loss of Signal State (squelched)	—	—	50	mV
$V_{TX-CM-DC-ACTIVE-LOS-DELTA}$	Absolute Delta of DC Common Mode Voltage between Active Mode and Loss of Signal State	0	—	100	mV
$V_{TX-LOS-DIFF-AC-p}$	Differential Peak Output Voltage in Loss of Signal State	0	—	10	mV
$V_{TX-LOS-DIFF-DC}$	DC Differential Output Voltage in Loss of Signal State	0	—	5	mV

Table 7 Transmitter Electrical Requirements (Part 2 of 2)

1. Refer to Figure 5.



A — FR4 Trace B — SMA Connector C — Measurement Point

Note: FR4 test channel is bypassed for 1-inch input trace case.

Figure 5 Residual Jitter Characterization Test Setup

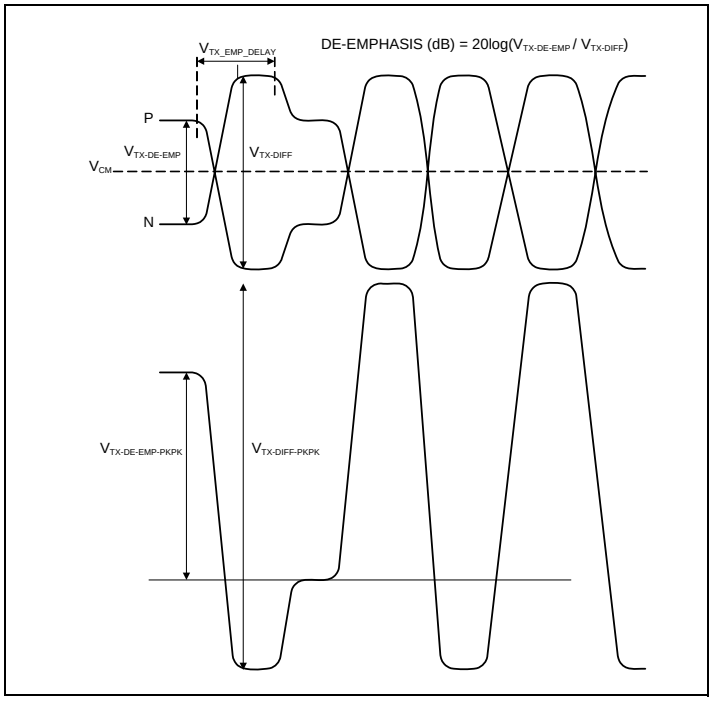


Figure 6 Transmitter Swing Levels With and Without De-emphasis

Note: $V_{TX\text{-}DIFF\text{-}PKPK}$ Peak to Peak voltage is twice as large as voltage difference between P pins and N pins of differential pairs. For example, if the P pin swings from 0.8V to 1.4V while the N pin swings from 1.4V to 0.8V, then:$V_{TX\text{-}DIFF\text{-}PKPK}$ = 2*(1.4-0.8)=1.2V.

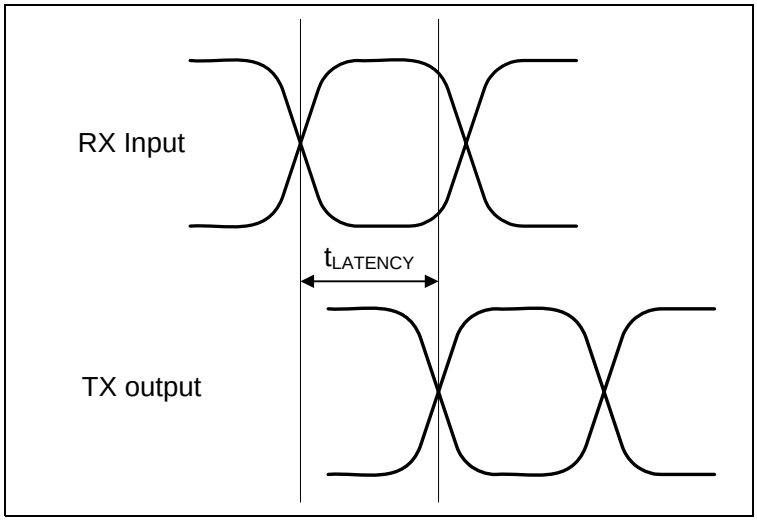


Figure 7 Definition of Latency Timing

Pin Description

Note: Unused pins can be left floating.

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
Power			
VDD	6, 16	1.2V (typ) Power supply for Repeater high speed channels and internal logic. Each VDD pin should be connected to the VDD plane through a low inductance path, with a via located as close as possible to the landing pad of VDD pins. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each VDD pin to ground plane.	Power
VSS	3, 13, center pad	VSS reference. VSS should be connected to the ground plane through a low inductance path, with a via located as close as possible to the landing pad.	Power
Data Signals			
ARXN ARXP	2 1	Channel A Receive Data Ports	Input
ATXN ATXP	14 15	Channel A Transmit Data Ports	Output
BRXN BRXP	12 11	Channel B Receive Data Ports	Input
BTXN BTXP	4 5	Channel B Transmit Data Ports	Output
Channel Control and Status			
ARXEQ (Channel A) BRXEQ (Channel B)	8 18	Receiver Equalization at F=2.5GHz (5Gbps). Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. A0RXEQ — Setting VSS — 2dB (2.5GHz) Open — 6dB (2.5GHz) (Default) VDD — 14dB (2.5GHz)	Input - 3 level
ATXSW (Channel A) BTXSW (Channel B)	19 9	Transmitter Voltage Swing (pk-pk). Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. A0TXSW — Swing — De-Emphasis VSS — 0.5Vdiff-pkpk — 0dB Open — 0.8Vdiff-pkpk (Default) — -3.5dB VDD — 0.95Vdiff-pkpk — -6.5dB	Input - 3 level
Other Signals			
NC	7, 10, 17, 20	Not connected internally.	

Table 8 Pin Description

Package Pinout — 20-QFN Signal Pinout

Table 9 lists the pin numbers and signal names for the P0602Q device.

Function	Pin	Function	Pin	Function	Pin
ARXEQ	8	ATXSW	19	BTXP	5
ARXN	2	BRXEQ	18	BTXSW	9
ARXP	1	BRXN	12	VSS	3, 13, center pad
ATXN	14	BRXP	11	NC	7, 10, 17, 20
ATXP	15	BTXN	4	VDD	6, 16

Table 9 Alphabetical Pin List

Pin Diagram

The following figure lists the pin numbers and the signal names for the 20-QFN package.

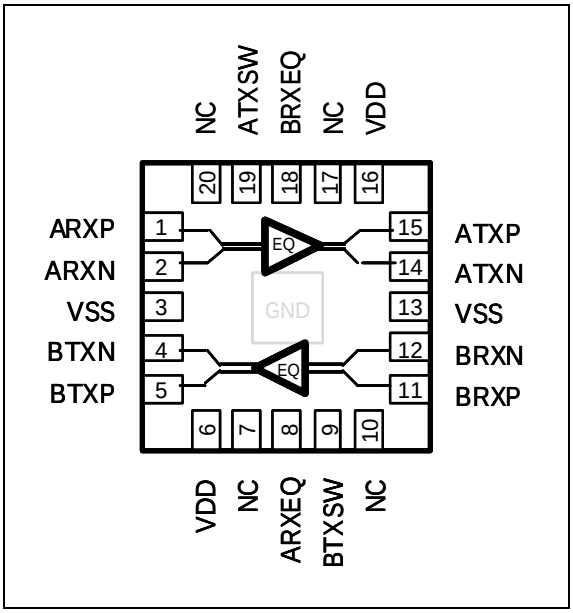
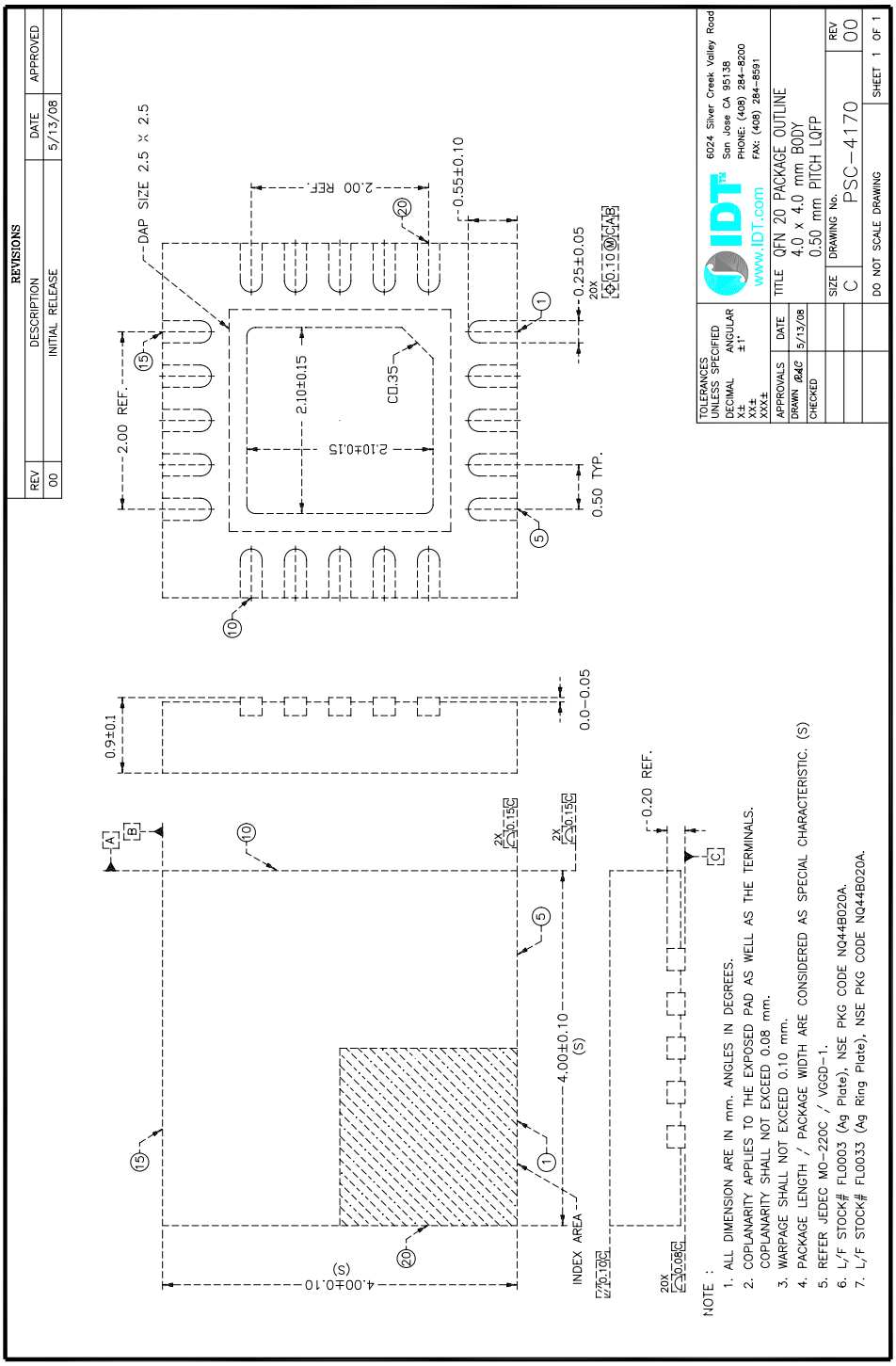


Figure 8 Pin Diagram — Top View

Note: Data positive (P) and negative (N) pins may be switched without any protocol impact provided channel polarity from host to target is maintained. Example: pins 1 and 2 may be switched provided that pins 14 and 15 are also switched; pins 4 and 5 may be switched provided that pins 11 and 12 are also switched.

QFN Package Dimension



Revision History

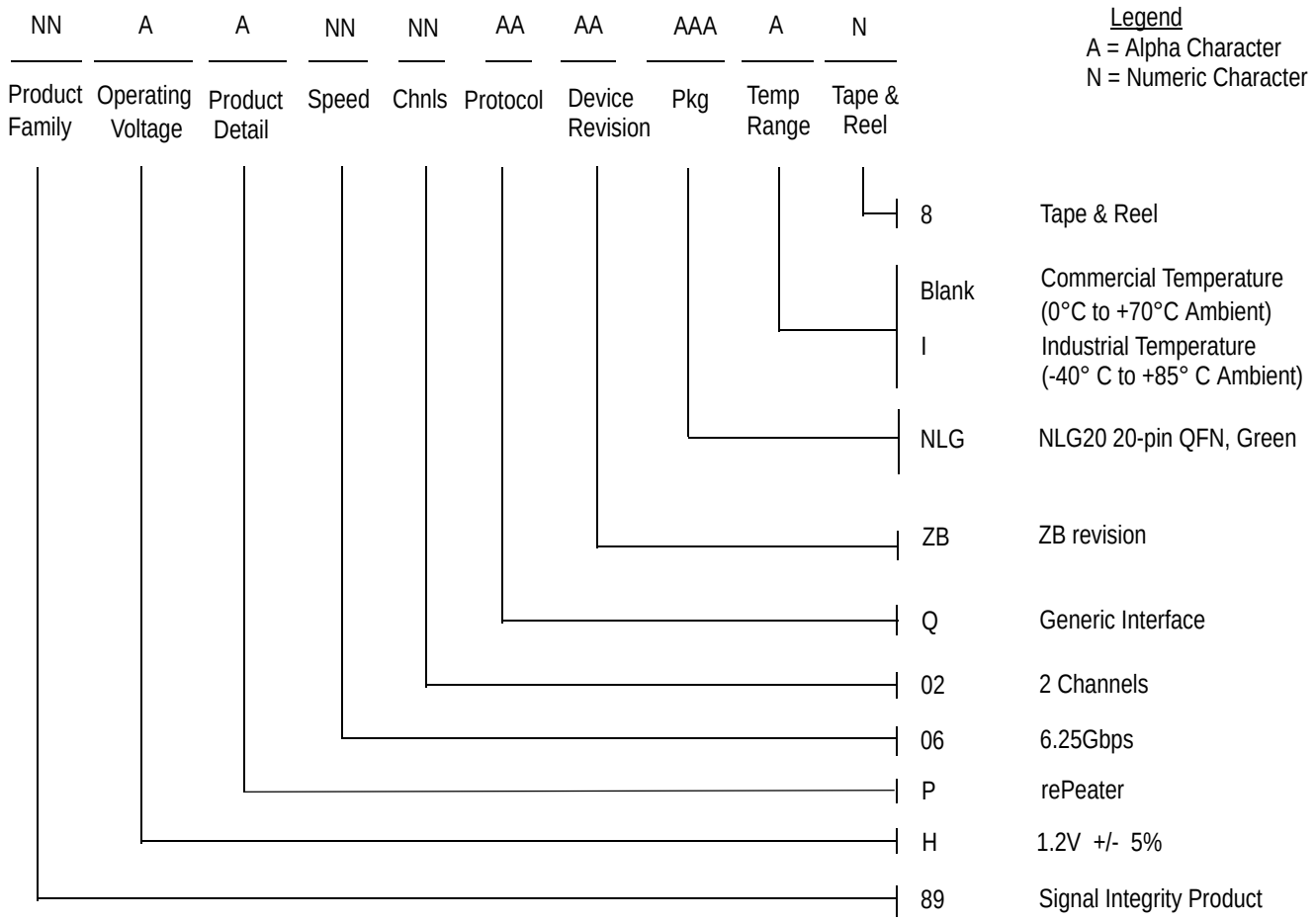
November 2, 2010: Initial publication of final datasheet.

February 8, 2011: Removed black packaging options from Order page.

February 14, 2011: Renumbered figures beginning with new Figure 4 (it was mis-labeled Figure 3).

March 18, 2011: Re-ordered BRXx and BTXx pins in Tables 8 and 9 and Figure 8 to correspond to industry pinout convention.

Ordering Information



Legend
A = Alpha Character
N = Numeric Character

Valid Combinations

89HP0602QZBNLG / 89HP0602QZBNLG8	20-pin Green QFN package, Commercial Temperature
89HP0602QZBNLGI / 89HP0602QZBNLGI8	20-pin Green QFN package, Industrial Temperature

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