

Features

- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

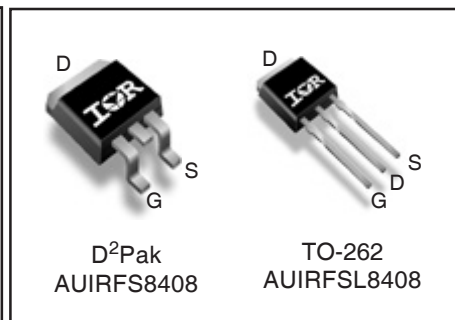
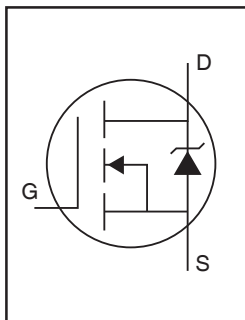
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this product an extremely efficient and reliable device for use in Automotive and wide variety of other applications.

Applications

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- SMPS

HEXFET® Power MOSFET

V_{DS}	40V
$R_{DS(on)}$ typ.	1.3mΩ
max.	1.6mΩ
I_D (Silicon Limited)	317A①
I_D (Package Limited)	195A



G	D	S
Gate	Drain	Source

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFSL8408	TO-262	Tube	50	AUIRFSL8408
AUIRFS8408	D²Pak	Tube	50	AUIRFS8408
		Tape and Reel Left	800	AUIRFS8408TRL
		Tape and Reel Right	800	AUIRFS8408TRR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	317①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	224①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	195	
I_{DM}	Pulsed Drain Current ②	1270②	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	294	W
	Linear Derating Factor	1.96	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	490	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ③	800	
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 24a, 24b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.51	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	—	40	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

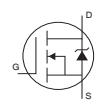
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to 25°C, I _D = 5mA ^②
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	1.3	1.6	mΩ	V _{GS} = 10V, I _D = 100A
V _{GS(th)}	Gate Threshold Voltage	2.2	3.0	3.9	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	150		V _{DS} = 40V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Internal Gate Resistance	—	2.1	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

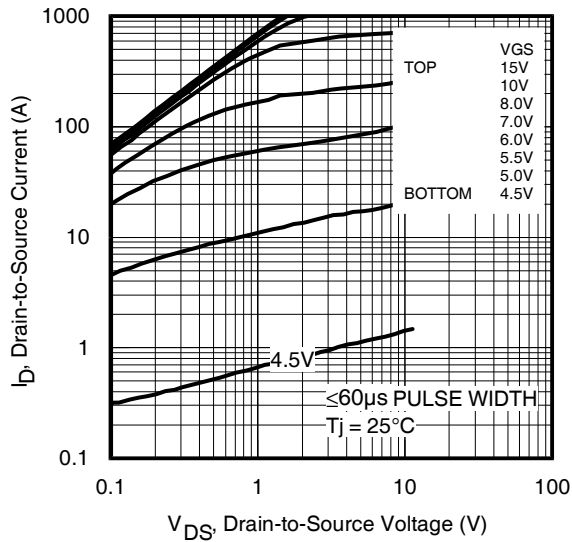
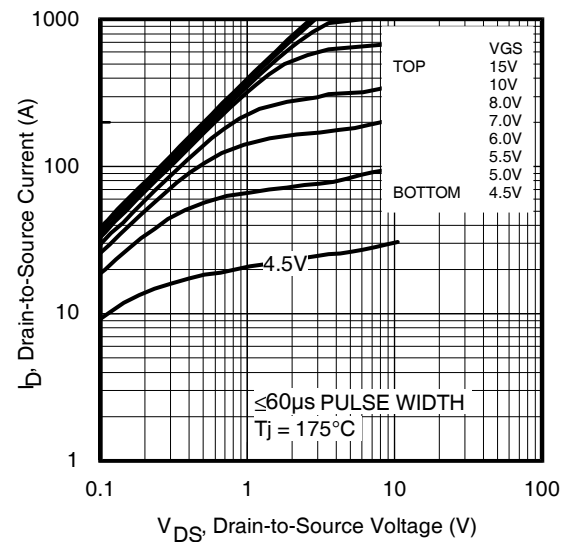
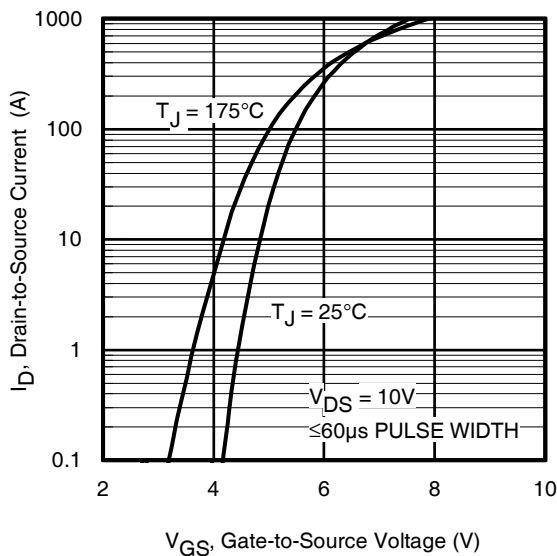
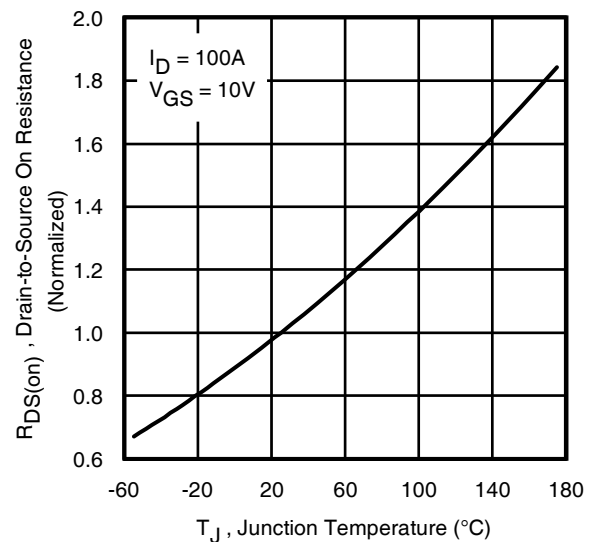
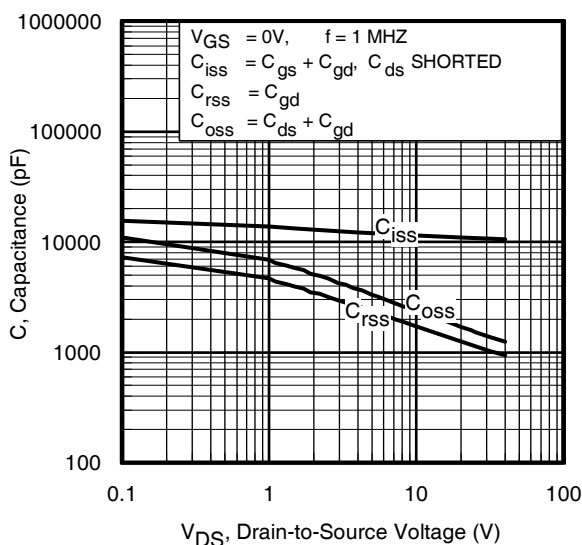
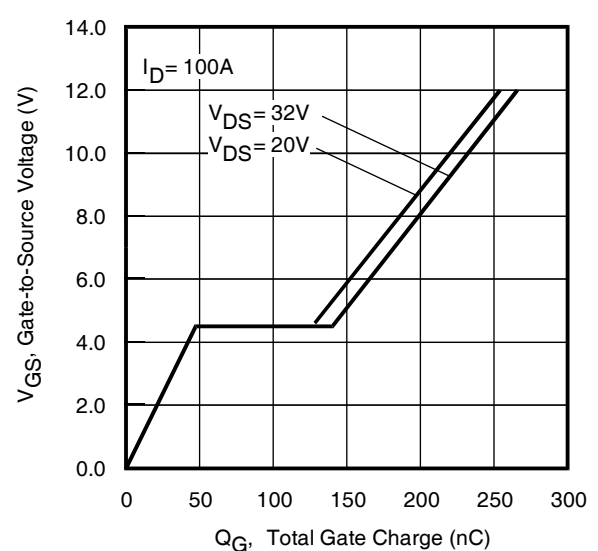
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	211	—	—	S	V _{DS} = 10V, I _D = 100A
Q _g	Total Gate Charge	—	216	324		I _D = 100A
Q _{gs}	Gate-to-Source Charge	—	51	—	nC	V _{DS} = 20V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	77	—		V _{GS} = 10V ^⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	139	—		I _D = 100A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	29	—		V _{DD} = 26V
t _r	Rise Time	—	202	—	ns	I _D = 100A
t _{d(off)}	Turn-Off Delay Time	—	108	—		R _G = 2.4Ω
t _f	Fall Time	—	119	—		V _{GS} = 10V ^⑤
C _{iss}	Input Capacitance	—	10820	—		V _{GS} = 0V
C _{oss}	Output Capacitance	—	1540	—	pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	1140	—		f = 1.0 MHz, See Fig. 5
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	1880	—		V _{GS} = 0V, V _{DS} = 0V to 32V ^⑥ See Fig. 11
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	2208	—		V _{GS} = 0V, V _{DS} = 0V to 32V ^⑦

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	317 ^①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	1270 ^⑧		
V _{SD}	Diode Forward Voltage	—	0.9	1.3	V	T _J = 25°C, I _S = 100A, V _{GS} = 0V ^⑤
dv/dt	Peak Diode Recovery ^④	—	5.0	—	V/ns	T _J = 175°C, I _S = 100A, V _{DS} = 40V
t _{rr}	Reverse Recovery Time	—	38	—	ns	T _J = 25°C V _R = 34V, T _J = 125°C I _F = 100A di/dt = 100A/μs
Q _{rr}	Reverse Recovery Charge	—	50	—	nC	
		—	50	—		
I _{RRM}	Reverse Recovery Current	—	1.9	—	A	T _J = 25°C

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.099mH, R_G = 50Ω, I_{AS} = 100A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ I_{SD} ≤ 100A, di/dt ≤ 1307A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C.
- ⑩ Pulse drain current is limited by source bonding technology.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

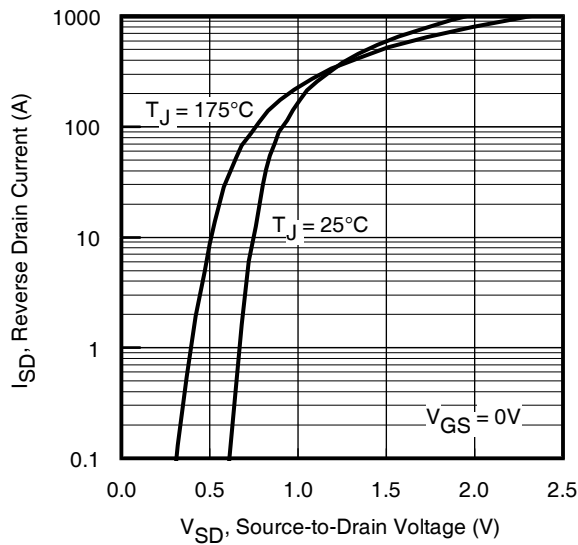


Fig 7. Typical Source-Drain Diode Forward Voltage

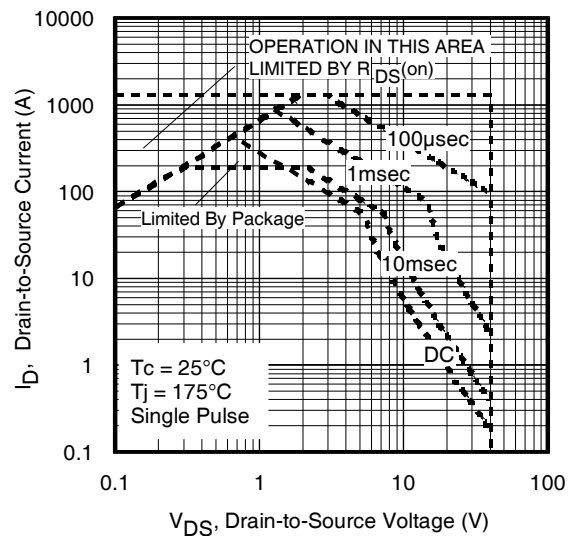


Fig 8. Maximum Safe Operating Area

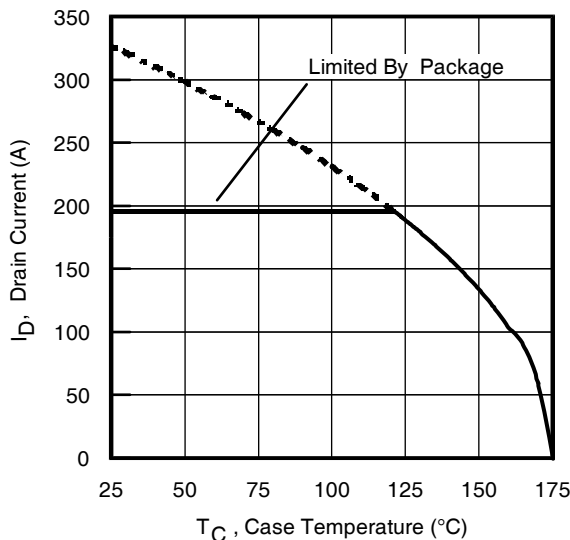


Fig 9. Maximum Drain Current vs. Case Temperature

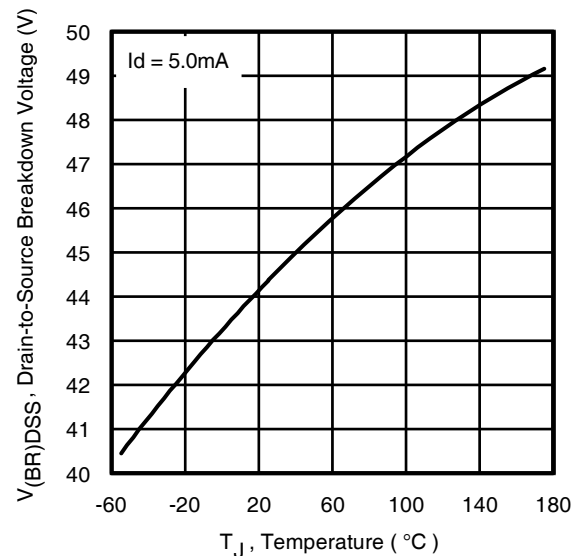


Fig 10. Drain-to-Source Breakdown Voltage

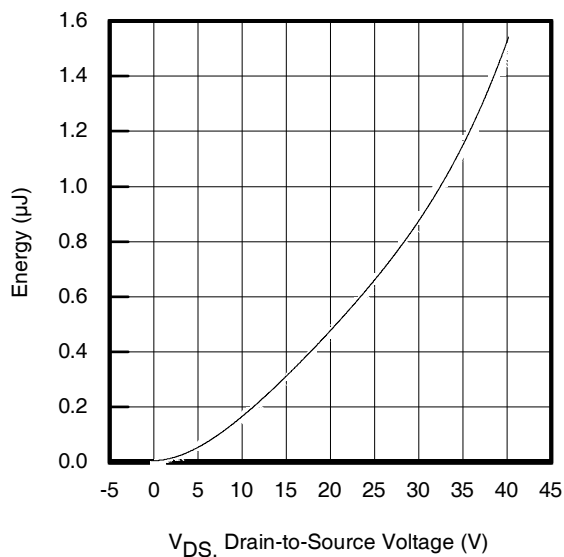


Fig 11. Typical C_{OSS} Stored Energy

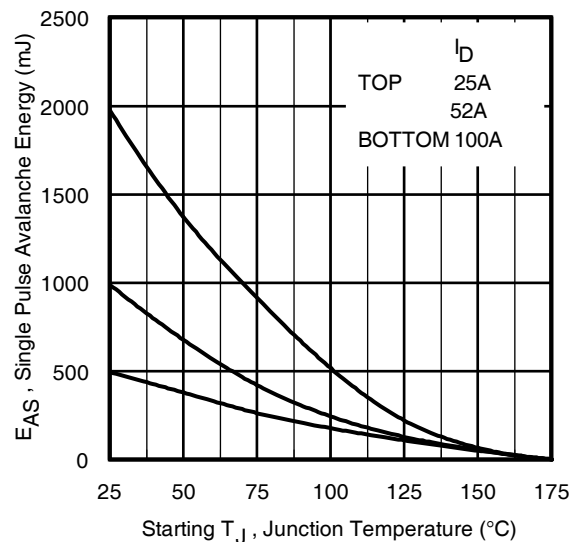
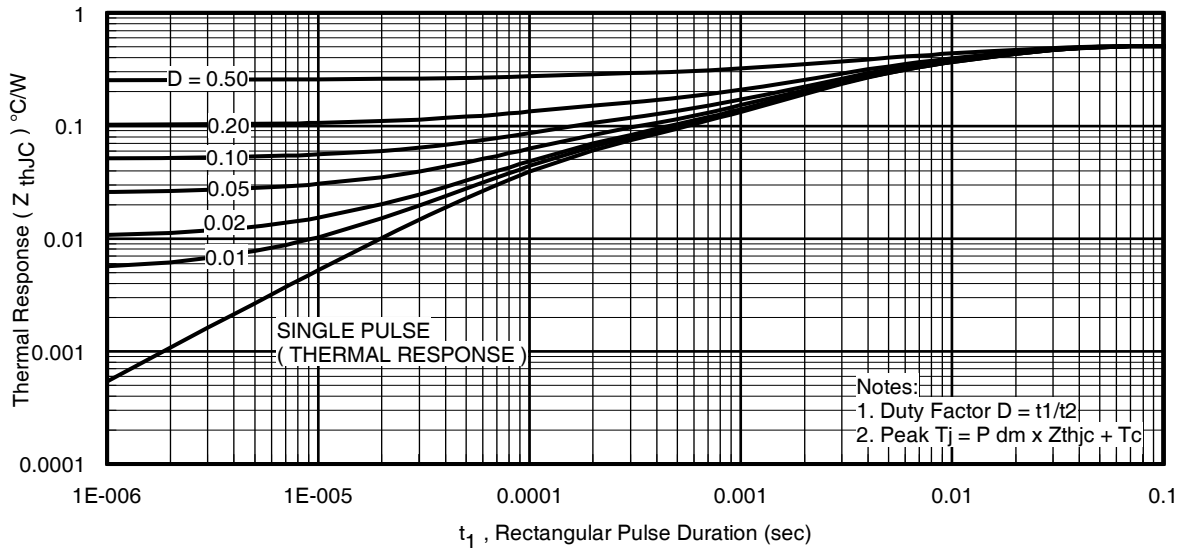
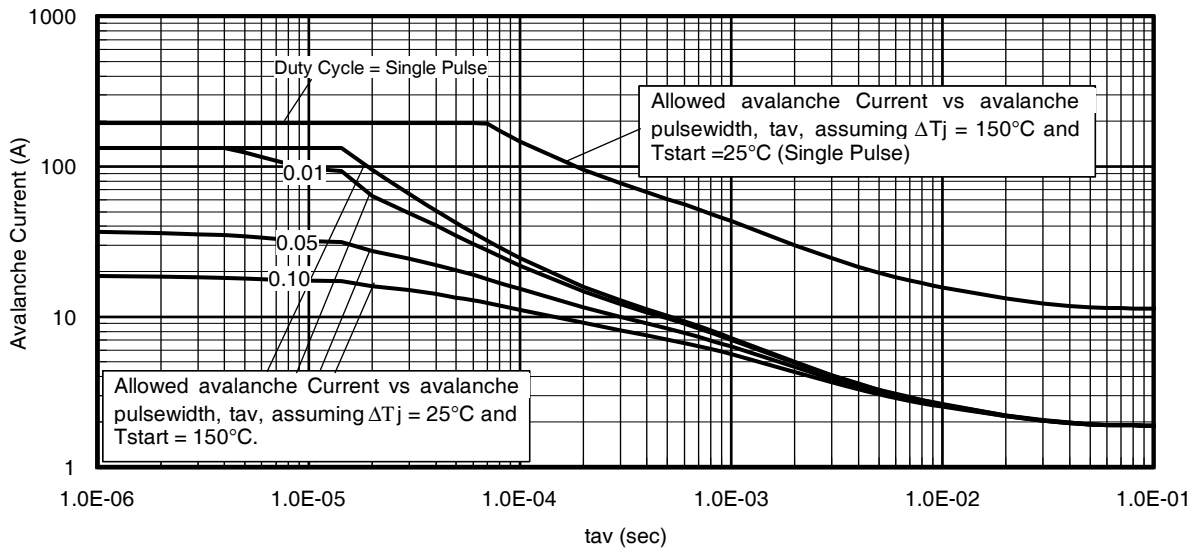
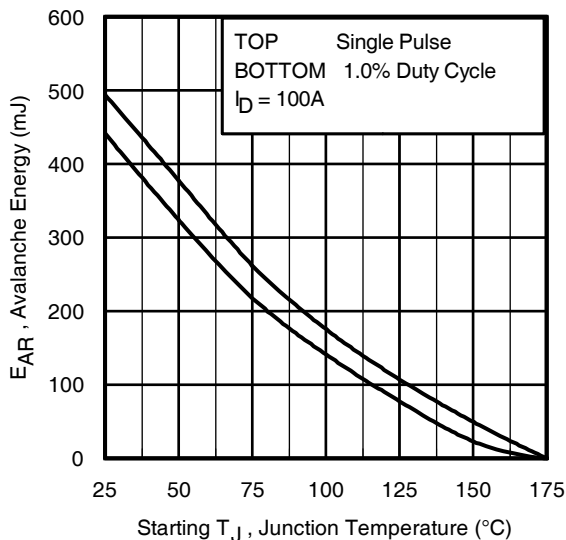


Fig 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

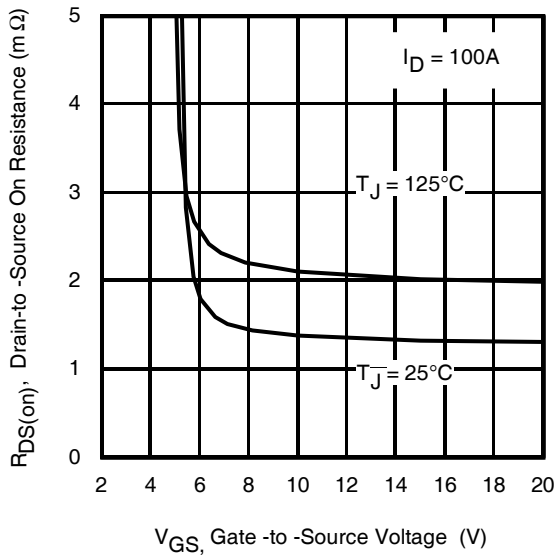
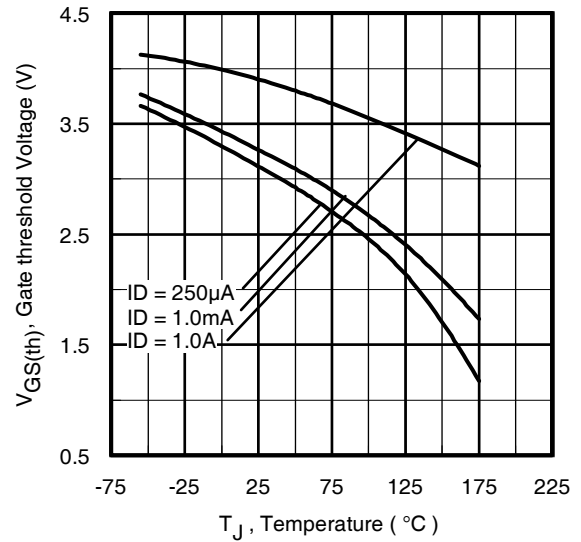
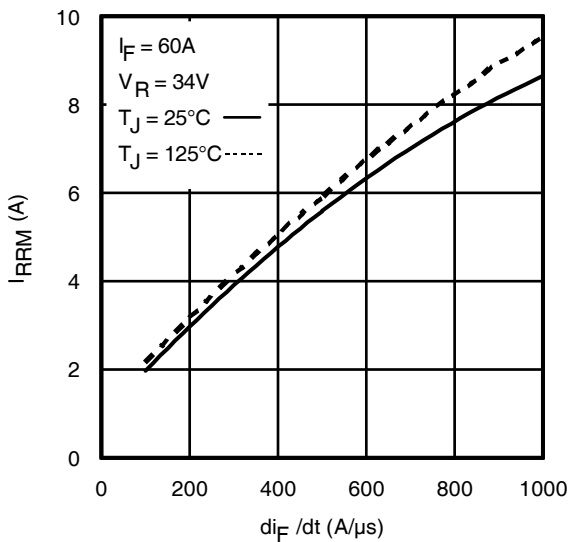
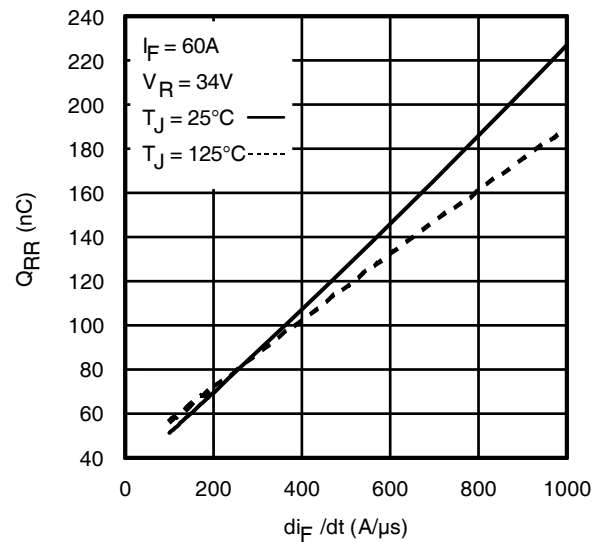
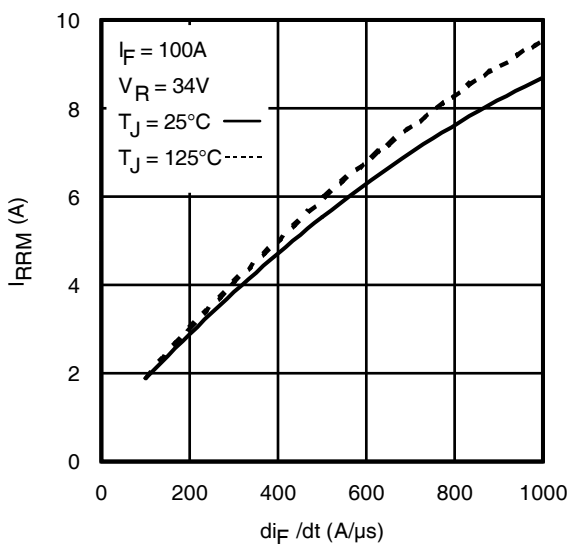
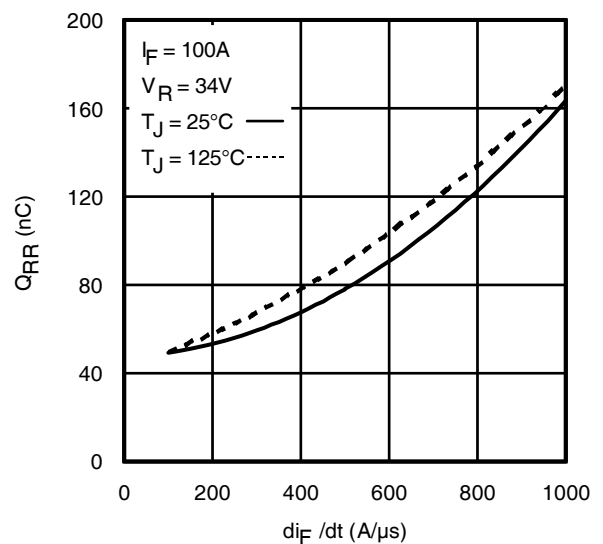
**Notes on Repetitive Avalanche Curves , Figures 14, 15
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. On-Resistance vs. Gate Voltage

Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_T/dt

Fig. 19 - Typical Stored Charge vs. di_T/dt

Fig. 20 - Typical Recovery Current vs. di_T/dt

Fig. 21 - Typical Stored Charge vs. di_T/dt

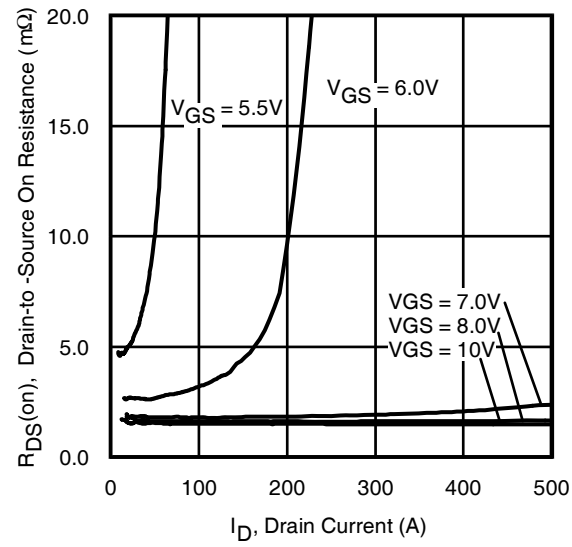


Fig 22. Typical On-Resistance vs. Drain Current

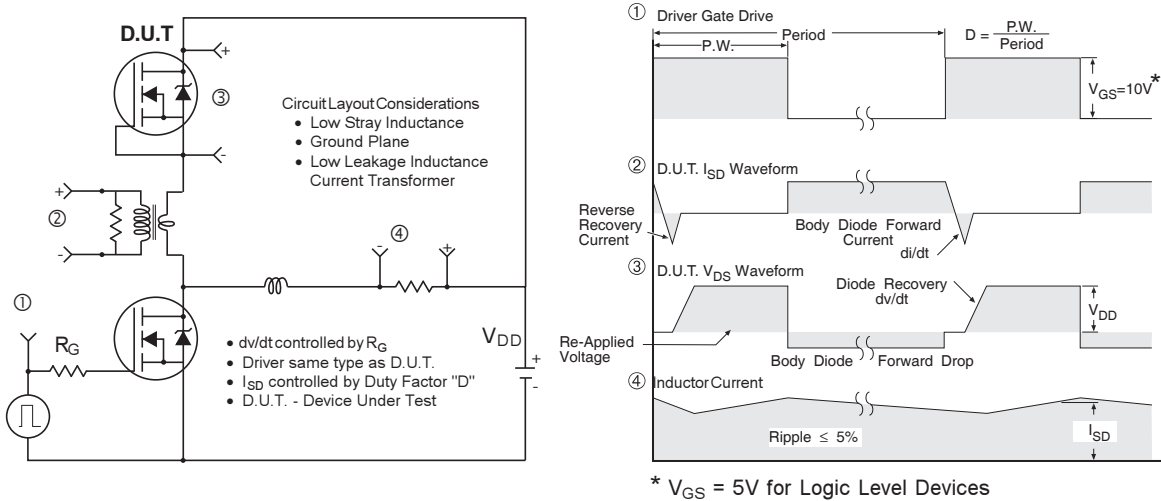


Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

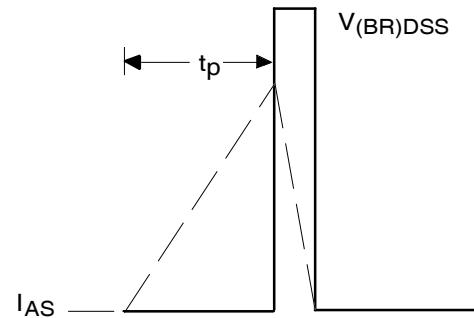
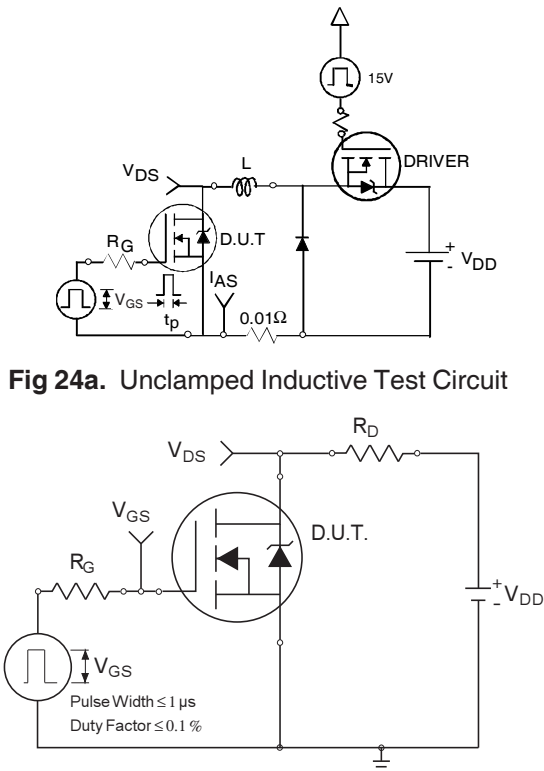


Fig 24a. Unclamped Inductive Test Circuit

Fig 24b. Unclamped Inductive Waveforms

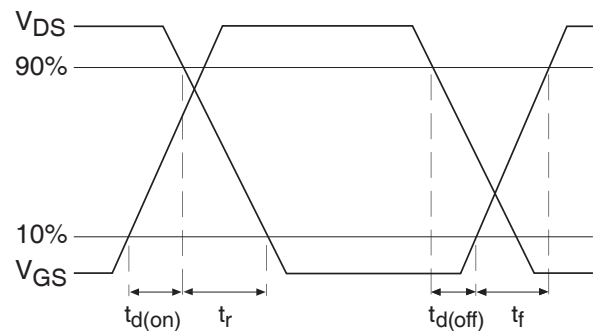
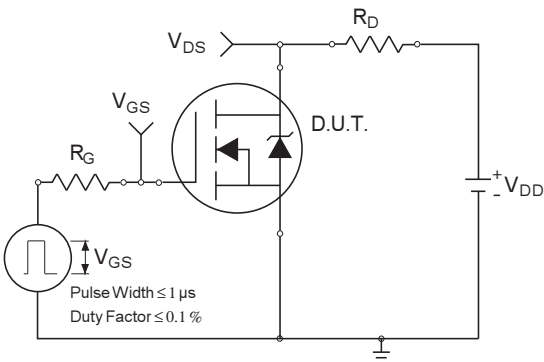


Fig 25a. Switching Time Test Circuit

Fig 25b. Switching Time Waveforms

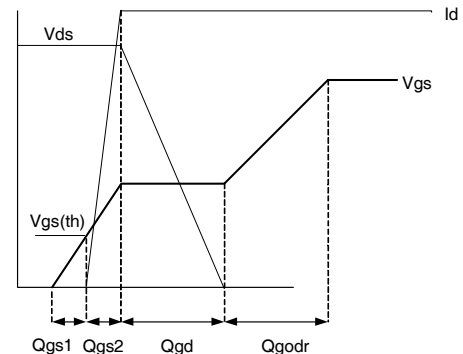
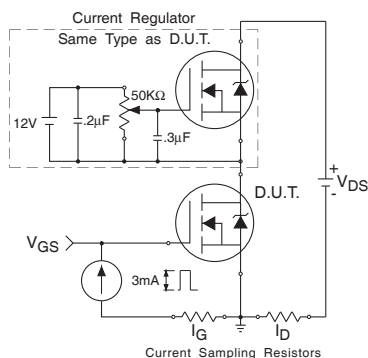
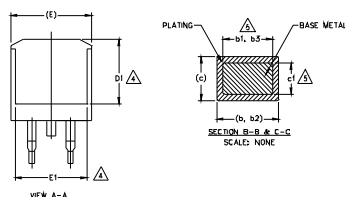
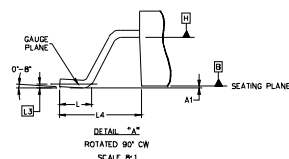
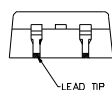
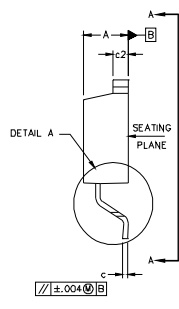
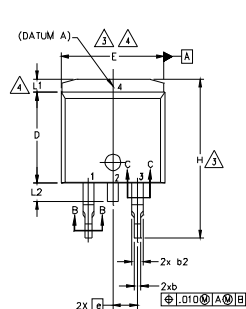


Fig 26a. Gate Charge Test Circuit

Fig 26b. Gate Charge Waveform

D²Pak Package Outline (Dimensions are shown in millimeters (inches))



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYM- BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b1	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	1.27	1.78	—	.070	
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

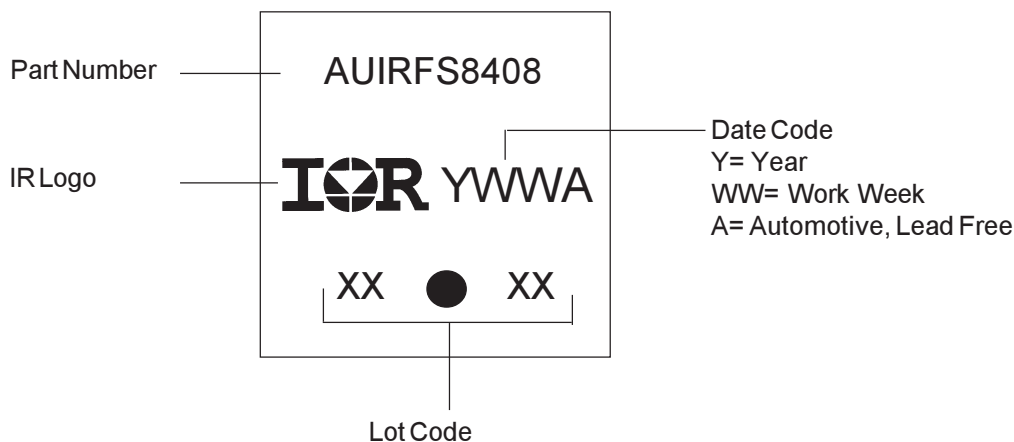
- 1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

DIODES

- 1.- ANODE *
2, 4.- CATHODE
3.- ANODE

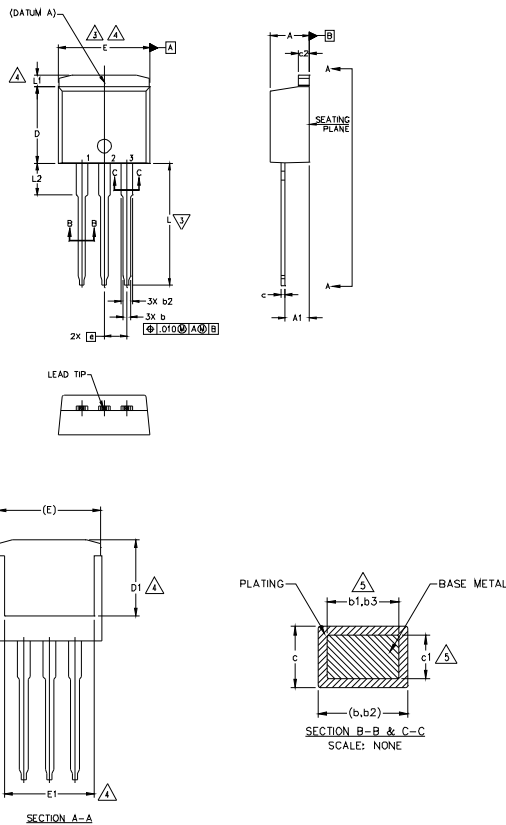
* PART DEPENDENT.

D²Pak Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

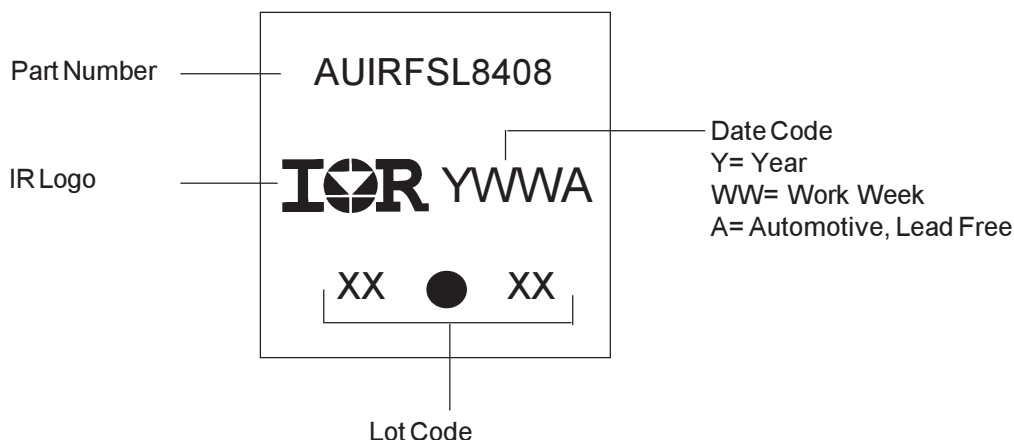
HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

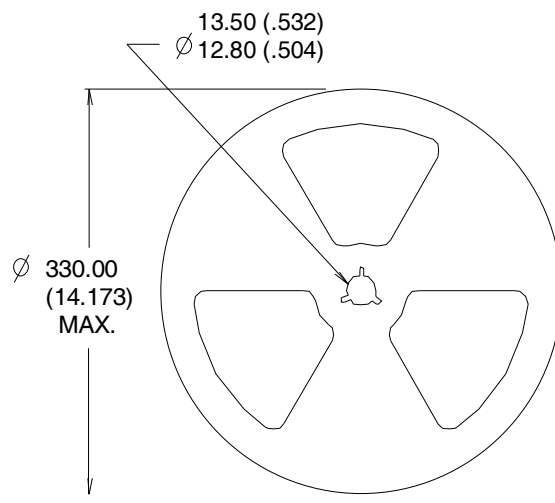
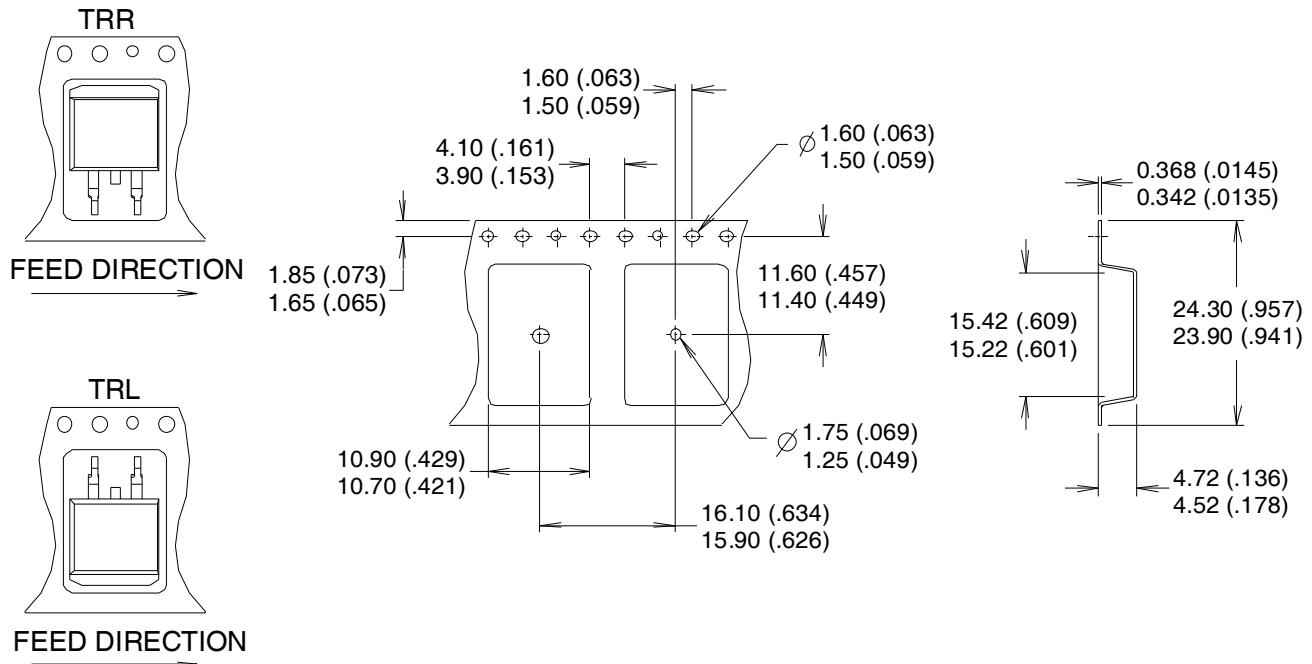
TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

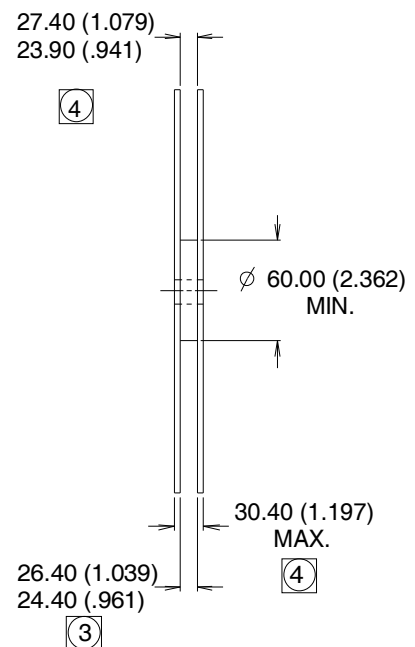
D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		3L-D ² PAK	MSL1
		3L-TO-262-PAK	N/A
ESD	Machine Model	Class M4 (+/- 600) ^{††} AEC-Q101-002	
	Human Body Model	Class H3A (+/- 6000) ^{††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000) ^{††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Highest passing voltage.

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For technical support, please contact IR’s Technical Assistance Center

<http://www.irf.com/technical-info/>

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