

ispClock5400D Evaluation Board

The ispClock5400D Evaluation Board includes everything the designer needs to quickly configure and evaluate the ispClock5406D in-system-programmable differential clock distribution device on a fully assembled printed-circuit board. The evaluation board can be used stand-alone to review the performance and in-system programmability of the 5400D device or as a companion board and clock source for LatticeECP3 FPGA evaluation boards:

- ▶ **LatticeECP3 Serial Protocol Board**
- ▶ **LatticeECP3 Video Protocol Board**

The four-layer board supports a 48-pin QFNS package, a header for user I/O and a JTAG programming cable connector. SMA connectors are installed to provide high-signal integrity access to selected high-speed I/O signals. JTAG programming signals can be generated by using an ispDOWNLOAD® programming cable connected between the evaluation board and a PC. All user-programmable features of the ispPAC-CLK5406D can be easily configured using Lattice Semiconductor's PAC-Designer® software.



Product Contents

The ispClock5400D Evaluation Board package includes:

- ▶ ispClock5406D Evaluation Board
- ▶ ispDOWNLOAD Cable (HW-USBN-2A)
- ▶ Universal AC Adapter
- ▶ QuickSTART Guide

Ordering Part Number

PACCLK5406D-S-EVN

