

# FCP104N60F

## N-Channel SuperFET® II FRFET® MOSFET

600 V, 37 A, 104 mΩ

### Features

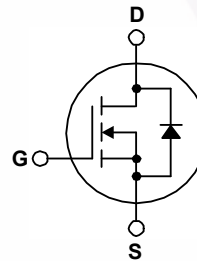
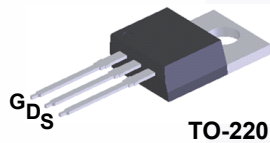
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 91\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 110\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 313\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP104N60F	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	37
		- Continuous ( $T_C = 100^\circ\text{C}$ )	24
$I_{DM}$	Drain Current	- Pulsed (Note 1)	114
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	809
$I_{AR}$	Avalanche Current	(Note 1)	6.8
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	3.57
$dv/dt$	MOSFET $dv/dt$	100	V/ns
	Peak Diode Recovery $dv/dt$	(Note 3)	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	357
		- Derate Above $25^\circ\text{C}$	2.85
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCP104N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP104N60F	FCP104N60F	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$V/^\circ\text{C}$
BV <sub>DS</sub>	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 18.5\text{ A}$	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	100	
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3	-	5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18.5\text{ A}$	-	91	104	m $\Omega$
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 18.5\text{ A}$	-	33	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	4610	6130	pF
C <sub>oss</sub>	Output Capacitance		-	3255	4330	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	155	235	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	74	-	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	313	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	110	145	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	24	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	44	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.9	-	$\Omega$

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\ \Omega$ (Note 4)	-	34	78	ns
t <sub>r</sub>	Turn-On Rise Time		-	20	50	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	102	214	ns
t <sub>f</sub>	Turn-Off Fall Time		-	5.7	21.4	ns

### Drain-Source Diode Characteristics

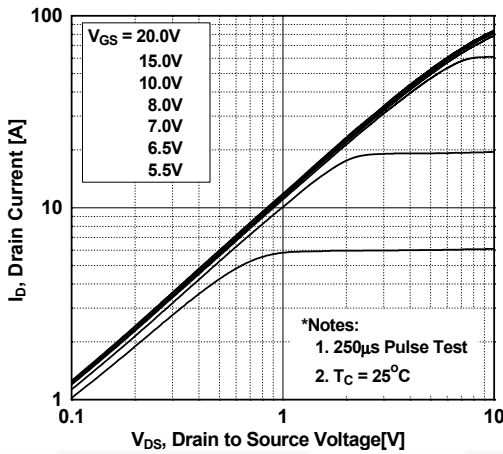
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	37	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	114	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 18.5\text{ A}$	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 18.5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	143	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	885	-	nC

#### Notes:

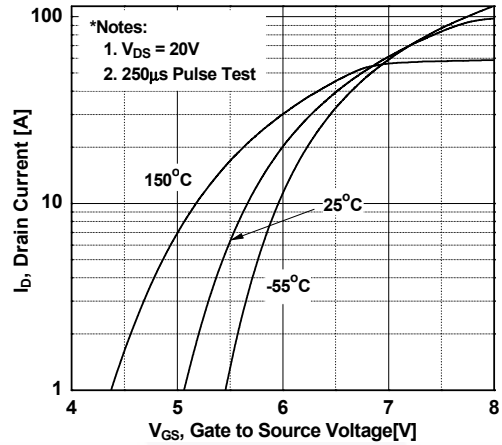
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 6.8\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 18.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Characteristics

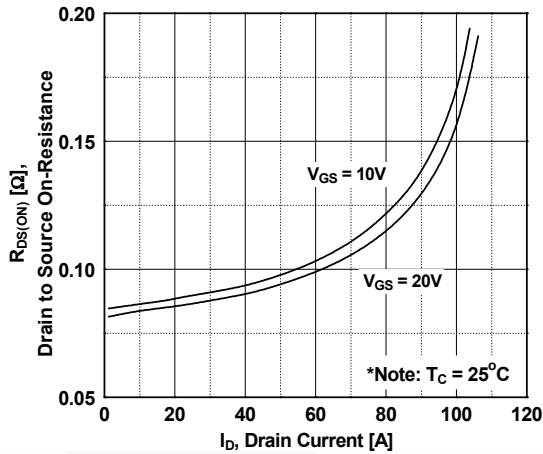
**Figure 1. On-Region Characteristics**



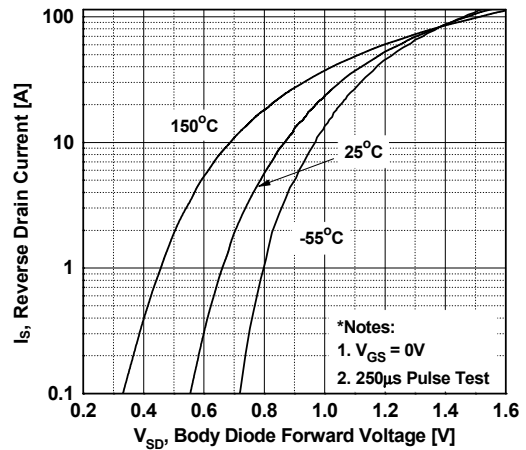
**Figure 2. Transfer Characteristics**



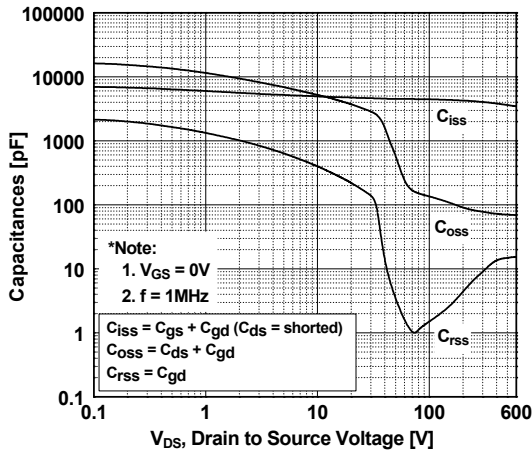
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



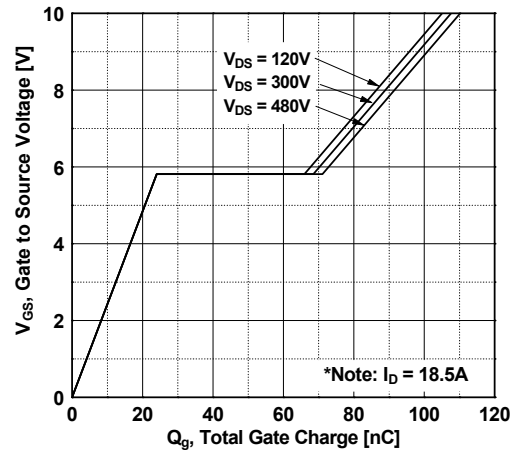
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

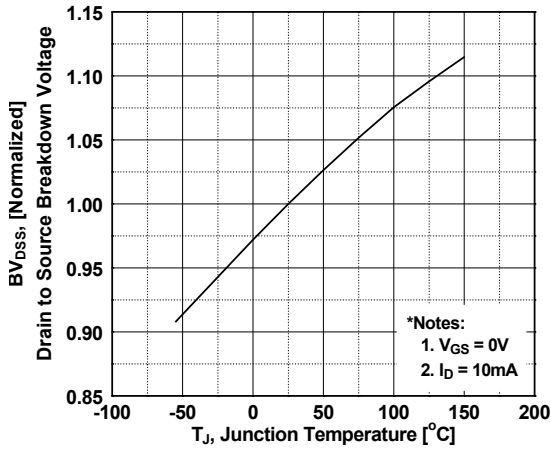


**Figure 6. Gate Charge Characteristics**

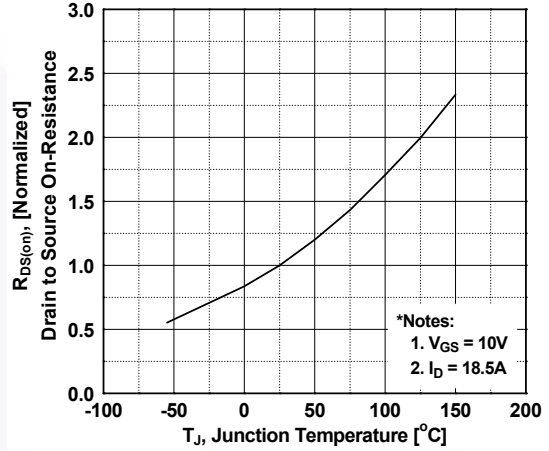


**Typical Characteristics** (Continued)

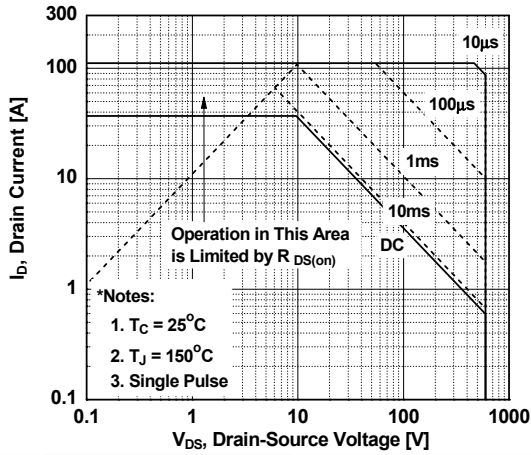
**Figure 7. Breakdown Voltage Variation vs. Temperature**



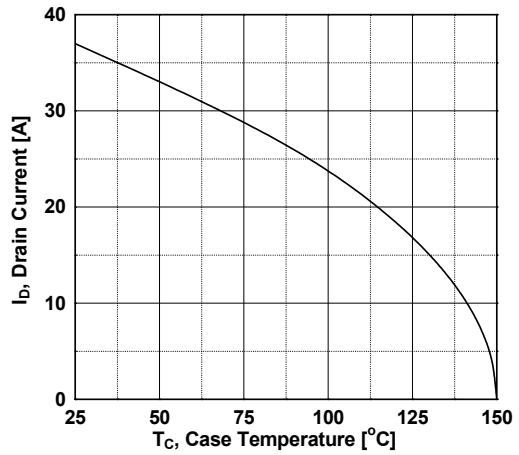
**Figure 8. On-Resistance Variation vs. Temperature**



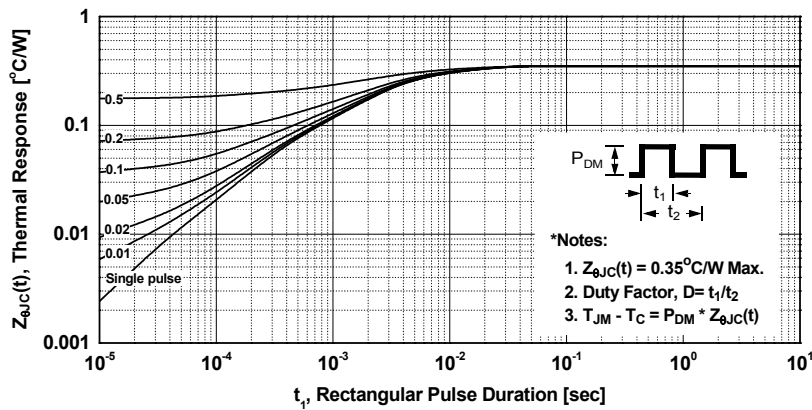
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**



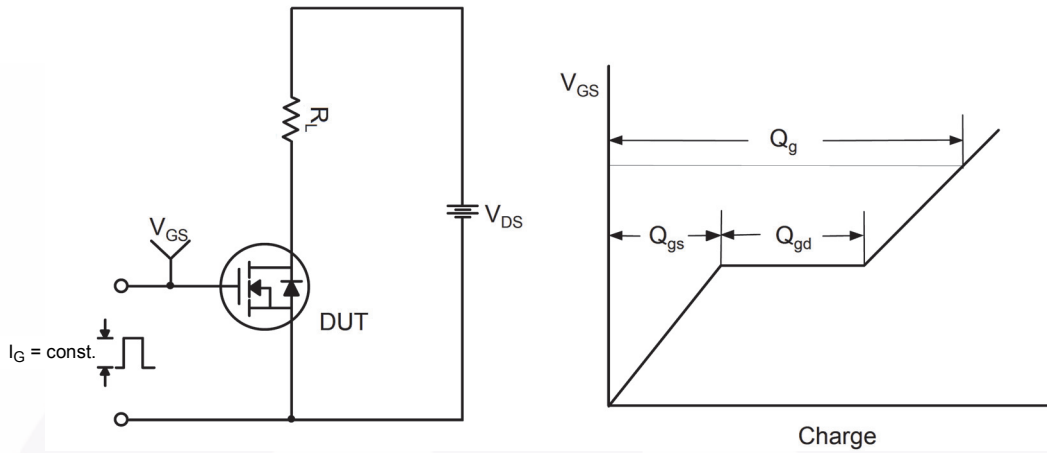


Figure 12. Gate Charge Test Circuit & Waveform

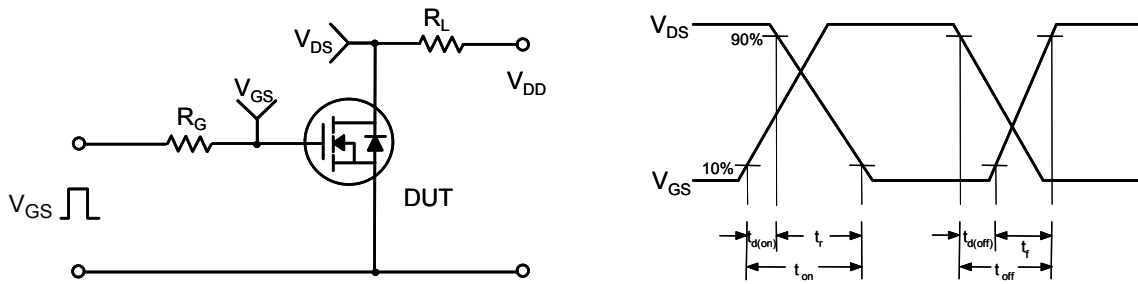


Figure 13. Resistive Switching Test Circuit & Waveforms

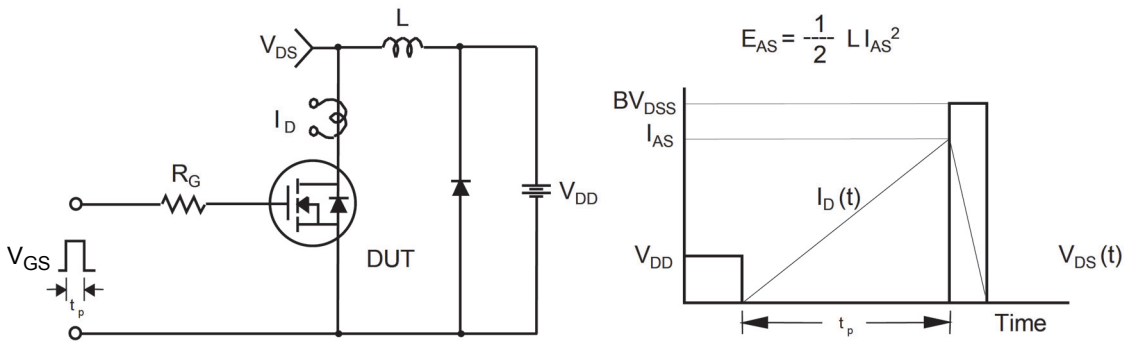


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

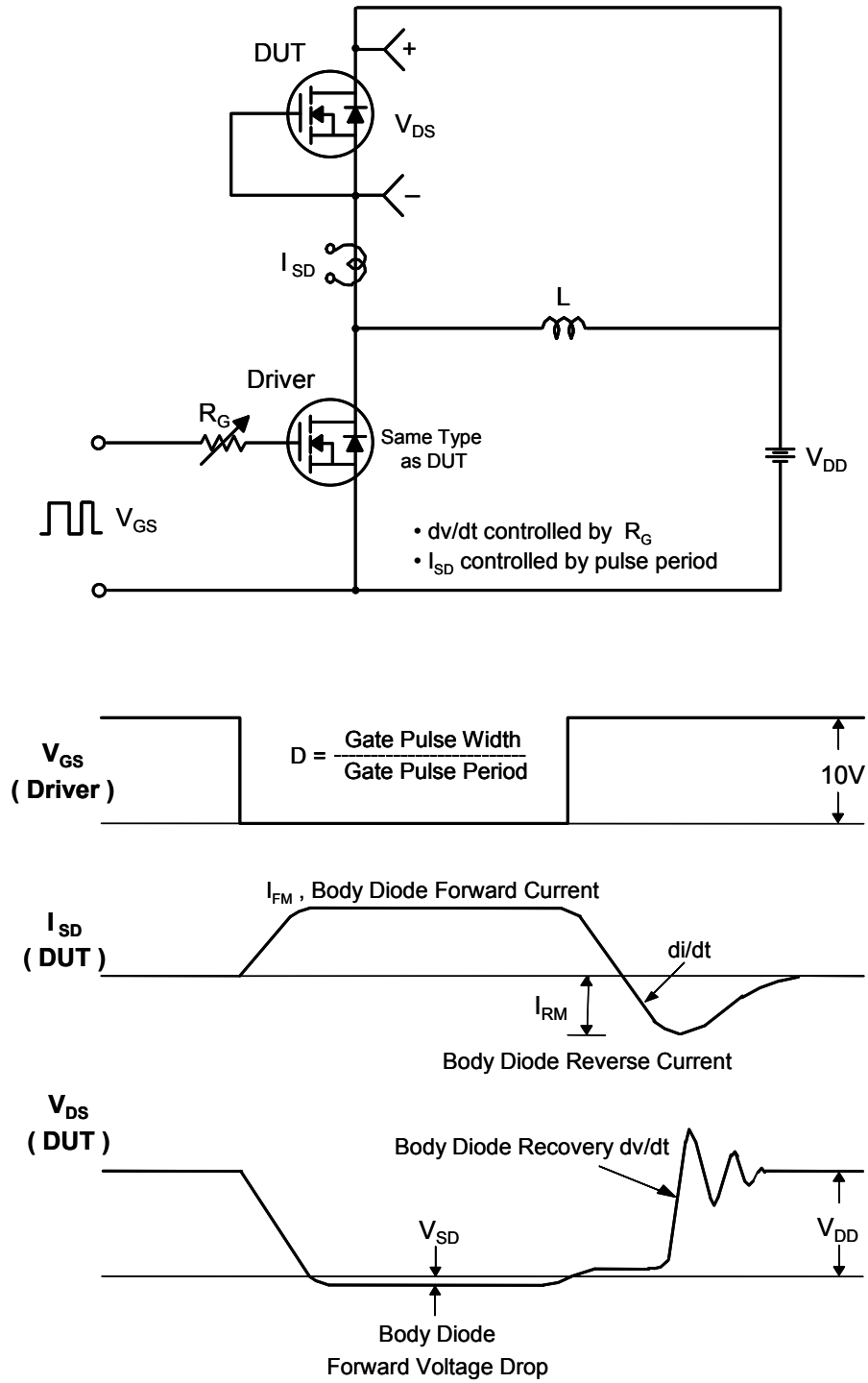
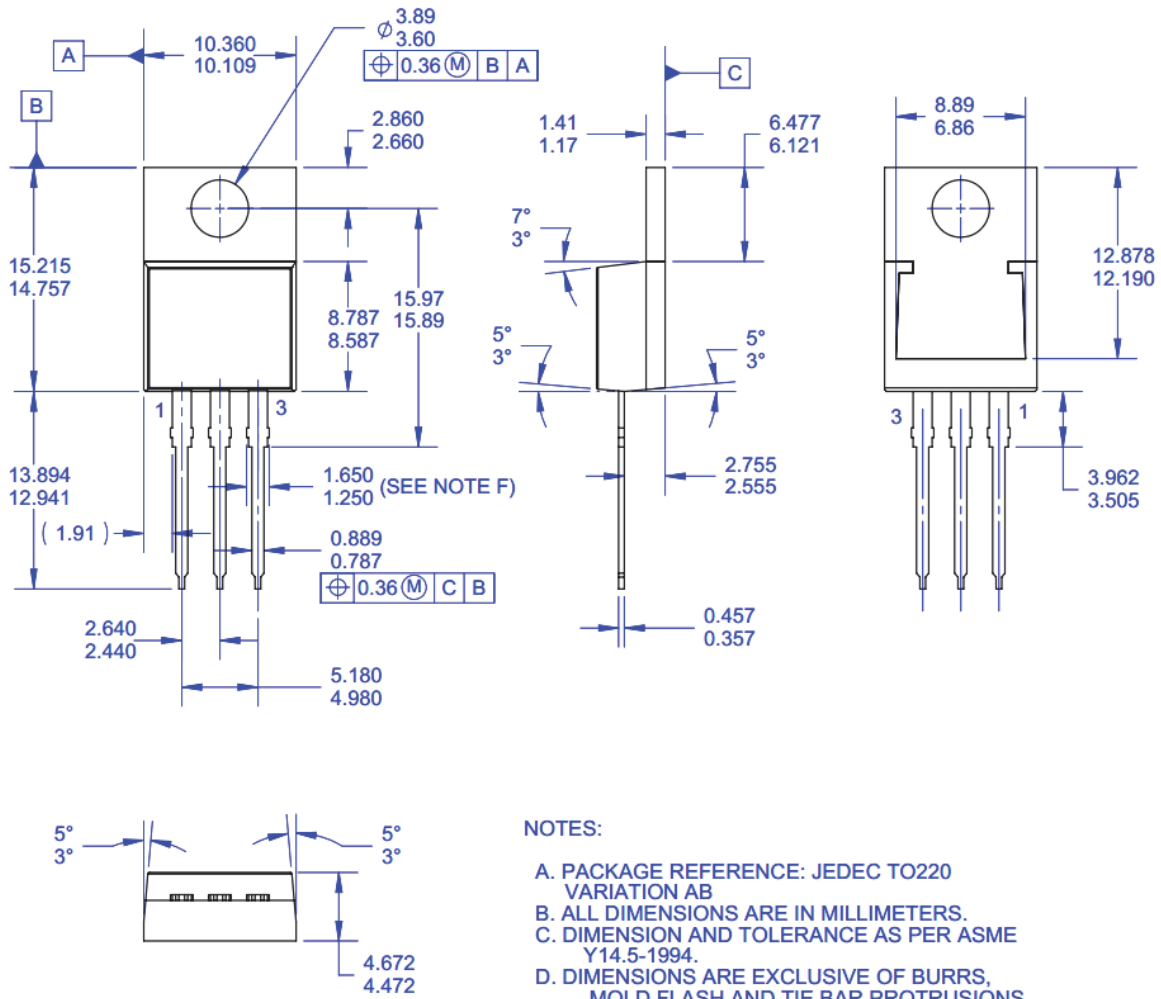


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

**Mechanical Dimensions**



**Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)**

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