Evaluation Board User Guide
UG-043

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*i*Coupler ADuM4160 USB Isolator Evaluation Board

INTRODUCTION

USB use has displaced older communications standards, such as RS-232, as the default serial communications port in PC-based systems. When compared to these other standards, USB has many enhanced features, such as power for peripherals, automatic driver installation, and higher data rates. However, when using USB, it is difficult to provide isolation, which has limited its acceptance in medical and industrial applications.

Analog Devices, Inc., has introduced the ADuM4160 USB isolator to address the difficult task of isolating the bus. The ADuM4160 USB isolator evaluation board was constructed to allow an easy interface to existing applications by standard cabling or discrete wiring.

The design goals of this evaluation platform are to

- Connect to systems through standard USB Type A and Type B connectors.
- Draw power from the USB host or from an external 5.0 V or 3.3 V power supply.
- Support isolated power for the downstream interface through an ADuM5000 *iso*Power® dc-to-dc converter.
- Support external downstream power from a 5 V or 3.3 V power supply.
- Provide test points for all power and signal paths.
- Support low and full speed communications.
- Support enumeration control.
- Support external ESD protection.
- Support common-mode chokes in xD+/xD−.
- Support ferrite inductors in V_{BUSx} and GND_x lines.

FEATURES OF THE ADuM4160

The ADuM4160 provides support for full speed and low speed data communications by interfacing directly with the xD+ and xD− lines. It is designed to be transparent to USB data traffic other than adding about as much delay as a hub and cable. Features of the isolator include the following:

- Built-in voltage regulators allow the ADuM4160 to draw power from either 5 V or 3.3 V sources.
- Application of the upstream pull-up resistor is under the control of a downstream pin, PIN (Pin 12).
- The operating speed of the isolator is set by pins on the upstream and downstream sides of the part, SPU and SPD (Pin 5 and Pin 13, respectively).

The upstream side of the ADuM4160 is Pin 1 through Pin 8, is connected to the left-hand side of the evaluation board, and interfaces through a Type B connector. The downstream facing side is Pin 9 through Pin 16, is connected to the right-hand side of the evaluation board, and interfaces through a Type A connector.

The evaluation board allows configuration of all of the features of the ADuM4160 chip as well as providing support for a variety of possible power schemes. The board also allows common-mode voltages; however, it is not recommended for performing safety related testing, such as high voltage withstand testing. Perform this type of testing on the component level or on a production board.

EVALUATION BOARD

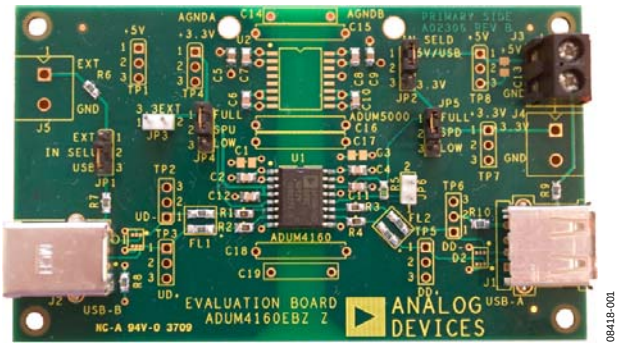

Figure 1. USB Evaluation Board

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REVISION HISTORY

2/10—Revision 0: Initial Version

POWER

UPSTREAM SIDE

The USB standard requires that the upstream facing port of a peripheral device derive power for its pull-up from the 5 V present on the cable. Power can also be used to power functions in the peripheral at up to 500 mA.

The ADuM4160 contains an internal voltage regulator that can derive the 3.3 V from V_{BUSx} for use in the data transmission and pull-up power. It also provides the user with the ability to bypass this regulator if a 3.3 V supply can be provided by the user. The evaluation board can choose to source its power from the cable at 5 V or from an external supply connected to terminal block J5, labeled EXT. Jumper JP1 selects between the two sources. When the external power is chosen, the ADuM4160 can be configured to accept either 3.3 V or 5 V from that source. If 3.3 V is supplied, then the internal regulator must be disabled by shorting Pin 1 and Pin 3 together. This is accomplished by placing a shunt across JP3, labeled 3.3EXT. This jumper should be open when the USB bus is the source of power.

Table 1. Upstream Power Jumper Settings

	Jumper Settings	
Power Source	**IN SELU (JP1)**	**3.3EXT (JP3)**
USB bus	USB (2 and 3)	Open
EXT 5.0 V	EXT (1 and 2)	Open
EXT 3.3 V	EXT (1 and 2)	Short

DOWNSTREAM SIDE

The USB standard does not allow any power to be sourced from a peripheral port. Power to run the downstream side of the ADuM4160 cannot come from the cable connection as it did on the upstream facing side. If the ADuM4160 is built into a peripheral device, it can receive power directly from the power supply of the peripheral. If the ADuM4160 is not built into the peripheral that it is protecting, then power must be provided from an external source or derived from the upstream bus power through a dc-to-dc converter. All of these possible power configurations are addressed in the evaluation board.

Power for the downstream port can be provided from external power supply connections through Terminal Block J3 and Terminal Block J4 or from the upstream USB power bus through an ADuM5000 *iso*Power dc-to-dc module that can be ordered separately. To make the board design robust and as simple as possible, only one method of powering the board can be used. The evaluation board comes configured to accept an external 5 V supply. If the downstream port is powered from the peripheral or an external supply, an ADuM5000 should not be installed.

The ADuM5000 is only capable of providing 100 mA of power to the downstream side. Applications that require more power at the downstream port must use the external power option. The ADuM5000 has been provided for the convenience of the user, and its use in final applications should be reviewed based on its data sheet precautions for power consumption and EMI mitigation.

Configuration of the downstream power is accomplished by installing or uninstalling the ADuM5000 converter, applying power to J3 or J4, and setting the appropriate jumper.

As with the upstream side of the ADuM4160, there is an internal regulator that derives the 3.3 V supply for the xD+ and the xD− signal lines from a 5 V source applied to V_{BUS2}. In addition, if V_{BUS2} and V_{DD2} are connected together to a 3.3 V source, the regulator is bypassed, and the voltage is used directly by the chip. The IN SELD (JP2) jumper selects between getting power from a 5 V source and a 3.3 V source. The 5 V source can either be an external voltage applied to J3 or an ADuM5000. The only 3.3 V source is the terminal block J4. If external power is used, the ADuM5000 must not be installed on the board.

Table 2. Downstream Power Jumper Settings

	Jumper Settings/Components	
Power Source	**IN SELD (JP3)**	**ADuM5000**
USB bus	5 V/USB	Installed
5 V (J3)	5 V/USB	Not Installed
3.3 V (J4)	3.3 V	Not Installed

GROUNDING SCHEME

The board consists of two separate ground and power systems. In addition, there is a floating capacitive structure on the bottom layer of the PCB that provides for EMI mitigation for the ADuM5000 dc-to-dc converter. This structure consists of a floating plane on each side of the isolation boundary. To allow evaluation of different EMI mitigation schemes, the planes can be for example

- Left floating which has a minimal effect on EMI.
- Connected by adding a strip of copper tape and soldering it to the exposed pads.
- Connected by safety capacitors installed in through-hole positions, C14 and C19.

In addition, the ground and power planes can be capacitively linked via C15 to C18 at the user's option. This can provide plane-to-plane noise bypassing through several paths to reduce radiated emissions from the ADuM5000 power supply.

There are two large screw holes along the top edge of the PCB that provide connection to the upstream ground plane and the downstream ground plane. These are provided to allow grounding of the PCB to the system in multiple configurations. The floating planes are designed with 0.4 mm of setback to all vias and other board planes. The PCB should not be used for high voltage testing if the floating structures are employed for noise reduction. If this type of structure is required in a final design, it should be built on an inner layer of the PCB to avoid creepage and clearance issues.

SPEED SELECTION

The ADuM4160 works at a fixed USB transmission speed, either low speed or full speed. The speed is set by the SPU and SPD pins on the upstream and downstream sides of the part and must be set by jumpers on the evaluation board. Both speed jumpers must be set to the same speed setting for proper operation.

Table 3. Speed Selection Jumpers

SPU (JP4)	SPD (JP5)	Speed
Short SPU-Full	Short SPD-Full	Full (12 Mbps)
Short SPU-Low	Short SPD-Low	Low (1.5 Mbps)

PULL-UP CONTROL

The PIN pin is provided to allow the control of enumeration and disconnect by the peripheral. When PIN is logic high, the pull-up on the upstream side of the ADuM4160 is applied to the data line appropriate for the USB speed mode. This allows enumeration and data transmission. When PIN is logic low, the upstream pull-up is disconnected, making the upstream port behave as though the port was not present.

This function is provided to allow the peripheral to delay communication with the host by delaying application of the upstream pull-up resistor until it is ready to be enumerated on the bus. If this functionality is not required, then PIN can be tied to V_{DD2}, and the pull-up is applied to the upstream side when power is applied to both the downstream power supplies.

Control of PIN is provided through Jumper JP6. The PIN input is pulled high by a 10 kΩ resistor. When a shunt is placed across JP6, it is pulled low. This provides a default state of high to PIN, allowing immediate enumeration.

Table 4. PIN Pull-Up Control

PIN (JP5)	Upstream Pull-Up State
Short	Disconnected
Open	Connected

SERIES RESISTORS

The two USB speeds supported by the ADuM4160 require different series resistance values at the transceiver terminals.

For full speed operation, Resistor R1 to Resistor R4 should be populated with 24 Ω, 1% resistors. These are installed in the base configuration of the evaluation board, and if the board is operated at full speed, no changes are required.

For low speed operation, R1 to R4 should be replaced by 0 Ω shunts. If the board is operated at a low speed, it must be modified from the as-received configuration. The shunt can be an 805-size SMT device or a simple wire shorting the pads. The resistors do not significantly affect the low speed performance and may be left in place for both speed modes, if impedance is not critical to the evaluation.

TEST POINTS

Positions for eight test points are included on the evaluation board. No headers are provided in the default configuration. Mounting holes for a ground signal pair are provided. The holes fit a standard square-pin spaced at 100 mil or 200 mil on center. This configuration was chosen to match the dimensions of the Tektronix high frequency active probes or standard headers. An appropriate scope header can be obtained by using 3-pin SIP wire wrap header and removing the center pin. The signal pin can be trimmed to match the spacing of the probe. If another type of connection is required, wires can be inserted into the holes provided for these connections.

OPTIONAL COMPONENTS

Options for installing common-mode chokes and external ESD protection on the DD+/DD− and UD+/UD− data lines are also available. Positions for TDK ACM3225 chokes are provided at Position FL1 and Position FL2. Positions for ESD diode packs, NUP2202 from ON Semiconductor, are provided at Position D1 and Position D2. In addition, pads for surface-mount ferrite inductors are provided at Position R6 to Position R10. All of these component positions are either unpopulated or filled with 0 Ω resistors from Analog Devices. They are on the PCB as a convenience to the end user.

EVALUATION BOARD SCHEMATIC AND ARTWORK

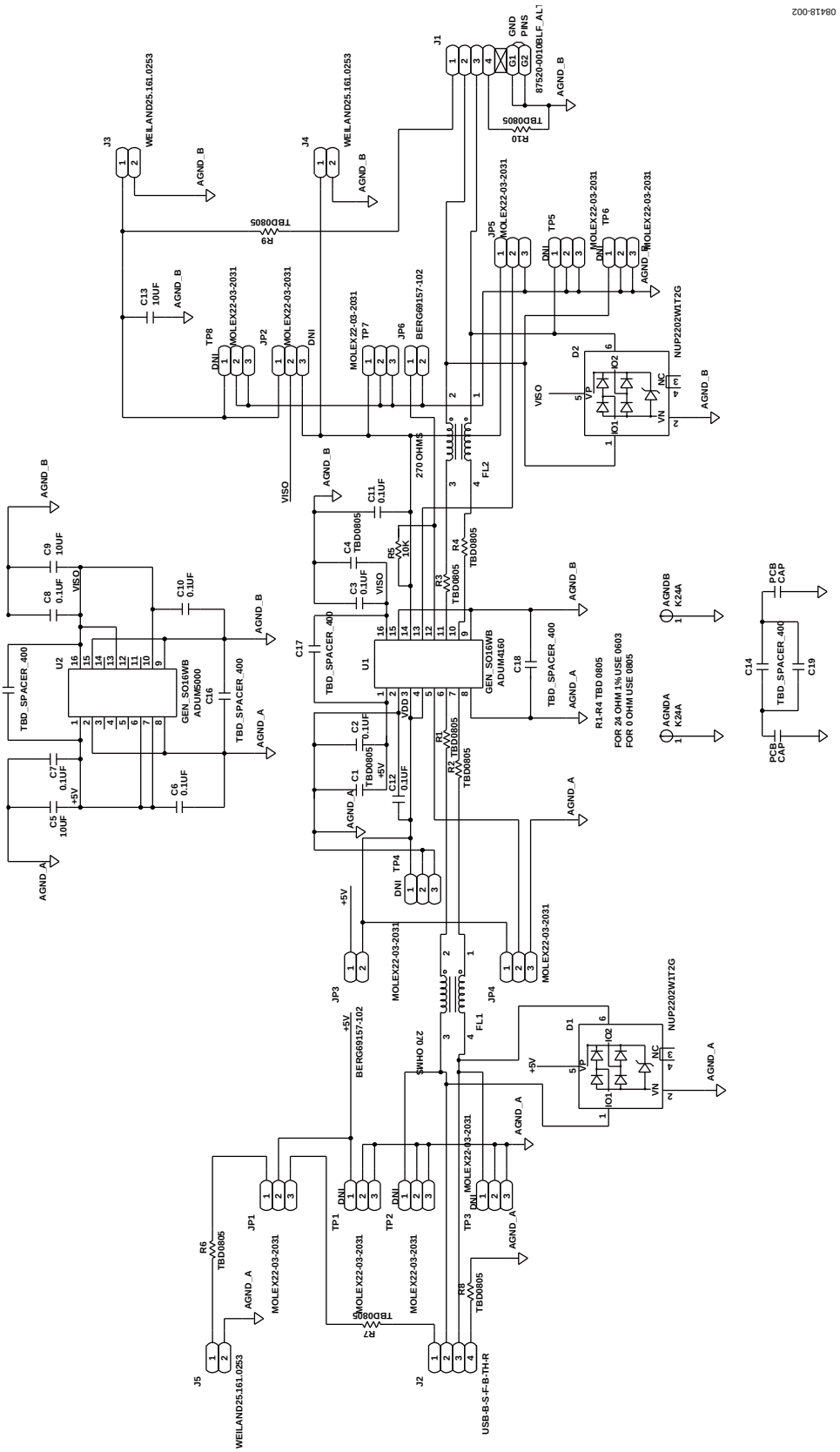

Figure 2. Evaluation Board Schematic

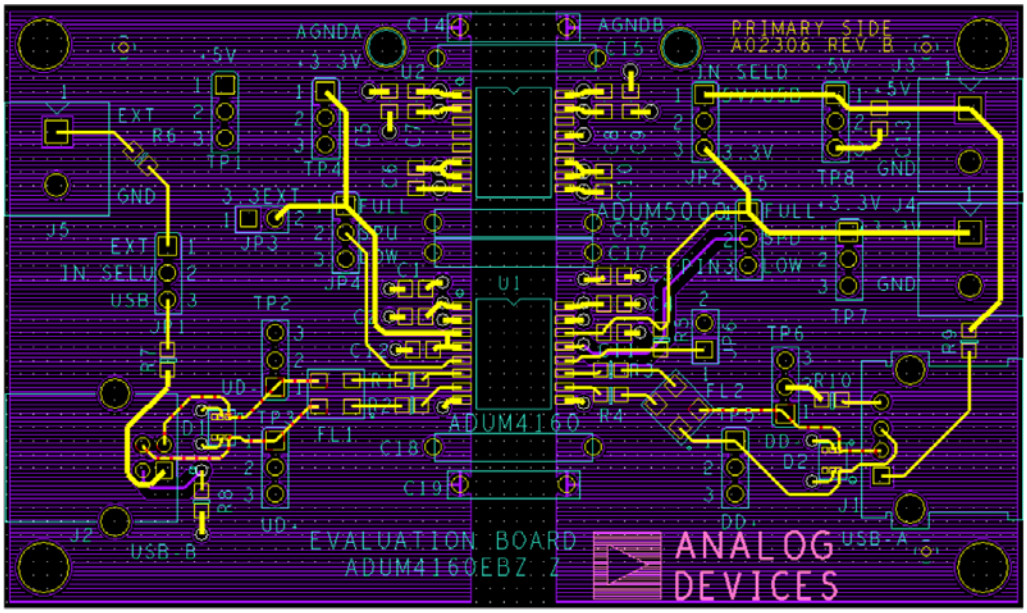

Figure 3. Evaluation Board Artwork

NOTES

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ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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