ESM-2545 Series

AMD Geode GX3 ETX Module

User's Manual

2nd Ed – 15 August 2007

Part No. E2047254500R

FCC Statement

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

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To receive the latest version of the user's manual; please visit our Web site at:
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In addition, free technical support is available from Avalue's engineers every business day. We are always ready to give advice on application requirements or specific information on the installation and operation of any of our products. Please do not hesitate to call or e-mail us.

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Contents

1. Getting Started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ESM-2545 AMD Geode GX3 ETX Module
- 1 x Quick Installation Guide
- 1 x DVD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities

If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	By	Comment
1st	May 2006	Jason Liu	Initial Release
	Feb 2007	Lingo Tsai	Logo Changed & Specification Modified
2nd	Aug. 2007	Lingo Tsai	-System modification -Remove BIASON from section 2.4.7.2 -Modify PIN4 of ETX 4 from PWGIN to NC of section 2.4.8 -Modify PIN7 of ETX 4 from NC to PWRBTN# of section 2.4.8 -Modify PIN90 of ETX 4 from NC to CBLID_P# of section 2.4.8 -Add the signal description for BATT, I2C_DAT, I2C_CLK of section 2.4.9
	Aug. 2009	Hsin Chiang	Update BIOS set up

1.4 Manual Objectives

This manual describes in detail the Avalue Technology ESM-2545 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ESM-2545 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

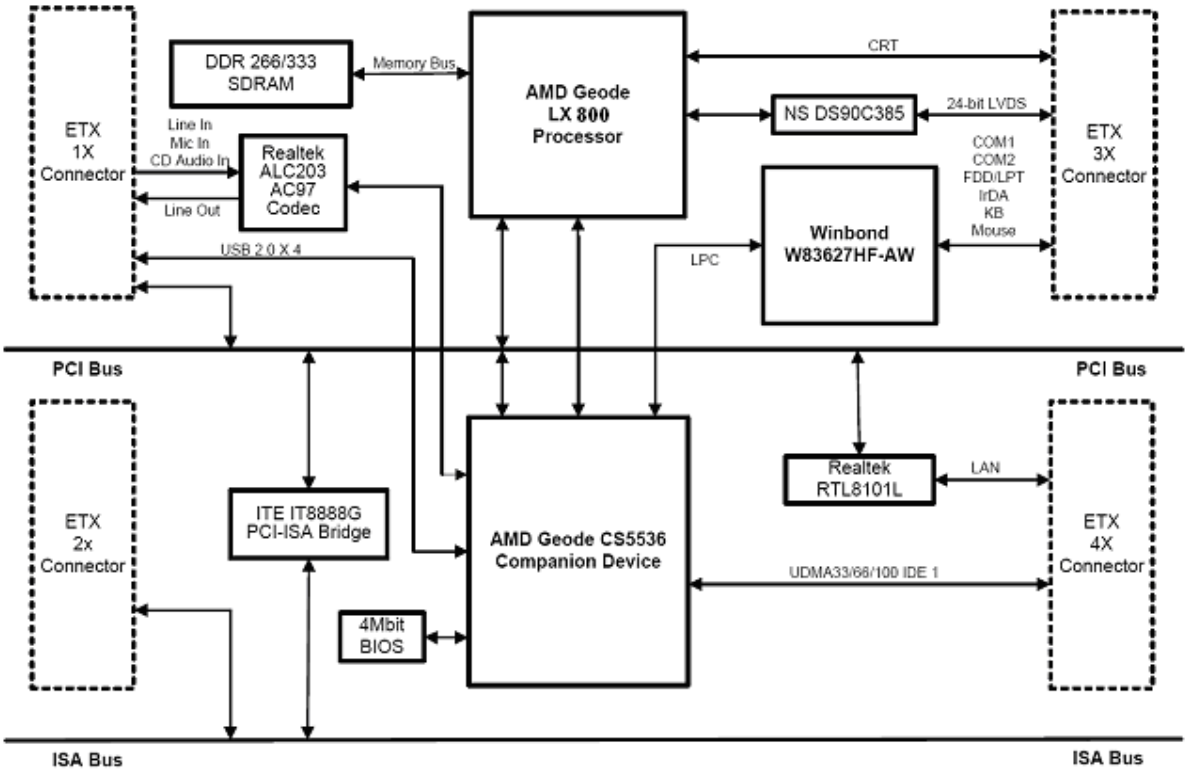
1.5 System Specifications

System	
CPU	Onboard AMD Geode LX800 @ 0.9 W with 128K L2 Cache
BIOS	Award 512 KB Flash BIOS
System Chipset	AMD Geode LX800/CS5536
I/O Chip	Winbond W83627HG-AW
System Memory	One 200-pin SODIMM socket supports up to 1 GB DDR 266/333/400 SDRAM
Watchdog Timer	Reset: 1 sec.~255 min. and 1 sec. or 1 min./step
Hardware Status Monitor	Monitoring CPU temperature and voltage
Expansion	Four PCI bus, four ISA bus
I/O	
MIO	1 x EIDE (Ultra DMA 100), 1 x FDD/LPT, 2 x RS-232, 1 x K/B & Mouse
IrDA	115k bps, IrDA 1.0 compliant
USB	4 x USB 2.0 ports
Display	
Chipset	AMD Geode LX800 with integrated graphics engine
Resolution	CRT mode: 1920 x 1440 @ 32 bpp (85 Hz) TFT mode: 1600 x 1200 @ 32 bpp (60Hz)
LVDS	Single channel 18-bit LVDS
Audio	
Chipset	AMD Geode CS5536
AC97 Codec	Realtek ALC203 supports 2 CH Audio
Audio Interface	Mic in, Line in, CD Audio in, Line out
Ethernet	
LAN	Realtek RTL8101L
Ethernet Interface	100Base-Tx Fast Ethernet compatible
Mechanical & Environmental	
Power Requirement	+5 V @ 2.02 A, 5 Vsb @ 0.08 A (With AMD LX800 500 MHz & 256 MB DDR 333 SDRAM)
Power Type	ATX
Operation Temperature	0~60°C (32~140° F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	5" x 3.7" (125 mm x 95 mm)
Weight	0.22 lbs (0.1 Kg)

1.6 Architecture Overview

1.6.1 Block Diagram

The following block diagram shows the architecture and main components of ESM-2545.



The following sections provide detail information about the functions provided onboard.

1.6.2 AMD Geode GX3 & CS5536

The AMD Geode™ GX3 processors are integrated x86 processors specifically designed to power embedded devices for entertainment, education, and business. Serving the needs of consumers and business professionals alike, it's an excellent solution for embedded applications, such as thin clients, interactive set-top boxes, single board computers, and mobile computing devices.

LX Processor General Features:

- 0.13 micron process
- 481-Terminal BGU (Ball Grid Array Cavity Up) with internal heatspreader
- x86/x87-compatible CPU core
- Processor frequency: up to 500 MHz
- Dhrystone 2.1 MIPs: 150 to 450
- Split I/D cache/TLB (Translation Look-aside Buffer):
  - 64 KB I-cache/64 KB D-cache
  - 128 KB L2 cache configurable as I-cache, D-cache, or both
- Efficient pre-fetch and branch prediction
- Integrated FPU that supports the MMX® and
- AMD 3DNow!™ instruction sets
- Fully pipelined single precision FPU hardware with microcode support for higher precisions
- JTAG interface:
  - ATPG, Full Scan, BIST on all arrays
  - 1149.1 Boundary Scan compliant
- ICE (in-circuit emulator) interface
- Reset and clock control
- Designed for improved software debug methods and performance analysis
- Power Management:
  - Thermal Design Power (TDP) 2.4W, 1.6W typical @ 500 MHz max power (projected)
  - GeodeLink active hardware power management
  - Hardware support for standard ACPI software power management
  - I/O companion SUSP/SUSPA power controls
  - Lower power I/O
  - Wakeup on SMI/INTR

GeodeLink™ Memory Controller

- High bandwidth packetized uni-directional bus for internal peripherals
- Standardized protocol to allow variants of products to be developed by adding or removing modules
- GeodeLink Control Processor (GLCP) for diagnostics and scan control
- Dual GeodeLink Interface Units (GLIUs) for device interconnect

GeodeLink™ Memory Controller

- Integrated memory controller for low latency to CPU and on-chip peripherals
- 64-bit wide DDR SDRAM bus operating frequency:
  - 200 MHz, 400 MT/S
- Supports unbuffered DDR DIMMS using up to 1 GB
- DRAM technology
- Supports up to 2 DIMMS (32 devices max)

2D Graphics Processor

- High performance 2D graphics controller
- Alpha BLT
- Microsoft® Windows® GDI GUI acceleration:
  - Hardware support for all Microsoft RDP codes
- Command buffer interface for asynchronous BLTs
- Second pattern channel support
- Hardware screen rotation

Display Controller

- Hardware frame buffer compression improves Unified
- Memory Architecture (UMA) memory efficiency
- CRT resolutions supported:
  - Supports up to 1920x1440x32 bpp at 85 Hz
  - Supports up to 1600x1200x32 bpp at 100 Hz
- Supports up to 1600x1200x32 bpp at 60 Hz for TFT
- Standard Definition (SD) resolution for Video Output Port (VOP):
  - 720x482 at 59.94 Hz interlaced for NTSC
  - 768x576 at 50 Hz interlaced for PAL
- High Definition (HD) resolution for Video Output Port (VOP):
  - Up to 1920x1080 at 30 Hz interlaced (1080i HD) (74.25 MHz)
  - Up to 1280x720 at 60 Hz progressive (720p HD) (74.25 MHz)
- Supports down to 7.652 MHz Dot Clock (320x240 QVGA)
- Hardware VGA
- Hardware supported 48x64 32-bit cursor with alpha blending

Video Processor

- Supports video scaling, mixing and VOP
- Hardware video up/down scalar
- Graphics/video alpha blending and color key muxing
- Digital VOP (SD and HD) or TFT outputs
- Legacy RGB mode
- VOP supports SD and HD 480p, 480i, 720p, and 1080i
- VESA 1.1, 2.0 and BT.601 24-bit (out only), BT.656 compliant

GeodeLink™ PCI Bridge

- PCI 2.2 compliant
- 3.3V signaling and 3.3V I/Os
- 33 to 66 MHz operation
- 32-bit interface
- Supports virtual PCI headers for GeodeLink devices

Video Input Port (VIP)

- VESA 1.1 and 2.0 compliant, 8 or 16-bit
- Video Blanking Interval (VBI) support
- 8 or 16-bit 80 MHz SD or HD capable
- Security Block
- Serial EEPROM interface for 2K bit unique ID and AES
- (Advanced Encryption Standard) hidden key storage
- (EEPROM optional inside package)
- Electronic Code Book (ECB) or Cipher Block Chaining (CBC)128-bit AES hardware support
- True random number generator (TRNG)

The AMD Geode™ CS5536 companion device is designed to work with an integrated processor North Bridge component such as the AMD Geode™ LX processor. Together, the Geode LX processor and Geode CS5536 companion device provide a system-level solution well suited for the high-performance and low-power needs of a host of embedded devices including digital set-top boxes, mobile computing devices, thin client applications, and single board computers.

The internal architecture uses a single, high-performance modular structure based on GeodeLink™ architecture. This architecture yields high internal speed (over 4 GB/s) data movement and extremely versatile internal power management. The GeodeLink architecture is transparent to application software. Communication with the Geode Geode LX processor is over a 33/66 MHz PCI bus.

The Geode CS5536 companion device incorporates many I/O functions, including some found in typical superI/O chips, simplifying many system designs. Since the graphics subsystem is entirely contained in the Geode GX3 processor, system interconnect is simplified. The device contains state-of-the-art power management that enables systems, especially battery powered systems, to significantly reduce power consumption.

Audio is supported by an internal controller, designed to connect to multiple AC97 compatible codecs. An IR (infrared) port supports all popular IR communication protocols.

The IR port is shared with one of two industry-standard serial ports that can reach speeds of 115.2 kbps. An LPC (low pin count) port is provided to facilitate connections to a superI/O should additional expansion, such as a floppy drive, be necessary, and/or to an LPC ROM for the system BIOS.

The hard disk controller is compatible to the ATA-6 specification. The bus mastering IDE controller includes support for two ATA-compliant devices on one channel. The CS5536 companion device provides four Universal Serial Bus (USB) 2.0 compliant ports, supporting low speed, full speed, and high speed connections. All four ports are individually automatically associated with either the Open Host Controller Interface (OHCI) or the Enhanced Host Controller Interface (EHCI) depending on the attached device type. A battery-backed real-time clock (RTC) keeps track of time and provides calendar functions.

A suite of 82xx devices provides the legacy PC functionality required by most designs, including two PICs (programmable interrupt controllers), one PIT (programmable interval timer) with three channels, and DMA (direct memory access) functions. The CS5536 companion device contains eight MFGPTs (multi-function general purpose timers) that can be used for a variety of functions. A number of GPIOs (general purpose input/outputs) are provided, and are assigned to system functions on power-up (i.e., LPC port).

State-of-the-art power management features are attained with the division of the device into two internal power domains. The GPIOs and multi-function timers are distributed into each domain allowing them to act as wakeup sources for the device. The device provides full ACPI (Advanced Configuration Power Interface) compliance and supports industry-standard Wakeup and Sleep modes.

For implementation details and suggestions for this device, see the supporting documentation (i.e., application notes, schematics, etc.) on the AMD Alchemy™ and Geode™ Developer Support web site.

1.6.3 Realtek ALC203 Audio Codec

The ALC203 is a 20-bit DAC and 18-bit ADC full-duplex AC'97 2.3 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio, and AMR/CNR based designs.

The ALC203 incorporates proprietary converter technology to achieve a high SNR (greater than 100 dB), sensing logics for device reporting, and a Universal Audio Jack® for improved user convenience. The ALC203 AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC203 CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, multiple stereo and mono inputs, along with flexible mixing, gain, and mute functions to provide a complete integrated audio solution for PCs.

The circuitry of the ALC203 CODEC operates from a 3.3V digital and 3.3V/5V analog power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. The ALC203 integrates a 50mW/20Ohm headset audio amplifier into the CODEC, saving BOM costs. The ALC203 also supports the S/PDIF out function (complies with AC'97 2.3) that offers easy connection of PCs to consumer electronic products, such as AC3 decoders/speakers and mini disk devices.

The ALC203 CODEC supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipsets. Bundled Windows series drivers (Win98/ME/NT/2000/XP, EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities (supporting Karaoke, 26-kinds of environment sound emulation, 10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. An internal 14.318MHz -> 24.576MHz PLL circuit generates required timing signals, eliminating the need for external crystal, whilst a built-in PCBEEP generator removes the need for an external buzzer.

1.6.4 Realtek RTL8101L Ethernet Controller

The Realtek RTL8101L is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-TX specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. The RTL8101L no longer supports CardBus mode as RTL8139C does.

In addition to the ACPI feature, the RTL8101L also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8101L is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8101L is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8101L LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality.

The RTL8101L also supports Analog Auto-Power-down, that is, the analog part of the RTL8101L can be shut down temporarily according to user requirements or when the RTL8101L is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8101L will be negligible. The RTL8101L also supports an auxiliary power auto-detect function, and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware (i.e., the OEM brand name of RTL8101L LAN card). The information may consist of part number, serial number, and other detailed information.

To provide cost down support, the RTL8101L is capable of using a 25MHz crystal or OSC as its internal clock source.

The RTL8101L keeps network maintenance costs low and eliminates usage barriers. It is the easiest way to upgrade a network from 10 to 100Mbps. It also supports full-duplex operation, making 200Mbps bandwidth possible at no additional cost. To improve compatibility with other brands' products, the RTL8101L is also capable of receiving packets with InterFrameGap no less than 40 Bit-Time. The RTL8101L is highly integrated and requires no "glue" logic or external memory.

The RTL8101L includes a PCI and Expansion Memory Share Interface (Realtek patent) for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management.

1.6.5 Winbond W83627HF-AW

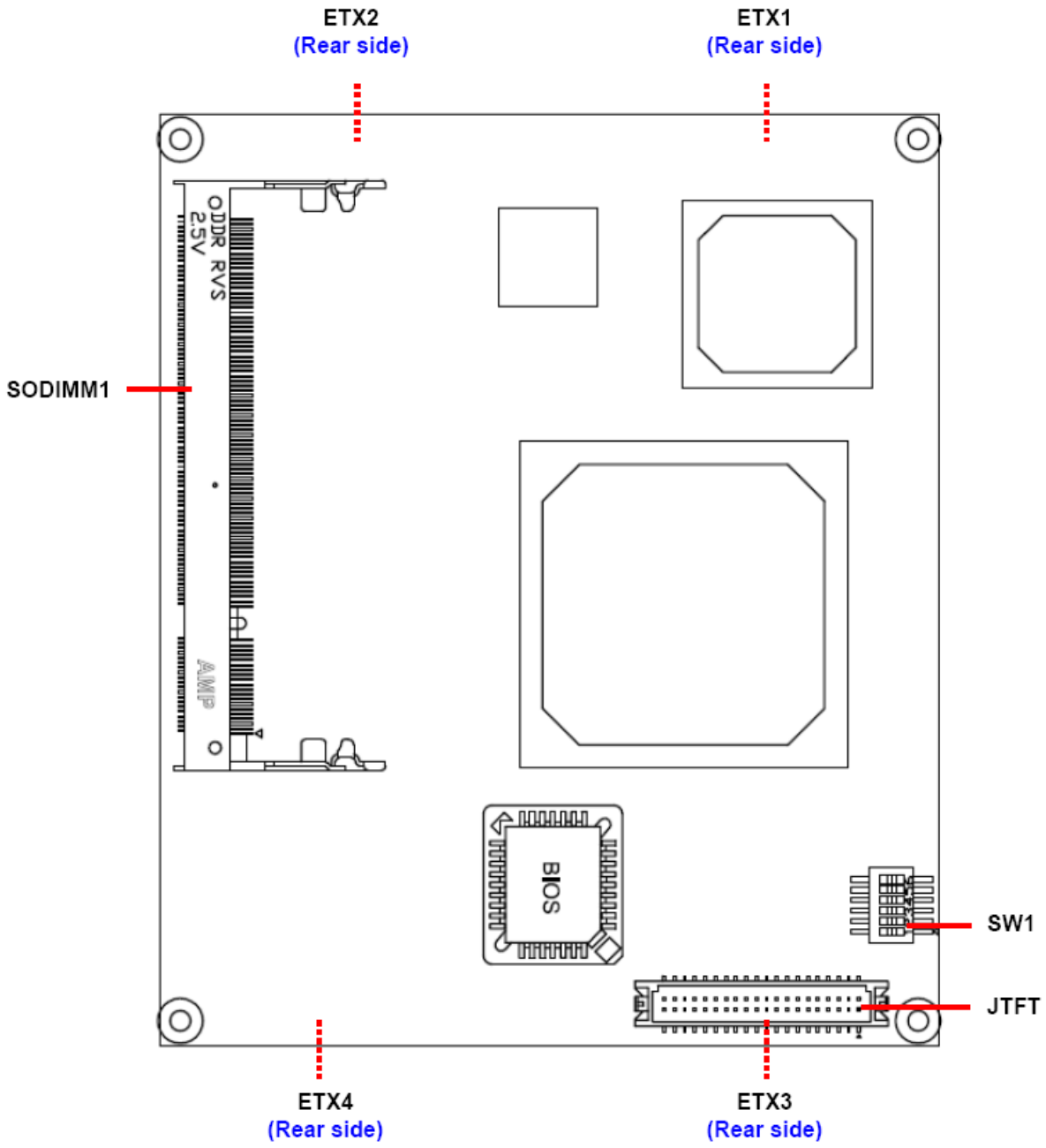
The W83627HF is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover W83627HG is made to meet the specification of PC98/PC99's requirement in the power management: ACPI and DPM (Device Power Management).
The W83627HF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.
Only the W83627HF support hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures, which are very important for a high-end computer system to work stably and properly.

1.6.6 ITE IT8888 PCI to ISA Bridge

The IT8888F/G is a PCI to ISA bridge single function device. The IT8888F/G serves as a bridge between the PCI bus and ISA bus. The IT8888F/G's 32-bit PCI bus interface is compliant with PCI Specification V2.1 and supports both PCI Bus Master & Slave. The PCI interface supports both programmable positive and full subtractive decoding schemes.
The IT8888F/G also integrates two enhanced DMA Slave controllers for achieving PCI DMA cycles: PC/PCI DMA Slave Controller & Distributed DMA Slave Controllers.
The device also contains one SM bus (single master mode) which can be connected to a Serial E2PROM for automatic power-on configuration. ITE's proprietary (USA & Taiwan patent pending) power-on auto-configuration through SM bus can provide customer with maximum design flexibility. The IT8888F/G also implements the optional fast positive decode of F, E, D, C memory segments. This special feature can provide a direct connection to an FALSH boot ROM.
The NOGO function, which is also implemented in the IT8888F/G for enabling or disabling subtractive decode of PCI interface could be a software controlled output pin from other host controlled devices. The Serial IRQ is also implemented in the device for sending and receiving ISA IRQs & IOCHCK#. The device includes an ISA interface which supports full ISA compatible functions.

2. Hardware Configuration

2.1 Product Overview



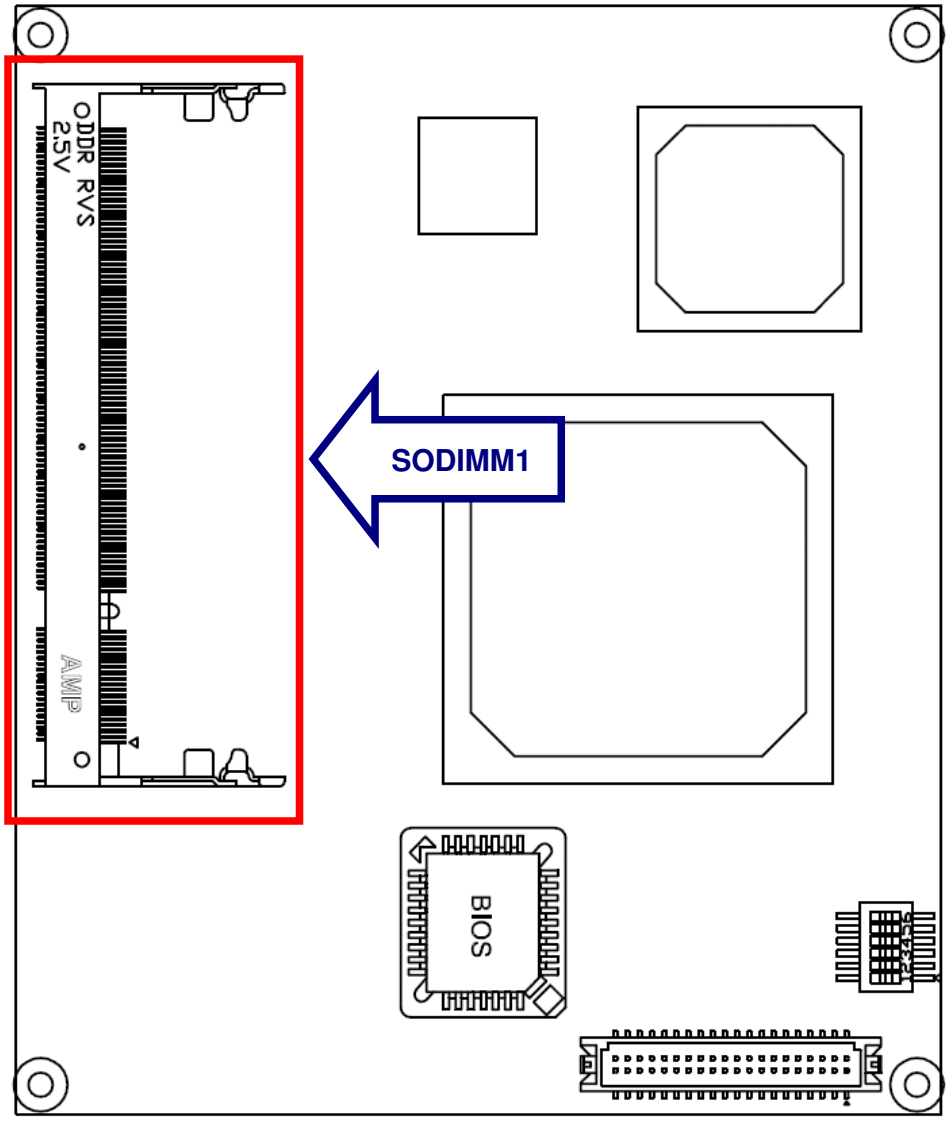
2.2 Installation Procedure

This chapter explains you the instructions of how to setup your system.

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the ATXPWR.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

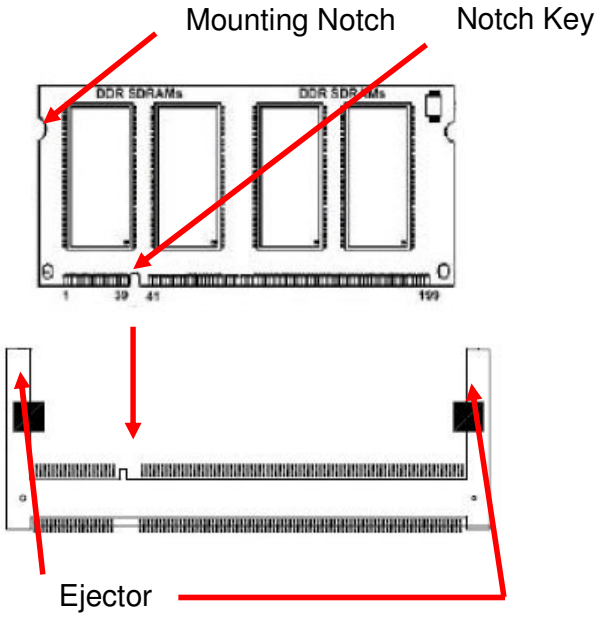
2.2.1 Main Memory

ESM-2545 provides one 200-pin SODIMM sockets to support DDR SDRAM. The total maximum memory size is 1 GB.



Make sure to unplug the power supply before adding or removing SODIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the DIMM socket on the board.
- Hold two edges of the DIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the socket automatically snaps into the mounting notch. Do not force the DIMM module in with extra force as the DIMM module only fit in one direction.



200-pin DDR DIMM

- To remove the DIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the DIMM module.

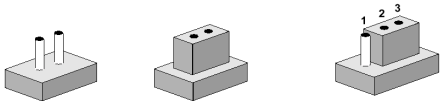
Note: (1) Please do not change any DDR SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

(2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



Open Closed Closed 2-3

The jumper settings are schematically depicted in this manual as follows:

Open Closed Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The following tables list the function of each of the board's jumpers and connectors.

Jumpers

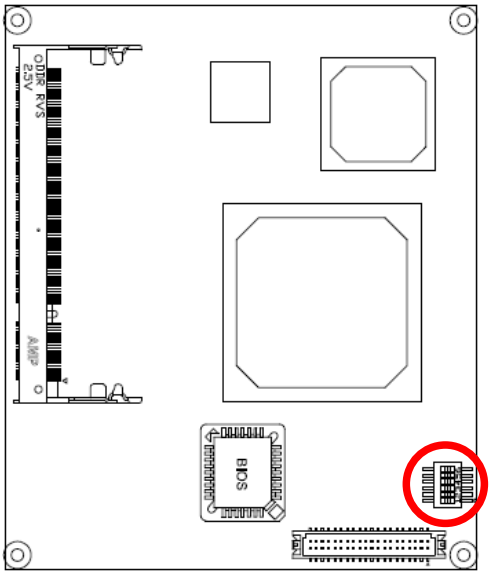
Label	Function	Note
SW1	CPU/Memory Frequency Select	Switch

Connectors

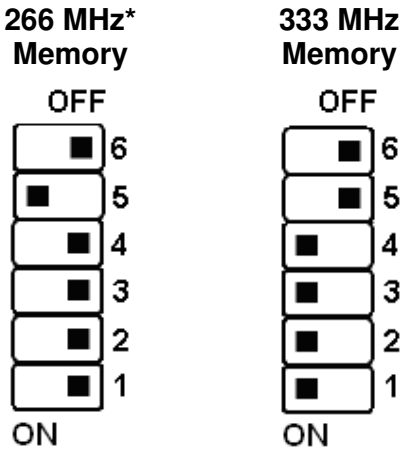
Label	Function	Note
ETX1	ETX connector X1	HIROSE FX8-100P-SV
ETX2	ETX connector X2	HIROSE FX8-100P-SV
ETX3	ETX connector X3	HIROSE FX8-100P-SV
ETX4	ETX connector X4	HIROSE FX8-100P-SV
JTFT	TFT panel connector	HIROSE DF-13-40DP-1.25V
SODIMM1	200-pin SODIMM socket	

2.4 Setting Jumpers & Connectors

2.4.1 CPU/Memory Frequency Select (SW1)

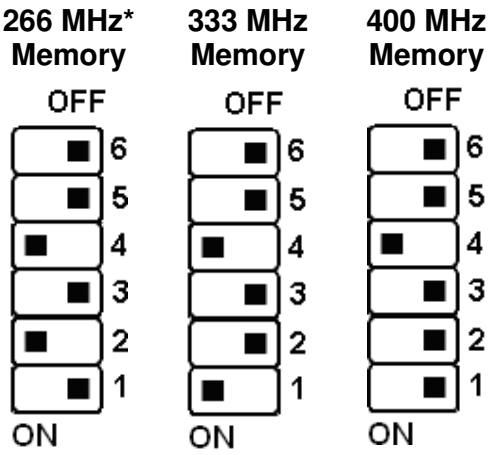


LX700
(CPU @ 433 MHz)

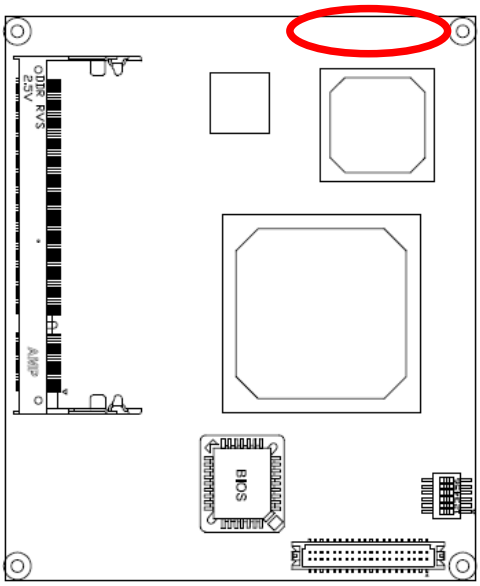


*** Default**

LX800
(CPU @ 500 MHz)



2.4.2 ETX Connecter X1 (ETX1)



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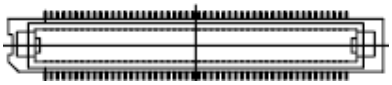
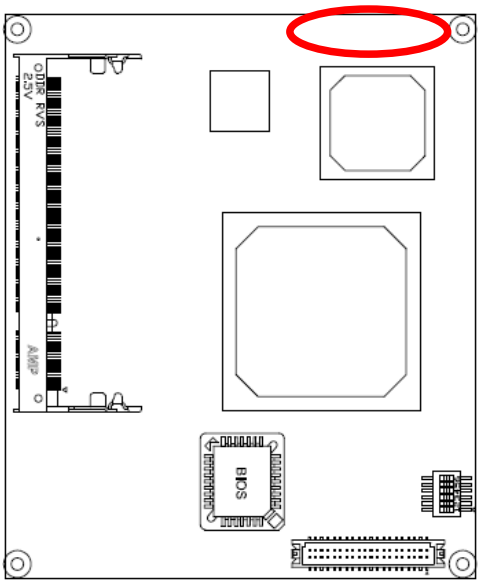


Signal	PIN	PIN	Signal
GND	1	2	GND
PCICLK3	3	4	PCICLK4
GND	5	6	GND
PCICLK1	7	8	PCICLK2
REQ3#	9	10	GNT3#
GNT2#	11	12	NC
REQ2#	13	14	GTN1#
REQ1#	15	16	NC
GNT0#	17	18	NC
+5V	19	20	+5V
SERIRQ	21	22	REQ0#
AD0	23	24	NC
AD1	25	26	AD2
AD4	27	28	AD3
AD6	29	30	AD5
CBE0#	31	32	AD7
AD8	33	34	AD9
GND	35	36	GND
AD10	37	38	AUXAL
AD11	39	40	MIC
AD12	41	42	AUXAR
AD13	43	44	ASVCC
AD14	45	46	SNDL
AD15	47	48	GND
CBE1#	49	50	SNDR



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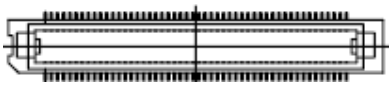


Signal	PIN	PIN	Signal
+5V	51	52	+5V
PAR	53	54	SERR#
GPERR#	55	56	NC
PME#	57	58	USB2#
LOCK#	59	60	DEVSEL#
TRDY#	61	62	USB3#
IRDY#	63	64	STOP#
FRAME#	65	66	USB2
GND	67	68	GND
AD16	69	70	CBE2#
AD17	71	72	USB3
AD19	73	74	AD18
AD20	75	76	USB0#
AD22	77	78	AD21
AD23	79	80	USB1#
AD24	81	82	CBE3#
+5V	83	84	+5V
AD25	85	86	AD26
AD28	87	88	USB0
AD27	89	90	AD29
AD30	91	92	USB1
PCIRST#	93	94	AD31
INTC#	95	96	INTD#
INTA#	97	98	INTB#
GND	99	100	GND

2.4.3 Signal Description – ETX Connecter X1 (ETX1)

2.4.3.1 PCI Signals

Signal	Signal Description
PCICLK [1:4]	PCI clock outputs for up to 4 external PCI slots or devices. The baseboard designer should route these clocks for 1300pS total delay from the ETX connector pin to the clock pin of the PCI device. See the ETX Design Guide for typical route length calculations.
REQ [0:3]#	Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.
GNT [0:3]#	Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.
AD [0:31]	PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.
CBE [0:3]#	PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.
PAR	Parity bit for the PCI bus. Generated as even parity across AD [31:0] and CBE [3:0]#.
SERR#	System Error. Asserted for hardware error conditions such as parity errors detected in DRAM.
GPERR#	Parity Error. For PCI operation per exception granted by PCI 2.1 Specification.
PME#	Power management event.
LOCK#	Lock Resource Signal. This pin indicates that either the PCI master or the bridge intends to run exclusive transfers.
DEVSEL#	Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.
TRDY#	Target Ready. This pin indicates that the target is ready to complete the current data phase of a transaction.
IRDY#	Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.
STOP#	Stop. This signal indicates that the target is requesting that the master stop the current transaction.
FRAME#	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. The access will be either an output driven by the Northbridge on behalf of the CPU, or an input during PCI master access.
PCIRST#	PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.

Signal	Signal Description
INTA#, INTB#, INTC#, INTD#	PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices.
IDSEL	This pin is not present on the ESM-2545 module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device that is used to set the device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines in order to set a unique configuration address. In ETX systems, the four external bus slots or devices are assumed to use AD[19:22] for IDSEL connections.
PME#	Power management event..

2.4.3.2 USB Signals

Signal	Signal Description
USB [0:3]	Universal Serial Bus Port [0:3] positive signal. These are the serial data pairs for USB Port N-and Port N#.
USB [0:3]#	Universal Serial Bus Port [0:3] negative signal. These are the serial data pairs for USB Port N-and Port N#.

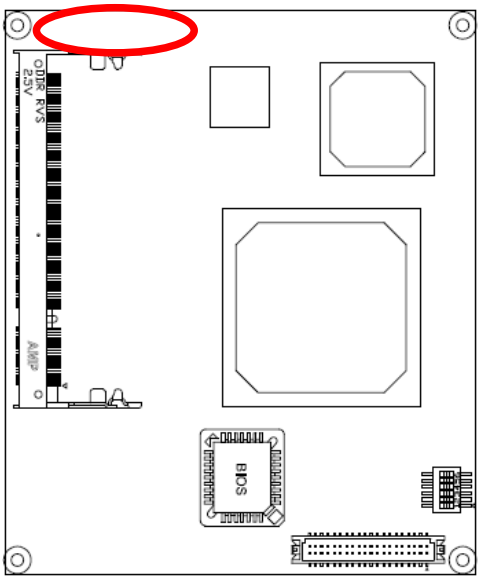
2.4.3.3 Audio Signals

Signal	Signal Description
SNDL/ SNDR	Line-level stereo output left/ right. These outputs have a nominal level of 1 volt RMS into a 10K impedance load. These outputs cannot drive low-impedance speakers directly.
AUXAL/ AUXAR	Auxiliary A input left/ right. Normally intended for connection to an internal or external CDROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm. Nominal input level is 1 volt RMS.
MIC	Microphone input. Minimum input impedance is 5KOhm, max. Input voltage is 0.15 Vp-p.
ASVCC	Analog supply voltage for sound controller. This is an output which is used for production test only. Do not make external connections to this pin.

2.4.3.4 Miscellaneous Signals

Signal	Signal Description
SERIRQ	Serial interrupt request. This pin is used to support the serial interrupt protocol.

2.4.4 ETX Connecter X2 (ETX2)



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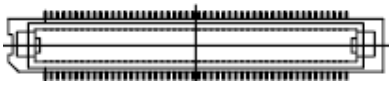
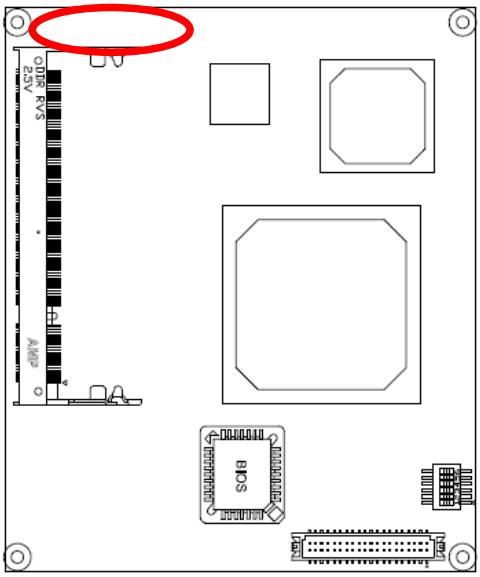


Signal	PIN	PIN	Signal
GND	1	2	GND
SD14	3	4	SD15
SD13	5	6	MASTER#
SD12	7	8	DREQ7
SD11	9	10	DACK7#
SD10	11	12	DREQ6
SD9	13	14	DACK6#
SD8	15	16	DREQ5
MEMW#	17	18	DACK5#
MEMR#	19	20	DREQ0
LA17	21	22	DACK0#
LA18	23	24	IRQ14
LA19	25	26	IRQ15
LA20	27	28	IRQ12
LA21	29	30	IRQ11
LA22	31	32	IRQ10
LA23	33	34	IO16#
GND	35	36	GND
SBHE#	37	38	M16#
SA0	39	40	OSC
SA1	41	42	BALE
SA2	43	44	TC
SA3	45	46	DACK2#
SA4	47	48	IRQ3
SA5	49	50	IRQ4



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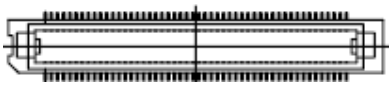


Signal	PIN	PIN	Signal
+5V	51	52	+5V
SA6	53	54	IRQ5
SA7	55	56	IRQ6
SA8	57	58	IRQ7
SA9	59	60	SYSCLK
SA10	61	62	REFSH#
SA11	63	64	DREQ1
SA12	65	66	DACK1#
GND	67	68	GND
SA13	69	70	DREQ3
SA14	71	72	DACK3#
SA15	73	74	IOR#
SA16	75	76	IOW#
SA18	77	78	SA17
SA19	79	80	SMEMR#
IOCHRDY	81	82	AEN
+5V	83	84	+5V
SD0	85	86	SMEMW#
SD2	87	88	SD1
SD3	89	90	NOWS#
DREQ2	91	92	SD4
SD5	93	94	IRQ9
SD6	95	96	SD7
IOCHK#	97	98	RSTDRV
GND	99	100	GND

2.4.5 Signal Description – ETX Connecter X2 (ETX2)

2.4.5.1 ISA Signals

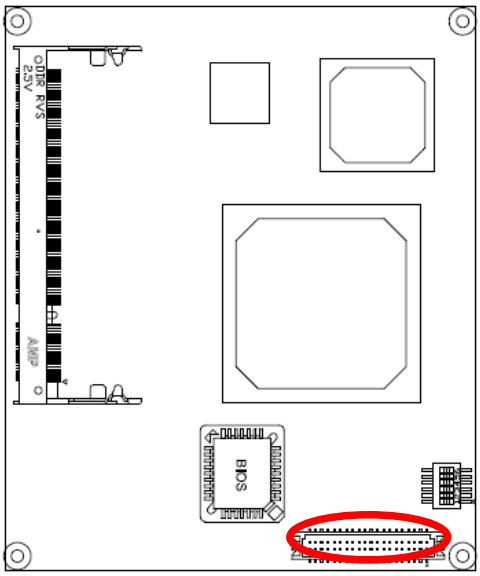
Signal	Signal Description
SD[0:15]	These signals provide data bus bits 0 to 15 for any peripheral devices. All 8-bit devices use SD[0:7] for data transfers. 16-bit devices use SD[0:15]. To support 8-bit devices, the data on SD[8:15] is gated to SD[0:7] during 8-bit transfers to these devices. 16-bit CPU cycles will be automatically converted into two 8-bit cycles for 8-bit peripherals.
SA[0:19]	Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17:23] allow access of up to 16MB of memory. SA[0:19] are gated on the ISA-bus when BALE is high and latched on to the falling edge of BALE.
SBHE#	*Bus High Enable* indicates a data transfer on the upper byte of the data bus SD[8:15]. 16-bit I/O devices use SBHE# to enable data bus buffers on SD[8:15].
BALE	BALE is an active-high pulse generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA[0:19], LA17.23, AEN, and SBHE# signals are valid.
AEN	AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.
MEMR#	MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory read cycles.
SMEMR#	SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory read cycles to addresses below 1MB.
MEMW#	MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory write cycles.
SMEMW#	SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory write cycles to address below 1MB.
IOR#	I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.

Signal	Signal Description
IOW#	I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.
IOCHK#	IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.
IOCHRDY	The I/O Channel Ready is pulled low in order to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. Any peripheral that cannot present read data or strobe in write data within this amount of time use IOCHRDY to extend these cycles. This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content due to the fact that memory refresh is disabled while IOCHRDY is low.
M16#	The M16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the M16# line is high. If M16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If M16# is low, an access to peripherals is done 16 bits wide.
IO16#	The IO16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the IO16# line is high. If IO16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If IO16# is low, an access to peripherals is done at 16 bit width.
REFSH#	REFSH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us in order to prevent loss of DRAM data.

Signal	Signal Description
NOWS#	The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.
MASTER#	This signal is used with a DRQ line to gain control of the system bus. A processor or a DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost as memory refresh is disabled during this process.
SYSCLK	SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary. This signal is supplied at all times except when the CPU module is in sleep mode.
OSC	OSC is supplied by the CPU module. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.
RESETDRV	This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices.
DREQ [0, 1, 2, 3, 5, 6, 7]	The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on the CPU modules.
DACK [0, 1, 2, 3, 5, 6, 7]#	DMA acknowledge 0.3 and 5.7 are used to acknowledge DMA requests. They are active-low.

Signal	Signal Description
TC	The active-high output TC indicates that one of the DMA channels has transferred all data.
IRQ [3:7, 9, 15]	These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are active-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

2.4.6 ETX Connecter X3 (ETX3)



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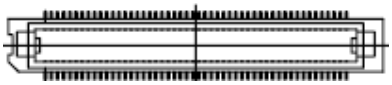
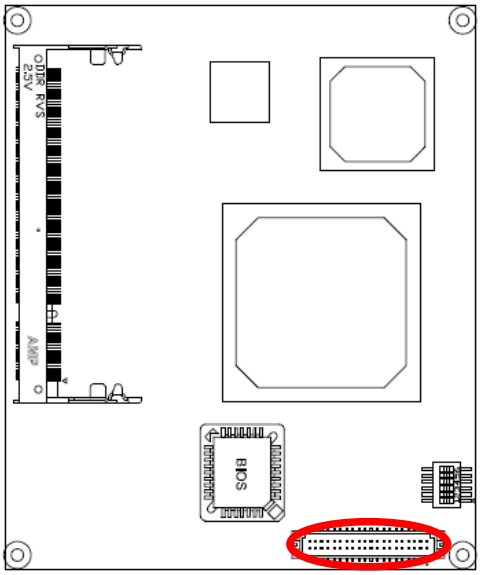


Signal	PIN	PIN	Signal
GND	1	2	GND
R	3	4	B
HSY	5	6	G
VSY	7	8	DDCK
NC	9	10	DDDA
NC	11	12	NC
NC	13	14	NC
GND	15	16	GND
NC	17	18	NC
NC	19	20	NC
GND	21	22	GND
Txout3#	23	24	NC
Txout3	25	26	NC
GND	27	28	GND
Txout2#	29	30	Txclk
Txout2	31	32	Txclk#
GND	33	34	GND
Txout0	35	36	Txout1
Txout0#	37	38	Txout1#
+5V	39	40	+5V
I^2C_DAT	41	42	NC
I^2C_CLK	43	44	ENBKL#
NC	45	46	DIGON
NC	47	48	NC
NC	49	50	NC



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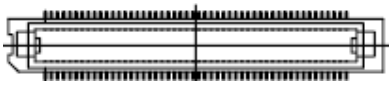


Signal	PIN	PIN	Signal
LPT/FLPY#	51	52	NC
+5V	53	54	GND
STB#	55	56	AFD#
NC	57	58	PD7
IRRX	59	60	ERR#
IRTX	61	62	PD6
RXD2	63	64	INIT#
GND	65	66	GND
RTS2#	67	68	PD5
DTR2#	69	70	SLIN#
DCD2#	71	72	PD4
DSR2#	73	74	PD3
CTS2#	75	76	PD2
TXD2#	77	78	PD1
RI2#	79	80	PD0
+5V	81	82	+5V
RXD1	83	84	ACK#
RTS1#	85	86	BUSY#
DTR1#	87	88	PE
DCD1#	89	90	SLCT#
DSR1#	91	92	MSCLK
CTS1#	93	94	MSDAT
TXD1	95	96	KBCLK
RI1#	97	98	KBDAT
GND	99	100	GND

2.4.7 Signal Description – ETX Connecter X3 (ETX3)

2.4.7.1 VGA Signals

Signal	Signal Description
HSY	Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.
VSY	Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.
R, G, B	Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.
DDCK, DDDA	These two pins can be used for a DDC interface between the graphics controller chip and the CRT monitor.

2.4.7.2 LVDS Flat Panel Interface Signals

Signal	Description
I^2C_DAT, I^2C_CLK	I^2C interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.
DIGON	**Controls panel digital power.**
ENBKL#	**Controls backlight power enable.**

2.4.7.3 Serial Port Signals

Note that all serial port signals on ESM-2545 connectors are logic level signals. External transceiver devices are necessary for the conversion of the logic level signals to the desired physical interface such as RS232, RS422, or RS485.

Signal	Signal Description
DTR1#, DTR2#	Active-low data terminal ready outputs for the serial port. Handshake output signal notifies the modem that the UART is ready to establish a data communication link.
RI1#, RI2#	Active-low input is for the serial port. Handshake signals notify the UART when a telephone ring signal is detected by the modem.
TXD1, TXD2	Transmitter serial data output from serial port.
RXD1, RXD2	Receiver serial data input.
CTS1#, CTS2#	Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.
RTS1#, RTS2#	Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.
DCD1#, DCD2#	Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.
DSR1#, DSR2#	This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

2.4.7.4 PS/2 Keyboard & Mouse Signals

Signal	Signal Description
KBDAT	Bi-directional keyboard data signal.
KBCLK	Keyboard clock signal.
MSDAT	Bi-directional mouse data signal.
MSCLK	Mouse clock signal.

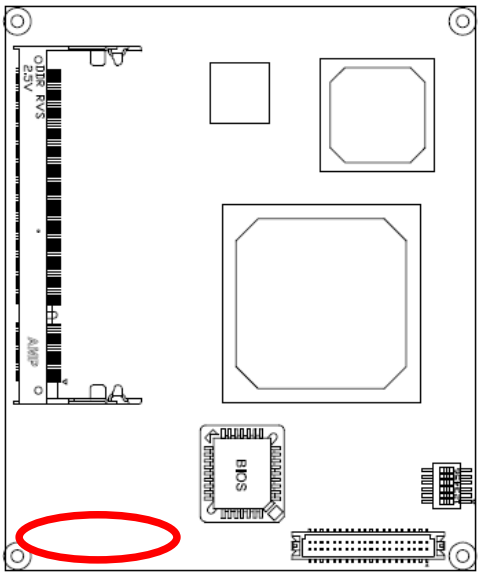
2.4.7.5 IrDA (SIR) Signals

Signal	Signal Description
IRTX, IRRX	Infrared transmit and receive pins.

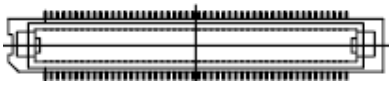
2.4.7.6 Parallel Port Signals

Signal	Signal Description
LPT/FLPY#	This ETX input signal selects whether the parallel port pins will implement parallel port or floppy support functionality. There is an internal pull-up on this signal. If this signal is high or unconnected, the following parallel port pin functions are in effect:
STB#	This active-low signal is used to strobe the printer data into the printer.
AFD#	This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.
PD[0:7]	This bi-directional parallel data bus is used to transfer information between the CPU and the peripherals.
ERR#	This active-low signal indicates an error situation has occurred at the printer.
INIT#	This active-low signal is used to initiate the printer when low.
SLIN#	This active-low signal selects the printer.
ACK#	This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.

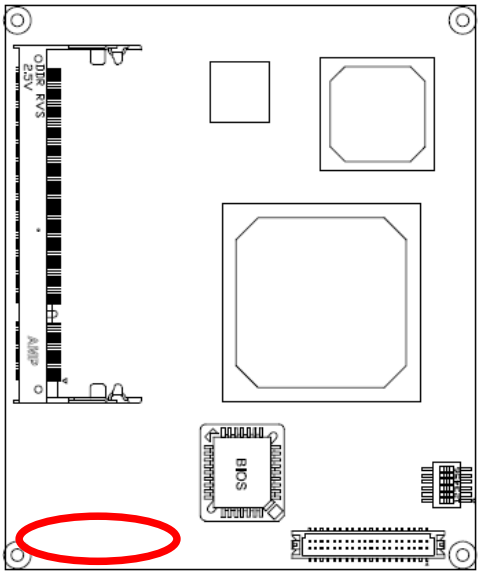
2.4.8 ETX Connecter X4 (ETX4)



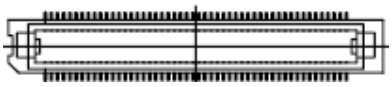
(Rear side)



Signal	PIN	PIN	Signal
GND	1	2	GND
5V_SB	3	4	NC
PS_ON	5	6	SPEAKER
PWRBTN#	7	8	BATT
NC	9	10	LILED
RSMRST#	11	12	ACTLED
NC	13	14	SPEEDLED
NC	15	16	I^2CLK
+5V	17	18	+5V
OVCR#	19	20	NC
EXTSMI#	21	22	I^2DAT
SMBCLK	23	24	SMBDATA
NC	25	26	NC
NC	27	28	DASP_S
NC	29	30	PIDE_CS3#
NC	31	32	PIDE_CS1#
GND	33	34	GND
NC	35	36	PIDE_A2
NC	37	38	PIDE_A0
NC	39	40	PIDE_A1
NC	41	42	NC
NC	43	44	PIDE_INTRQ
NC	45	46	PIDE_AK#
NC	47	48	PIDE_RDY
+5V	49	50	+5V



(Rear side)



Signal	PIN	PIN	Signal
NC	51	52	PIDE_IOR#
NC	53	54	PIDE_IOW#
NC	55	56	PIDE_DRQ
NC	57	58	PIDE_D15
NC	59	60	P IDE_D0
NC	61	62	PIDE_D14
NC	63	64	PIDE_D1
GND	65	66	GND
NC	67	68	PIDE_D13
NC	69	70	PIDE_D2
NC	71	72	PIDE_D12
NC	73	74	PIDE_D3
NC	75	76	PIDE_D11
NC	77	78	PIDE_D4
NC	79	80	PIDE_D10
+5V	81	82	+5V
NC	83	84	PIDE_D5
NC	85	86	PIDE_D9
NC	87	88	PIDE_D6
GPE2#	89	90	CBLID_P#
RXD#	91	92	PIDE_D8
RXD	93	94	NC
TXD#	95	96	PIDE_D7
TXD	97	98	HDRST#
GND	99	100	GND

2.4.9 Signal Description – ETX Connecter X4 (ETX4)

2.4.9.1 IDE Signals

Signal	Signal Description
PIDE_D[0:15]	IDE Data Bus.
PIDE_A[0:2]	IDE Address Bus.
PIDE_CS1#	IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_CS3#	IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_DRQ	IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.
PIDED_AK#	IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
PIDE_RDY	IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions.
PIDE_IOR#	IDE IOR# Command. This is the IOR# command output pin used to tell the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_IOW#	IDE IOW# Command. This is the IOW# command output pin used to notify the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_INTRQ	Interrupt request signal from the IDE device.
CBLID_P#	IDE cable detection. This is the CBLID_P# command may be used to detect the presence of an 80-conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.
HDRST#	Low-active hardware reset (RSTDRV inverted).

2.4.9.2 Ethernet Signals

Signal	Signal Description
TXD#, TXD	Ethernet Transmit Differential Pair. These pins transmit the serial bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
RXD#, RXD	Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
ACTLED	The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
LILED	The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
SPEEDLED	The Speed LED pin indicates high speed operation. This LED is not supported by all ETX boards. This pin is asserted low when a 100Mbps link is detected, and is not asserted for a 10Mbps link. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

2.4.9.3 Power Management Signals

Signal	Signal Description
RSMRST#	*Resume Reset input*. This input may be driven low by external circuitry in order to reset the power management logic on the ETX module.
EXTSMI	System management interrupt input. May be driven low by external circuitry to initiate an SMI.

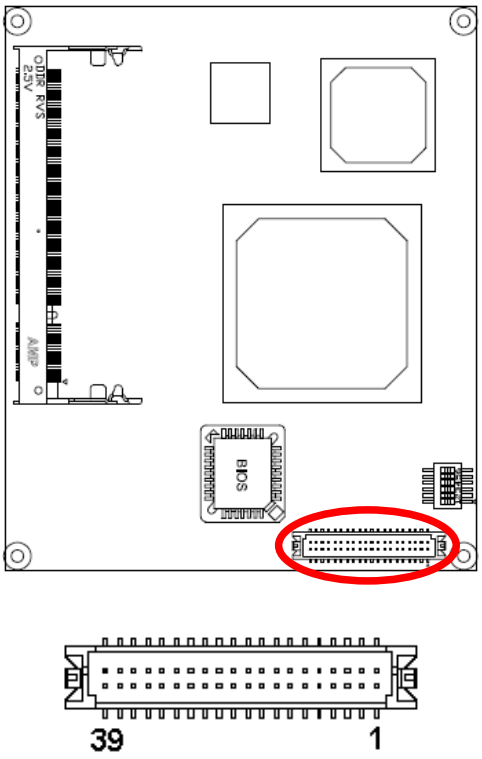
2.4.9.4 Power Control Signals

Signal	Signal Description
5V_SB	Power input for the internal suspends and power control circuitry. Connect to a 5V, 100mA stand-by power source available. May be a no-connect if a standby supply is not available.
PS_ON	Active-low output from ESM-2545. Can be connected to the PS_ON input of an ATX power supply in order to switch the main output. In order for this pin to function, 5V_SB must be supplied to the ESM-2545.
PWRBTN#	Power Button Input. Connect to GND with momentary-contact switch or open collector driver to implement ATX power button control of PS_ON. In order for this pin to function, 5V_SB must be supplied to the ESM-2545.

2.4.9.5 Miscellaneous Control Signals

Signal	Signal Description
SPEAKER	PC speaker output signal. This logic-level signal can be connected to an external transistor in order to drive a piezoelectric or dynamic speaker.
BATT	This is a 3V-backup-cell input. BATT is typically connected to a 3V-lithium-backup cell for RTC operation and CMOS register non-volatility in the absence of system power. When RTC operation is not required by the application, some ETX modules can back up CMOS contents to EEPROM without using a battery.
I^2C_DAT, I^2C_CLK	These clock and data lines implement an I^2C-bus, which supports external slave devices only. Data rate is approximate 1-10kHz. This interface supports EEPROMs and other simple I/O devices.
OVCR#	Over-current input detection. Used to monitor the USB power over-current. Pull with open collector to GND if over-current is detected.

2.4.10 TFT Panel Connector (JTFT)



Signal	PIN	PIN	Signal
+5V	2	1	+5V
GND	4	3	GND
+3.3V	6	5	+3.3V
GND	8	7	NC
P1	10	9	P0
P3	12	11	P2
P5	14	13	P4
P7	16	15	P6
P9	18	17	P8
P11	20	19	P10
P13	22	21	P12
P15	24	23	P14
P17	26	25	P16
P19	28	27	P18
P21	30	29	P20
P23	32	31	P22
GND	34	33	GND
FLM	36	35	SHFCLK
LP	38	37	M
NC	40	39	ENBKL

2.4.10.1 Signal Description – TFT Panel Connector (JTFT)

Signal	Description
P [0:23]	Flat panel data output for 18/24 bit TFT flat panels. Refer to table below for configurations for various panel types. The flat panel data and control outputs are all on-board controlled for secure power-on/off sequencing
SHFCLK	Shift Clock. Pixel clock for flat panel data
LP	Flat panel equivalent of HSYNC (horizontal synchronization)
FLM	Flat panel equivalent of VSYNC (vertical synchronization)
M	Multipurpose signal, function depends on panel type. May be used as AC drive control signal or as BLANK# or Display Enable signal
ENBKL	Enable backlight signal. This signal is controlled as a part of the panel power sequencing

2.4.10.2 Signal Description – TFT Panel Display (JTFT)

Signal	18-bit TFT	24-bit TFT
P0	-	B0
P1	-	B1
P2	B0	B2
P3	B1	B3
P4	B2	B4
P5	B3	B5
P6	B4	B6
P7	B5	B7
P8	-	G0
P9	-	G1
P10	G0	G2
P11	G1	G3
P12	G2	G4
P13	G3	G5
P14	G4	G6
P15	G5	G7
P16	-	R0
P17	-	R1
P18	R0	R2
P19	R1	R3
P20	R2	R4
P21	R3	R5
P22	R4	R6
P23	R5	R7

3. BIOS Setup

3.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
↑	Move to previous item
↓	Move to next item
←	Move to the item in the left hand
→	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

- **Navigating Through The Menu Bar**

  Use the left and right arrow keys to choose the menu you want to be in.

Note: Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**
  Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.4 In Case of Problems

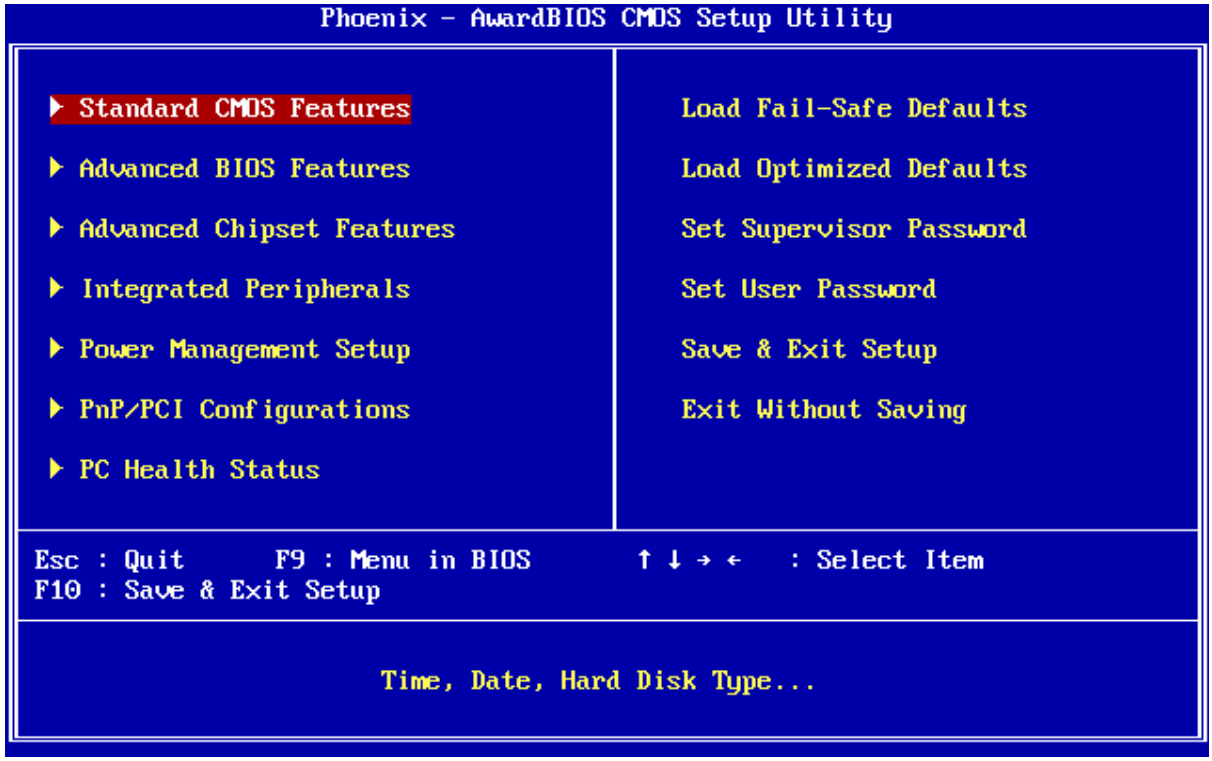
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

3.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

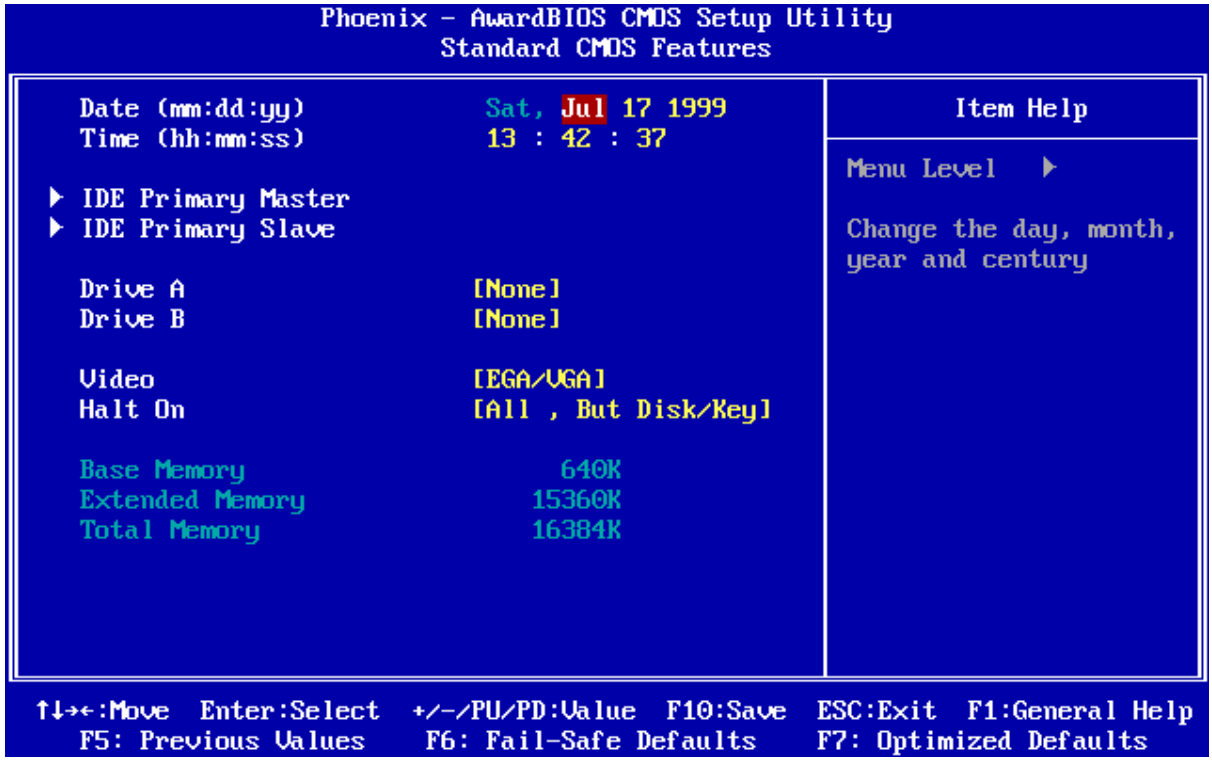
Note that a brief description of each highlighted selection appears at the bottom of the screen.



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen.
Visit the Avalue website (www.avalue.com.tw) to download the latest product and BIOS information.

3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



3.5.1.1 Main Menu Selection

This reference table shows the selections that you may make on the Main Menu.

Item	Options	Description
Date	MM DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master IDE Primary Slave	Options are in 3.5.1.2	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard Invalid All, but Diskette Invalid All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you

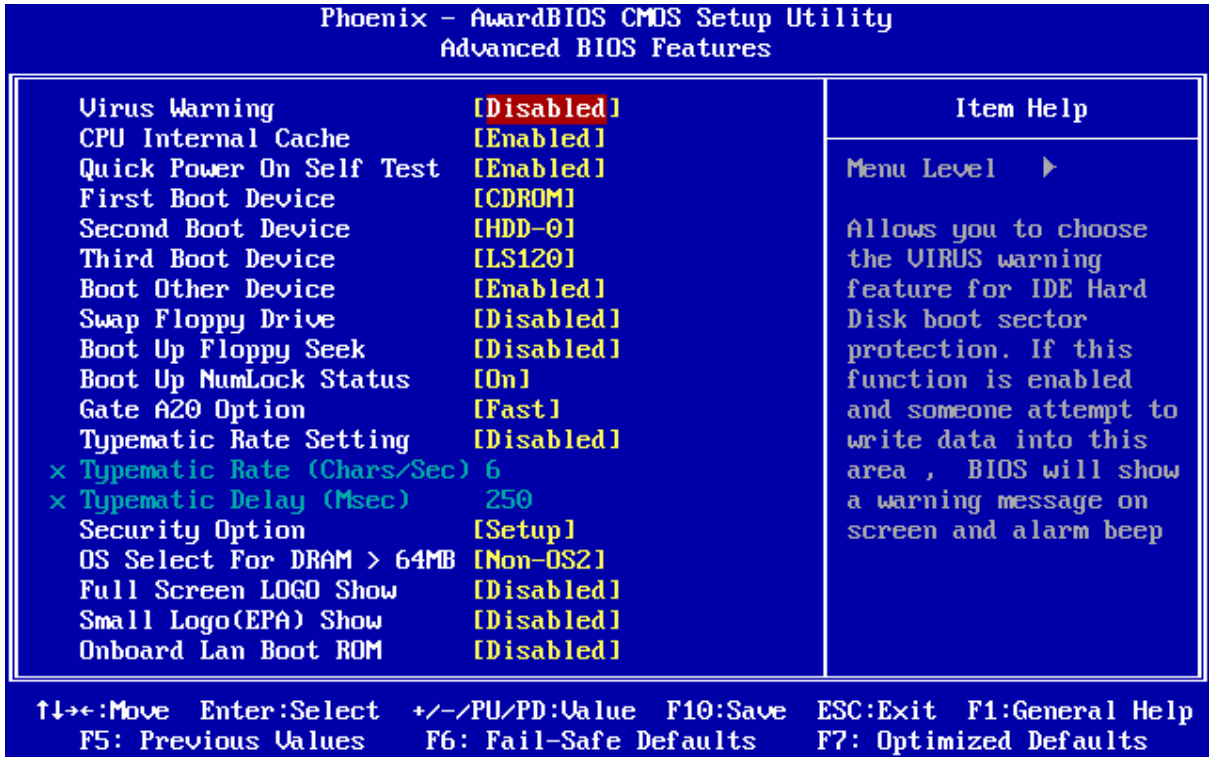
3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. The below Figure will shows the IDE primary master sub menu.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master IDE Primary Slave,	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Access Mode	CHS LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Channel …' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



3.5.2.1 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Item	Description
Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

3.5.2.2 CPU Internal Cache

This category speeds up memory access. However, it depends on CPU/chipset design. The default value is en able.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.3 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Item	Description
Enabled	Enable quick POST
Disabled	Normal POST

3.5.2.4 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Item	Description
Floppy	Floppy Device
LS120	LS120 Device
HDD-0	First Hard Disk Device
SCSI	SCSI Device
CDROM	CDROM Device
HDD-1	Second Hard Disk Device
USB-FDD	USB Floppy Device
USB-ZIP	USB ZIP Device
USB-CDROM	USB CDROM Device
USB-HDD	USB Hard Disk Device
LAN	Network Device
Disabled	Disabled any boot device

3.5.2.5 Swap Floppy Drive

While system has two floppy drivers installed, this item will be affected. This function is to assign physical drive B to logical drive A.

Item	Description
Enabled	Assign physical drive B to logical drive A
Disabled	No change

3.5.2.6 Boot Up Floppy Seek

Select whether the system seeks for a floppy driver every time the system boots.

Item	Description
Enabled	Seek for a floppy driver
Disabled	Skip driver seeking

3.5.2.7 Boot Up NumLock Status

Select power on state for NumLock.

Item	Description
ON	Enable NumLock
OFF	Disable NumLock

3.5.2.8 Gate A20 Option

Select if chipset or keyboard controller should control Gate A20.

Item	Description
Normal	A pin in the keyboard controller controls Gate A20
Fast	Lets chipset control Gate A20

3.5.2.9 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

Item	Description
Enabled	Enable typematic rate/delay setting
Disabled	Disable typematic rate/delay setting

3.5.2.10 Typematic Rate (chars/Sec)

The BIOS features will only work if the Typematic Rate Setting features has been enabled. This feature determines the rate at which the keyboard will repeat a keystroke if you pass it continuously.

The Choices: 6, 8, 10, 12, 15, 20, 24, 30

3.5.2.11 Typematic Delay

This BIOS setting will only work if the Typematic Rate Setting feature has been enabled. This feature determines how long, in milliseconds (thousandths of a second), the keyboard controller will wait before it starts repeating the keystroke that you have pressed continuously. The longer the delay, the longer the keyboard controller will wait before it starts repeating the keystroke.

The Choices: 250, 500, 750, 1000

3.5.2.12 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

Item	Description
System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

3.5.2.13 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

Item	Description
Non-OS2	Disable OS for over 64 MB DRAM
OS2	Enable OS for over 64 MB DRAM

3.5.2.14 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

Item	Description
Enable	Enable full screen logo show
Disable	Disable full screen logo show

3.5.2.15 Small Logo (EPA) Show

This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description
Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

3.5.2.16 Onboard LAN Boot ROM

This item allows to boot over the network when system POST and shorten the booting time by set disabled

Item	Description
Enabled	Enable Onboard LAN boot.
Disabled	Disabled Onboard LAN boot.

3.5.2.17 C8000-CBFFF/CC000-CFFFF/D0000-D3FFF/D4000-D7FFF/D8000-DBFFF/DC000-DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

Item	Description
Enabled	Optional shadow is enabled
Disabled	Optional shadow is Disabled

3.5.2.18 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

Item	Description
Enable	Enable full screen logo show
Disable	Disable full screen logo show

3.5.2.19 Small Logo (EPA) Show

This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description
Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

3.5.2.20 Onboard LAN Boot ROM

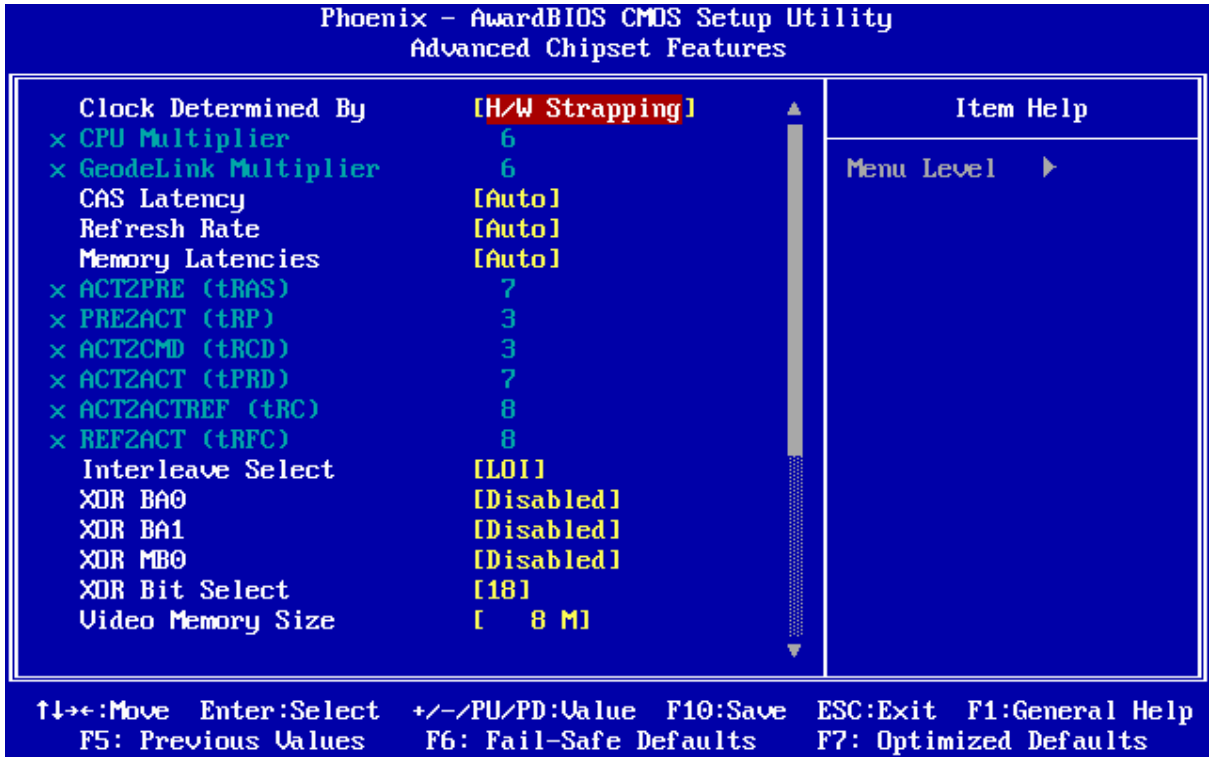
This item allows to boot over the network when system POST and shorten the booting time by set disabled

Item	Description
Enabled	Enable Onboard LAN boot.
Disabled	Disabled Onboard LAN boot.

3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.



3.5.3.1 Clock Determined By

Allows the clock speed to either be determined by the hardware strapping or manual settings. If the H/W strapping option is selected, then the manual divisor settings will be grayed out.

The choices: H/W Strapping, Manual Setting

3.5.3.2 CPU Frequency

The formulae for the CPU Multiplier are as follows

33.3 Mhz * CPU Multiplier = CPU speed

The choices: 1~32

3.5.3.3 CAS Latency

This item allows to select CAS Latency.

The choices: Auto, 1.5, 2.0, 2.5, 3.0, 3.5.

3.5.3.4 Refresh Rate

This item allows you to set the refresh rate of chipset.

The choices: 15µs, 3 µs, 7 µs, 31 µs, 62 µs, 123µs, Auto

3.5.3.5 Memory Latency

This item allows you to set Memory Latency mode.

The choices: Auto, Manual

3.5.3.6 ACT2PRE (tRAS)

Like DRAM Act to PreChrg CMD, this BIOS feature controls the memory bank's minimum row active time (tRAS). This constitutes the time when a row is activated until the time the same row can be deactivated.

The choices: 0~15

3.5.3.7 PRE2ACT (tRP)

This item allows you to set PRE2ACT.

The choices: 0~7

3.5.3.8 ACT2CMD (tRCD)

This item allows you to set ACT2CMD.

The choices: 0~7

3.5.3.9 ACT2ACT (tPRD)

This item allows you to set ACT2ACT.

The choices: 0~15

3.5.3.10 ACT2ACTREF (tRC)

This BIOS feature controls the memory module's Row Cycle Time or tRC. The row cycle time determines the minimum number of clock cycles a memory row takes to complete a full cycle, from row activation up to the precharging of the active row.

The choices: 0~15

3.5.3.11 REF2ACT (tRFC)

This item allows you to set ACT2ACTREF.

The choices: 0~31

3.5.3.12 Video Memory Size

This item allows selecting video memory size.

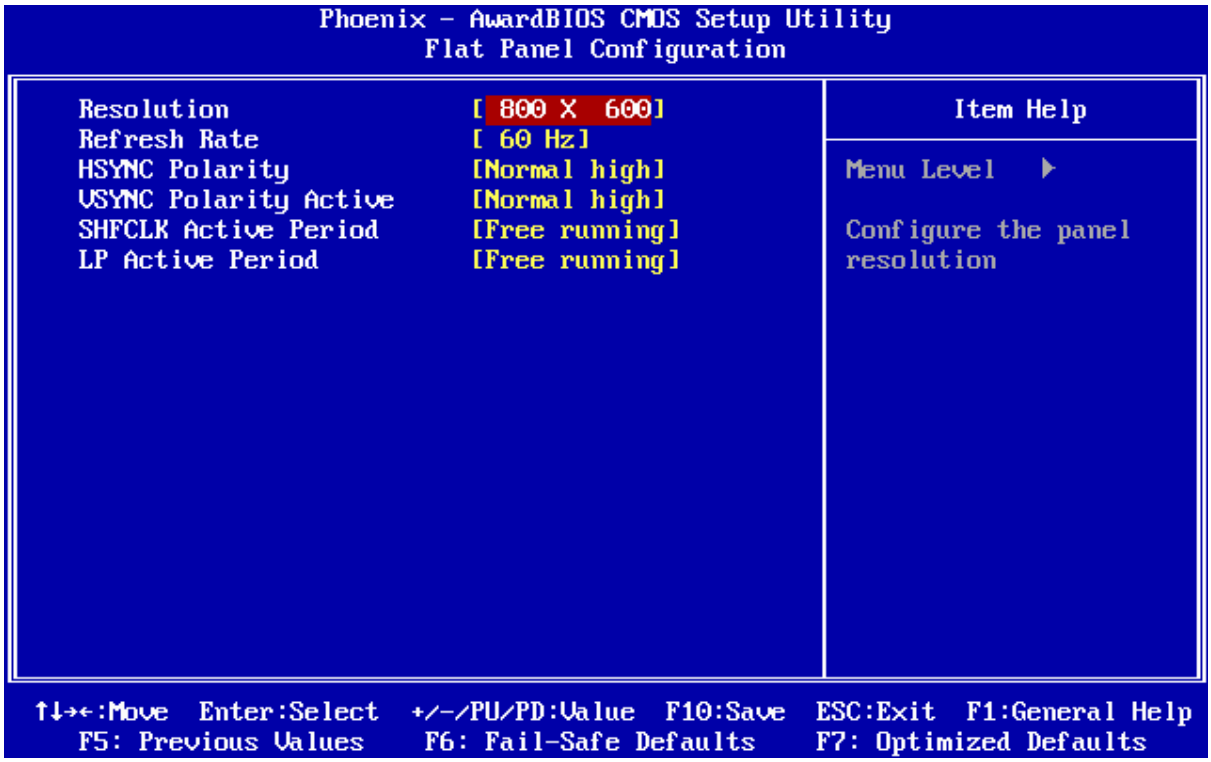
The choices: Disable, 8 M, 16 M, 32 M, 64 M, 128 M, 254 M.

3.5.3.13 Output display

This item allows to select output display.

The choices: Auto, lat Panel, TV Output, CRT, CRT, Panel & CRT.

3.5.3.14 Flat Panel Configuration



Item	Options	Description
Flat Panel Type	TFT, LVDS Auto	This item allows to select the flat panel type.
Resolution	320x240, 640x480, 800x600, 1024x768, 1152x864, 1280x1024, 1600x1200	This item allows to select the resolution.
Refresh Rate	60Hz, 70Hz, 72Hz, 75Hz, 85Hz, 90Hz, 100Hz	This refresh rate is only the number of time the image is being refreshed on the monitor screen.
HSYNC Polarity	Normal High, Normal Low	Select polarity of HSYNC signals.
VSYNC Polarity Active	Normal High, Normal Low	Set the polarity of VSYNC signals active.
SHFCLK Active Period	Active only, Free running	Shift clock or pixel clock for the flat panel data.
LP Active Period	Active running Free running	Latch Pulse is the line pulse or latch pulse for the flat panel data.

3.5.3.15 Onboard Audio

This item allows you to enable the onboard audio function.

The choices: Enabled, Disabled.

3.5.3.16 Onboard USB1.1

This item allows you to enable the USB1.1 function.

The choices: Enabled, Disabled.

3.5.3.17 Onboard USB2.0

This item allows you to enable USB2.0 function.

The choices: Enabled, Disabled.

3.5.3.18 Onboard USB UBC

This item allows you to enable USB UBC function.

The choices: Enabled, Disabled.

3.5.3.19 Onboard USB OTG

This item allows you to enable USB OTG function.

The choices: Enabled, Disabled.

3.5.3.20 Onboard IDE

This item allows you to enable IDE function.

The choices: Enabled, Disabled.

3.5.3.21 Overcurrent report

This item allows you to select overcurrent report

The choices: Enabled, Disabled.

3.5.3.22 Port 4 assignment

This item allows you to select port 4 assignment.

The choices: Host, Device, Not used.

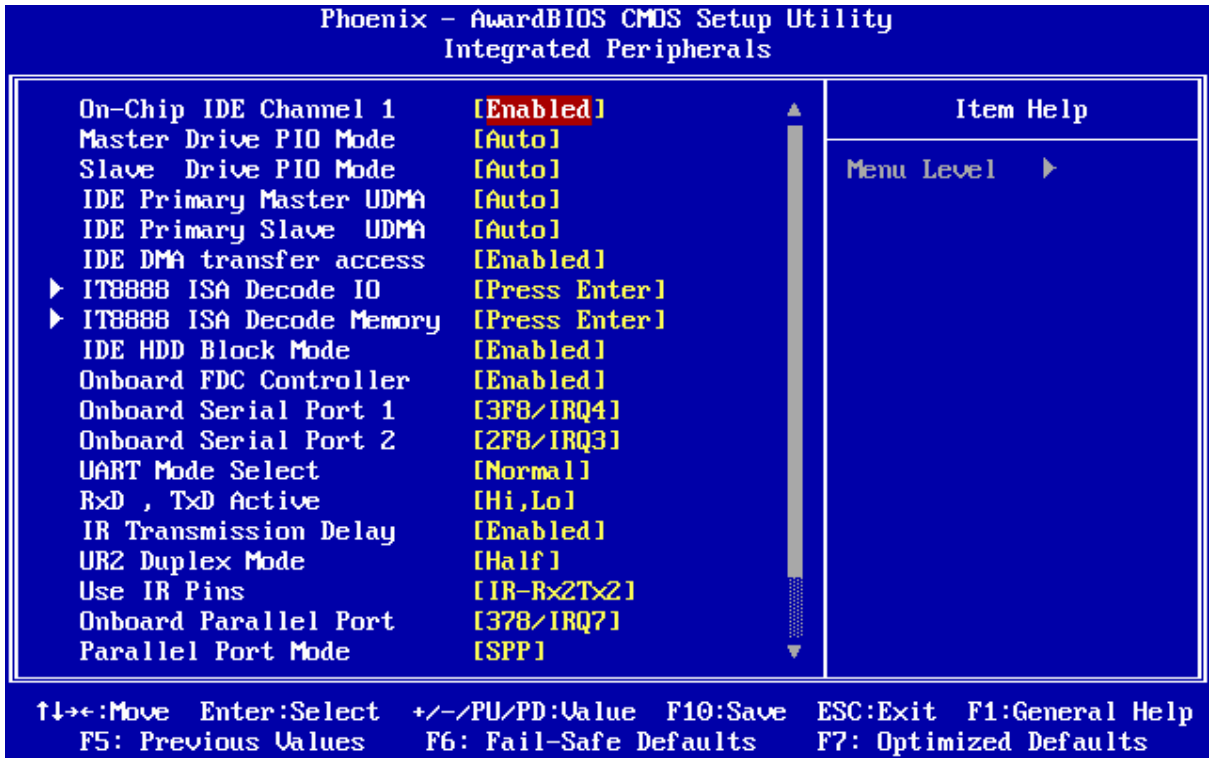
3.5.3.23 Memory Hole At 15M-16M

This item allows you to select memory hole at 15M-16M.

The choices: Enabled, Disabled.

3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

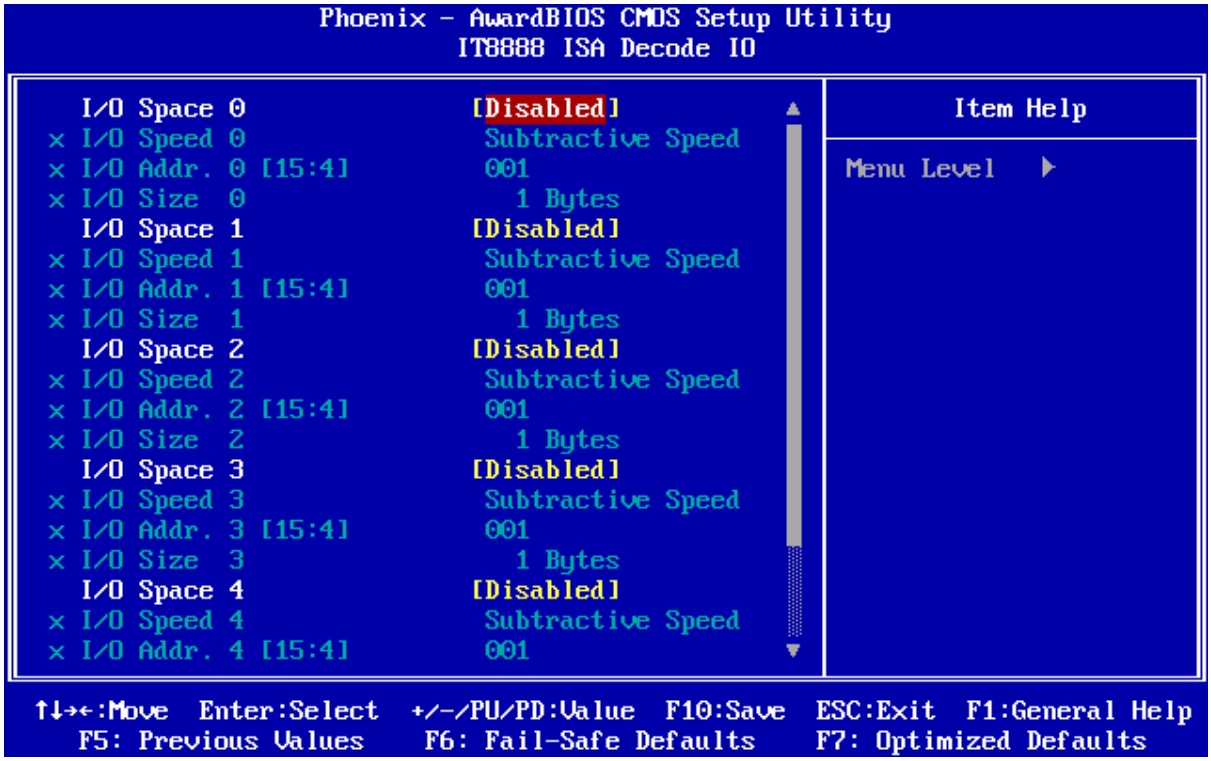


Item	Options	Description
On-Chip IDE Channel 1	Enabled Disabled	This item allows to enable On-chip IDE channel.
Master Drive PIO Mode Slave Drive PIO Mode	Auto Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	The IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
IDE Primary Master UDMA	No Value	Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If the hard drive and the system software both support Ultra DMA, select Auto to enable BIOS support.
IDE Primary Slave UDMA	Auto Disabled	
IDE DMA Transfer	Enabled Disabled	This feature allows you to enable or disable DMA (Direct Memory Access) support for all IDE devices. If you disable this BIOS feature, the BIOS will disable DMA transfers for all IDE drives. They will revert to PIO mode transfers. If you enable this BIOS feature, the BIOS will enable DMA transfers for all IDE drives. The proper DMA mode will be detected at boot-up. If the drive does not support DMA transfers, then it will use PIO mode instead.
IT8888 ISA Decode IO IT8888 ISA Decode Memory	Options are in 3.5.1.2	Press <Enter> to enter the sub menu of detailed options
IDE HDD Block Mode	Enabled Disabled	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If the IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard FDC Controller	Enabled Disabled	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you are not going to use FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Port 1 Onboard Serial Port 2	Disable 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3 Auto	Select an address and corresponding interrupt for the first and second serial ports.
UART Mode Select	IrDA ASKIR Normal	Select UART2 mode as standard serial port or IR port.
RxD , TxD Active	Hi,Hi Hi,Lo Lo,Hi Lo,Lo	This item allows you to determine the active of RxD, TxD level.
IR Transmission Delay	Enabled Disabled	This item allows you to enable/disable the IR Transmission Delay.
UR2 Duplex Mode	Half Full	Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction

		transmission. Half-duplex mode permits transmission in one direction only at a time.
Use IR Pins	RxD2,TxD2 IR-Rx2Tx2	This item allows you to determine the pin definition.
Onboard Parallel Port	Disabled 378/IRQ7 278/IRQ5 3BC/IRQ7 Auto FDD Mode	Select a matching address and interrupt for the physical parallel (printer) port.
Parallel Port Mode	SPP EPP ECP ECP+EPP Normal	Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.
EPP Mode Select	EPP1.9 EPP1.7	Select EPP port type 1.7 or 1.9.
ECP Mode Use DMA	1 3	Select a DMA channel for the port.
Watch Dog Timer Select	Disabled, 10, 20, 30, 40 Sec. 1, 2, 4 Min.	This option will determine watch dog timer

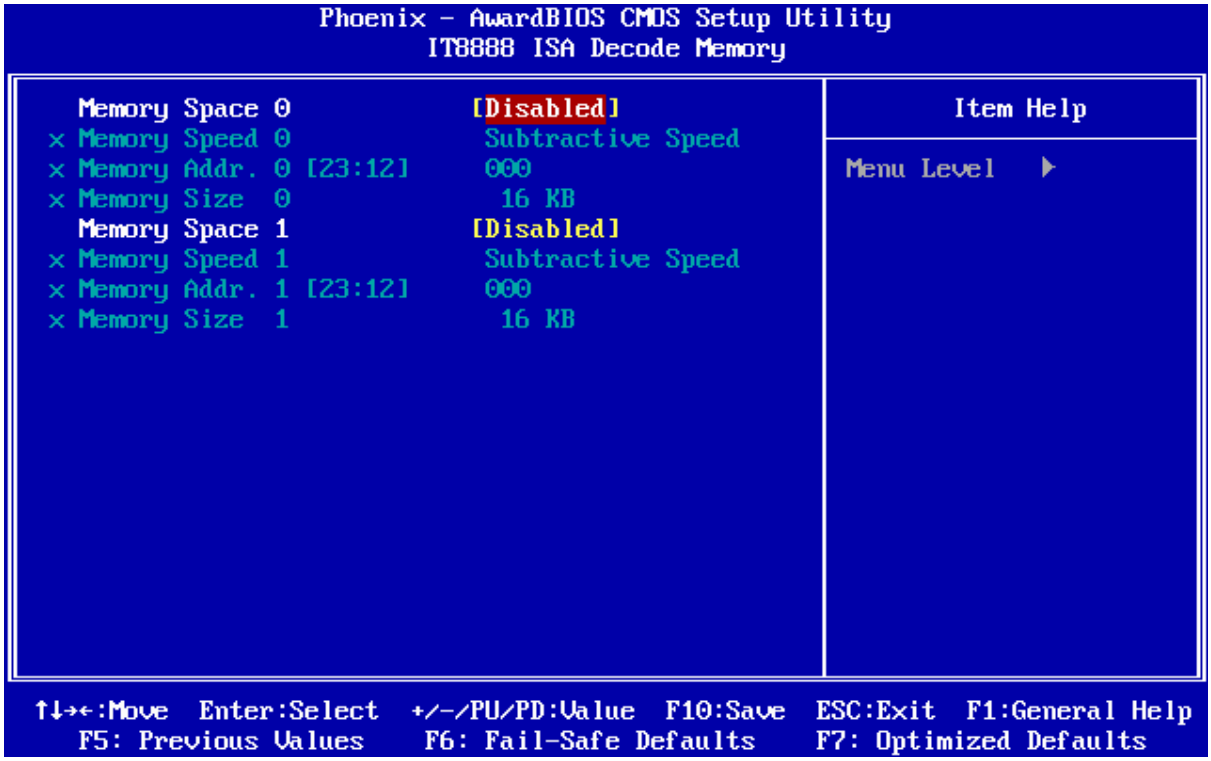
3.5.4.1 IT8888 ISA Decode IO

The decode I/O spaces can be programmed to claim PCI I/O cycle with Fast/Medium/Slow/Subtractive DEVSEL# (Device Select) timing speed.



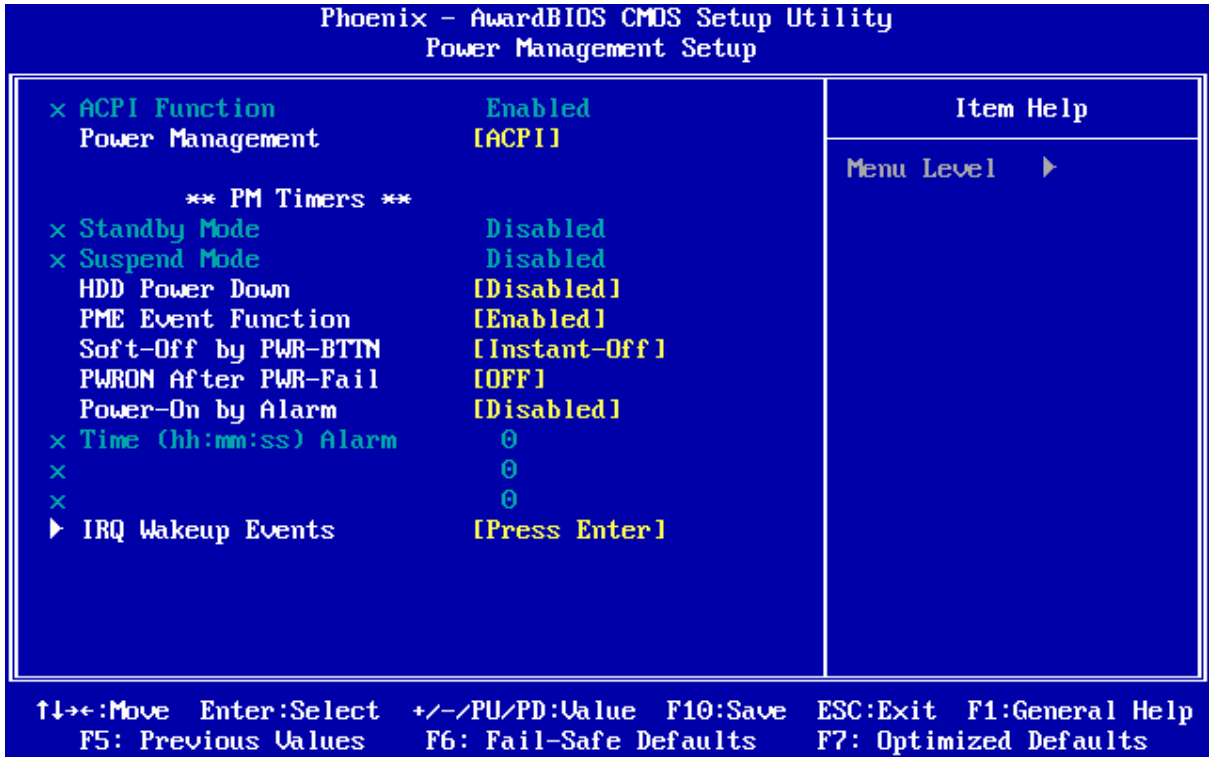
3.5.4.2 IT8888 ISA Decode Memory

The decode Memory spaces can be programmed to claim PCI Memory cycle with Fast/Medium/Slow/Subtractive DEVSEL# (Device Select) timing speed.



3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



3.5.5.1 Power Management

This category allows you to select the type (or degree) of power saving.

The choices: Disabled, Legacy, APM, ACPI.

3.5.5.2 Standby Mode

This item allows you to select the mode of standby.

The choices: Disabled, 1, 5, 10, 15, 30, 45 Sec., 1, 5, 10, 15, 30, 45, 60, 90, 120 Min

3.5.5.3 Suspend Mode

This item allows you to select the mode of suspend.

The choices: Disabled, 1, 5, 10, 15, 30, 45 Sec., 1, 5, 10, 15, 30, 45, 60, 90, 120 Min

3.5.5.4 HDD Power Down

This category allows you to set the mode of power saving.

The choices: Disabled, 1, 5, 10, 15, 30, 45 Sec., 1, 5, 10, 15, 30, 45, 60, 90, 120 Min

3.5.5.5 PME Event Function

This category allows you to select the type (or degree) of PME Function.

The choices: Disabled, Enable

3.5.5.6 Soft-Off by PWR-BTTN

This determines whether the system shut down instantly or delayed for 4 seconds when pushing on power button.

The choices: Instant-Off, Delay 4 Sec.

3.5.5.7 PWRON after PWR-Fail

This BIOS feature allows you to set the PC to automatically start itself up after a power failure. When set to On, the PC will automatically start up when power is restored. When set to Off, the PC will remain powered off even when power is restored.

The choices: On, OFF

3.5.5.8 Power-On by Alarm

This function is for setting date and time for your computer to boot up.

The choices: Enabled, Disabled.

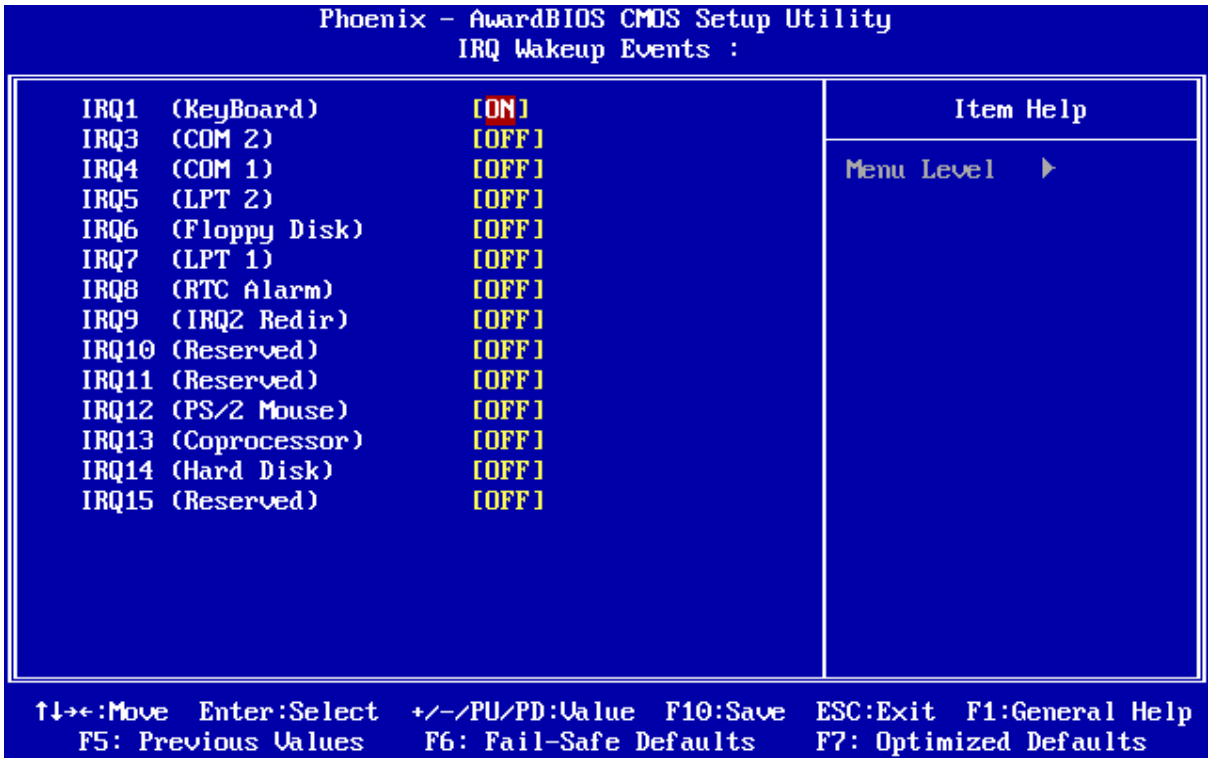
3.5.5.9 Time<hh:mm:ss> Alarm

After enabled “Power-On by Alarm”, set the specific hour/minute/second specified in these fields.

The choices: Alarm Hour: 00-23 /Alarm Minute: 00-59/ Alarm Second: 00-59

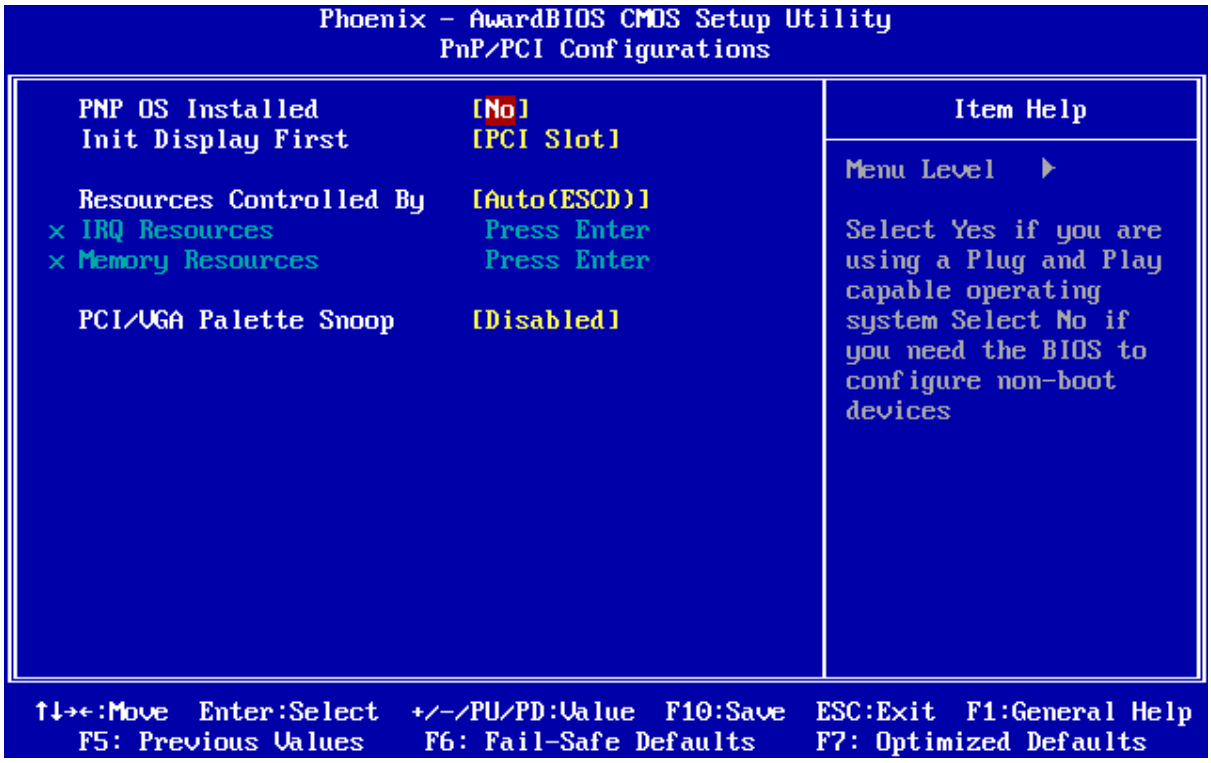
3.5.5.10 IRQ Wakeup Events

The VGA, LPT & COM, HDD & FDD, and PCI master are I/O events which can prevent the system from entering a power saving mode or can awaken the system from such a mode. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service.



3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



3.5.6.1 PNP OS Installed

The operation system environment is Plug-and-Play aware sets “YES”

The choices: Yes, No.

3.5.6.2 Init Display First

This item allows you to decide to active whether PCI Slot or AGP first.

The choices: PCI Slot, Onboard.

3.5.6.3 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

3.5.6.4 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all booting and Plug & Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field

to "manual" choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a "➢").

The choices: Auto (ESCD), Manual.

3.5.6.5 IRQ Resource

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

3.5.6.6 IRQ-3/4/5/7/10/11 assigned to

This item allows you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot. Reserved (Legacy ISA) for devices compliant with the original PC AT bus specification, PCI devices (PCI/ISA PnP) compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

The choices: PCI device, Reserved

3.5.6.7 Memory Resources

When resources are controlled manually, assign each system memory a type, depending on the type of device using the memory.

3.5.6.8 Reserved Memory Base

This section shows the status of your memory resources.

The choices: N/A, C800, CC00, D000, D400, D800, DC00

3.5.6.9 Reserved Memory Length

This section shows the status of your memory resources.

The choices: 8K, 16K, 32K, 64K

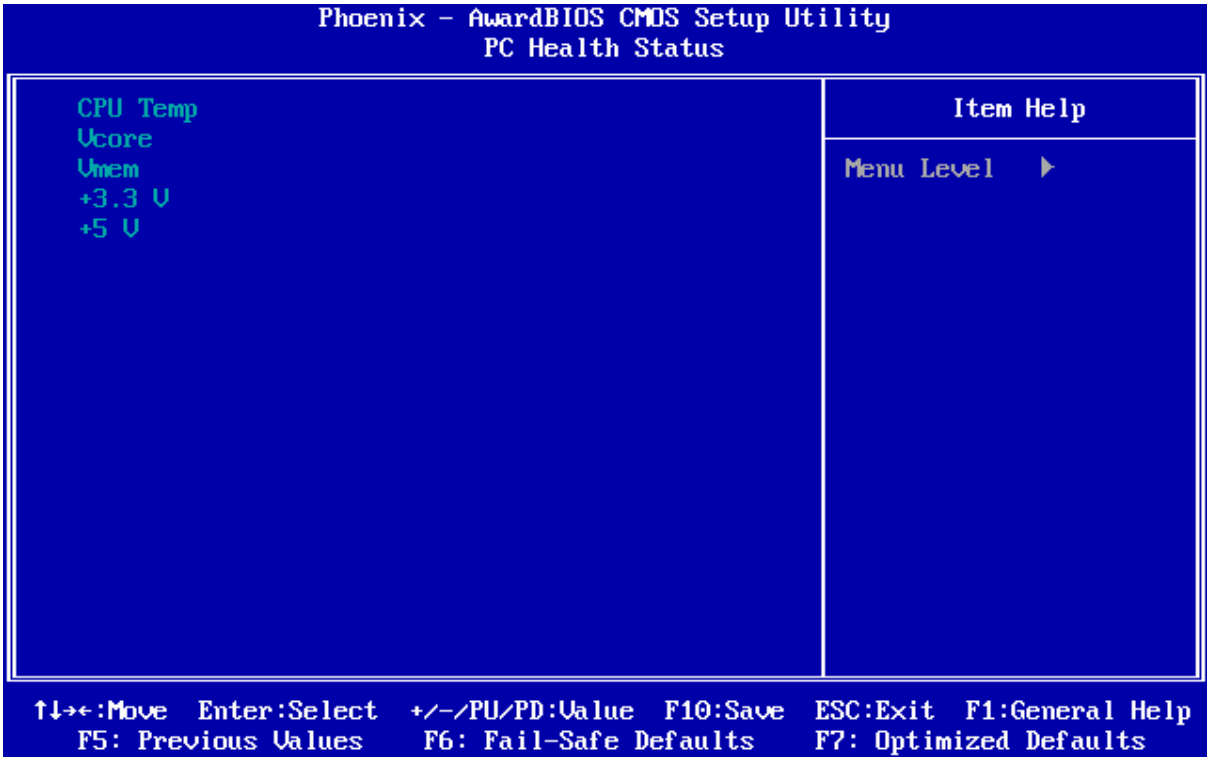
3.5.6.10 PCI/VGA Palette Snoop

This item allows you to decide if your graphics card should allow VGA palete snooping by a fixed function display card. It is only useful if your use a fixed function display card that requires a VGA-compatible graphics card to be present (i.e. MPEG decoder card).

The choices: Enabled, Disabled.

3.5.7 PC Health Status

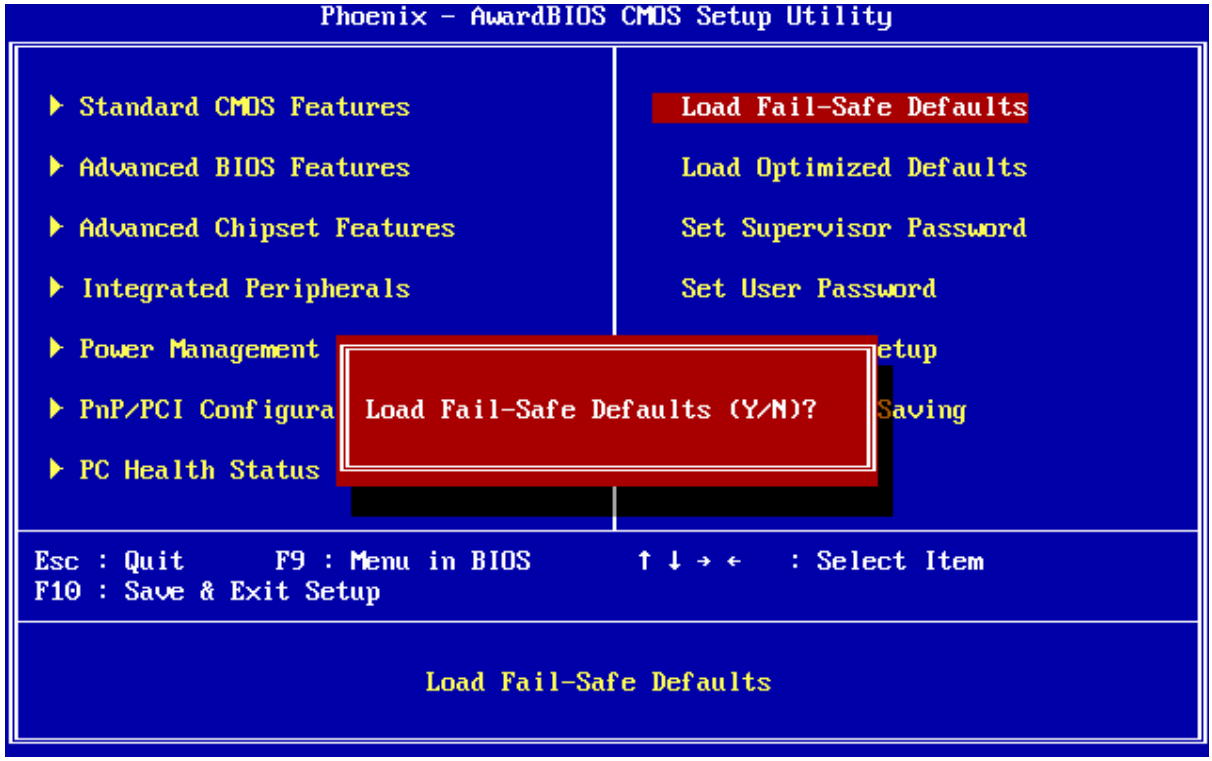
This section shows the status of your CPU and System.



3.5.8 Load Fail-Safe Defaults

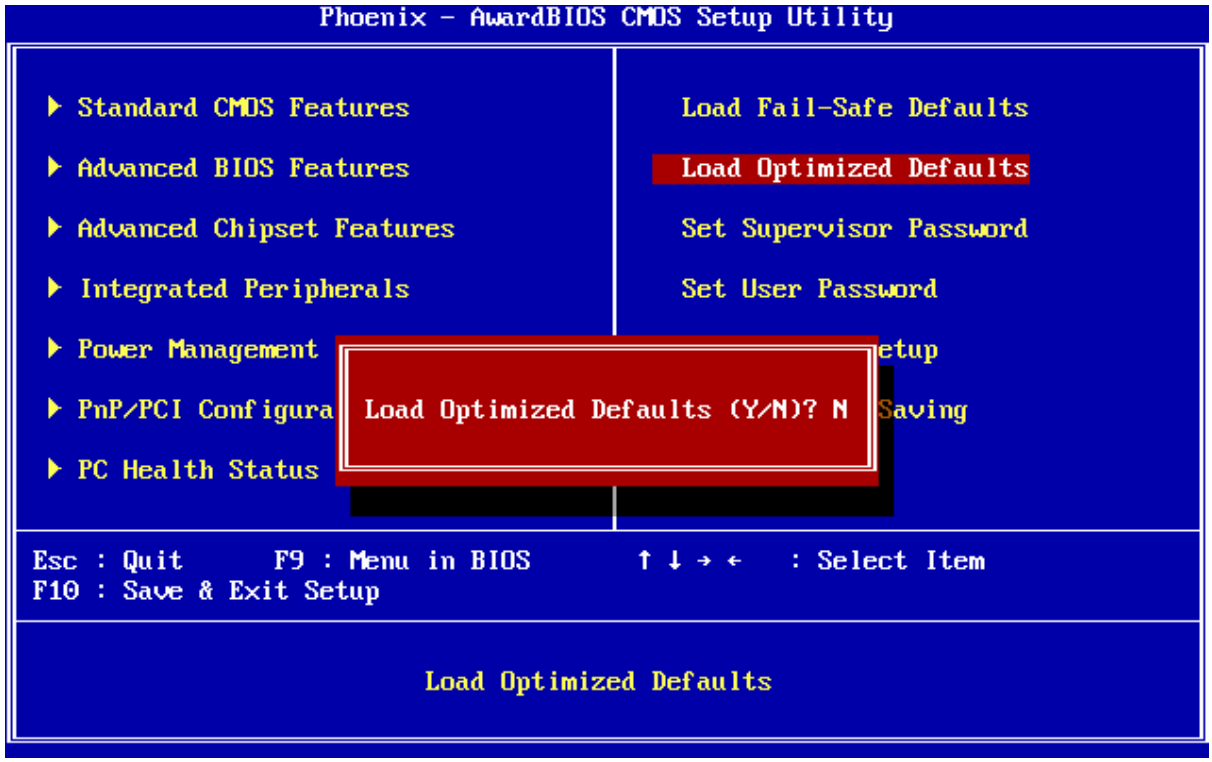
Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Press <Y> to load the BIOS default values for the most stable, minimal-performance system operations.



3.5.9 Load Optimized Defaults

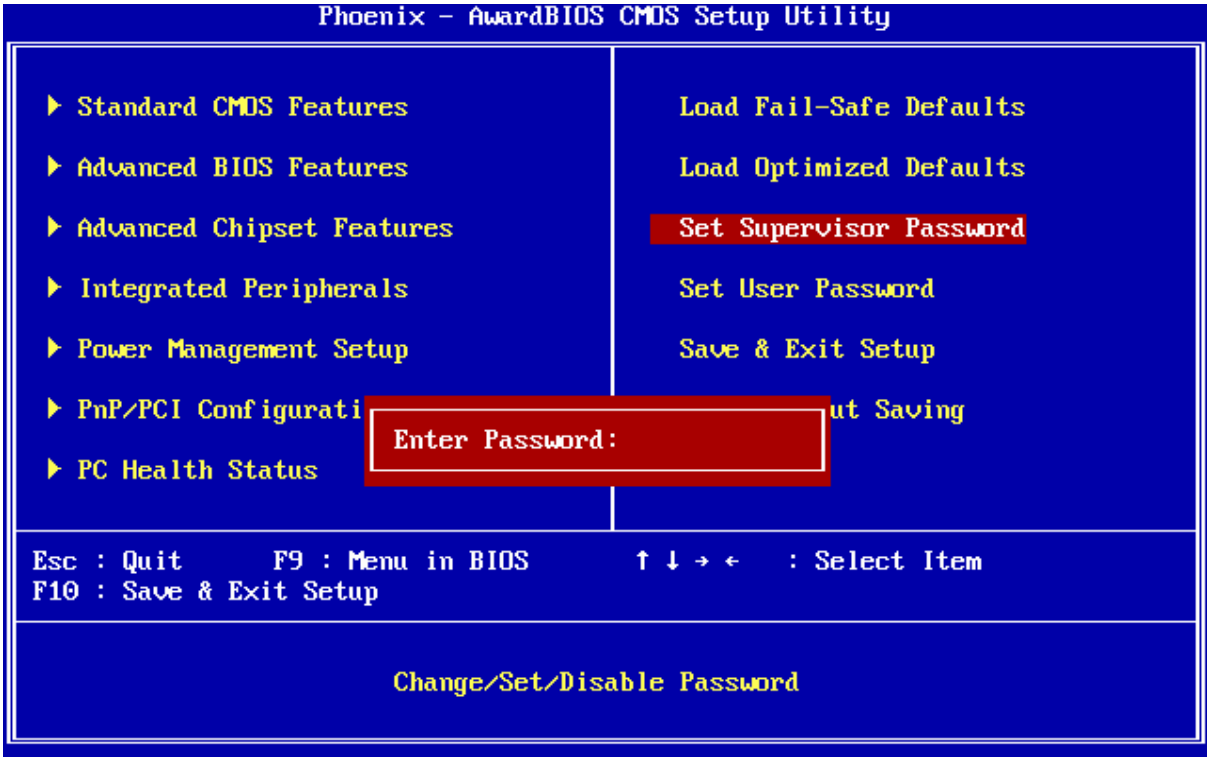
Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs. Press <Y> to load the default values setting for optimal performance system operations.



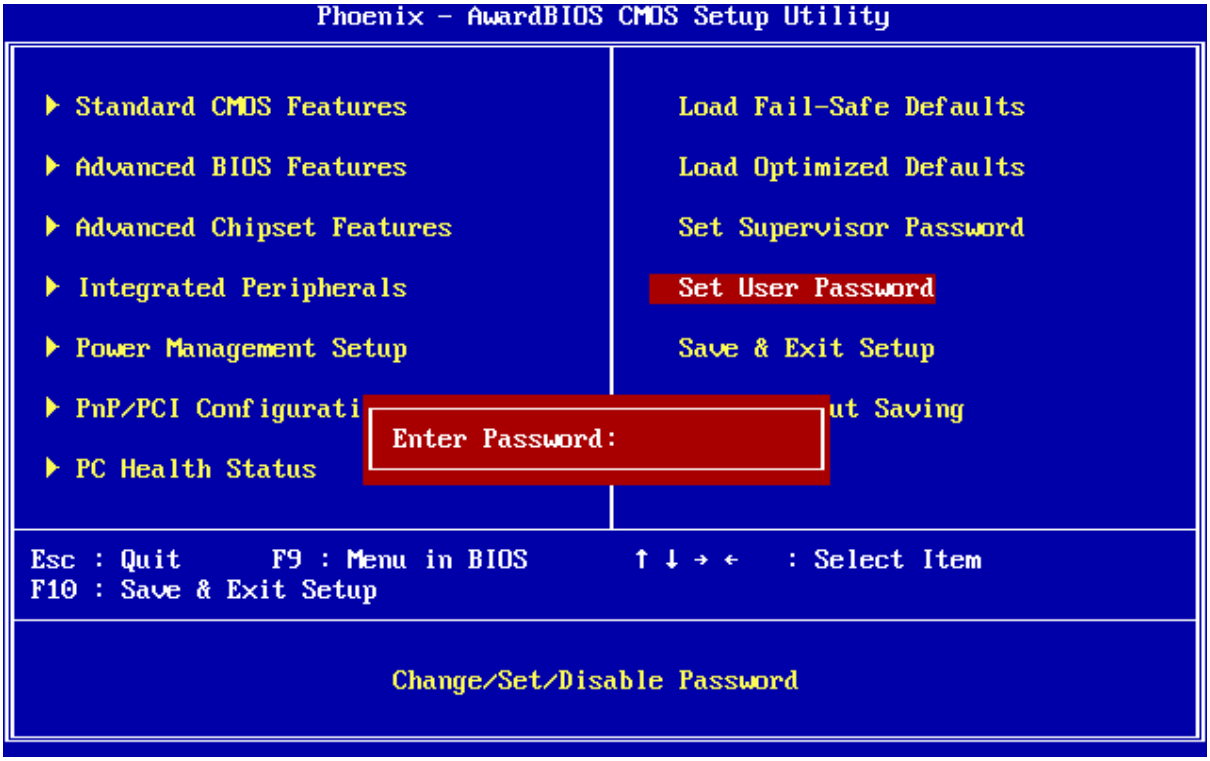
3.5.10 Set Supervisor / User Password

You can set either supervisor or user password, or both of them.

Supervisor Password: able to enter/change the options of setup menus.



User Password: able to enter but no right to change the options of setup menus.



Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

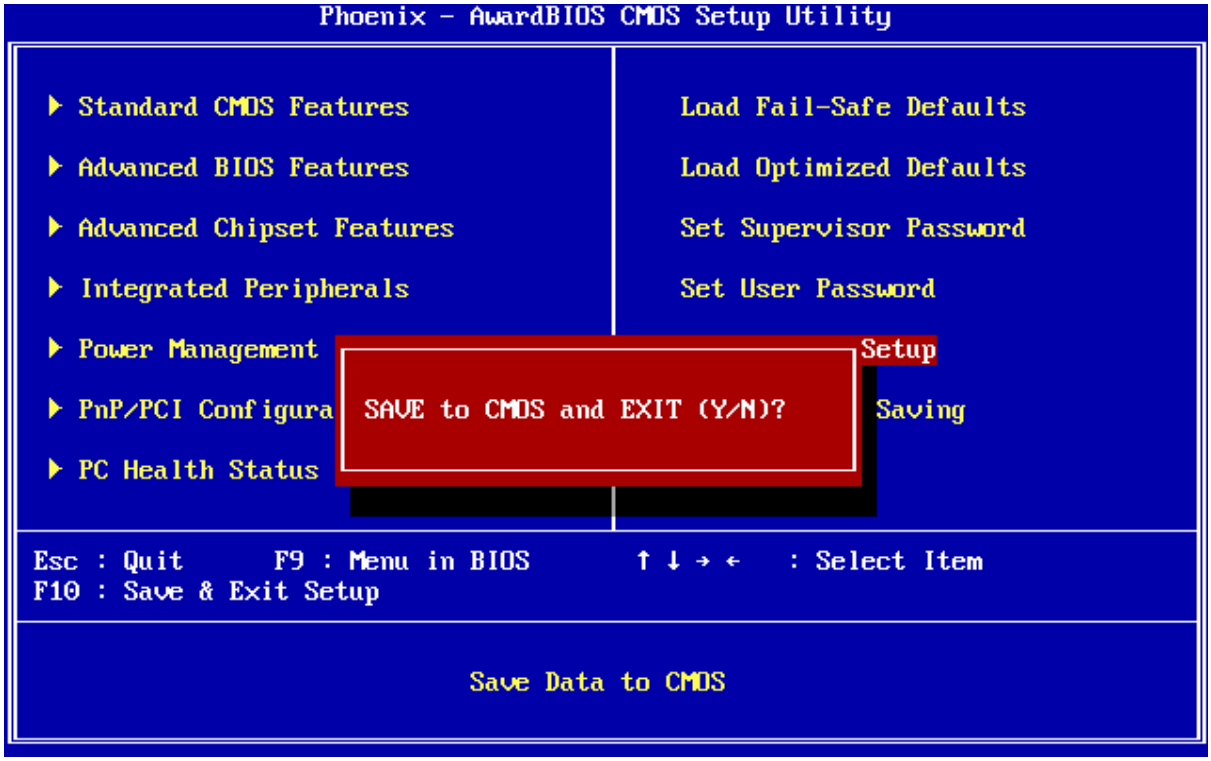
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup

3.5.11 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

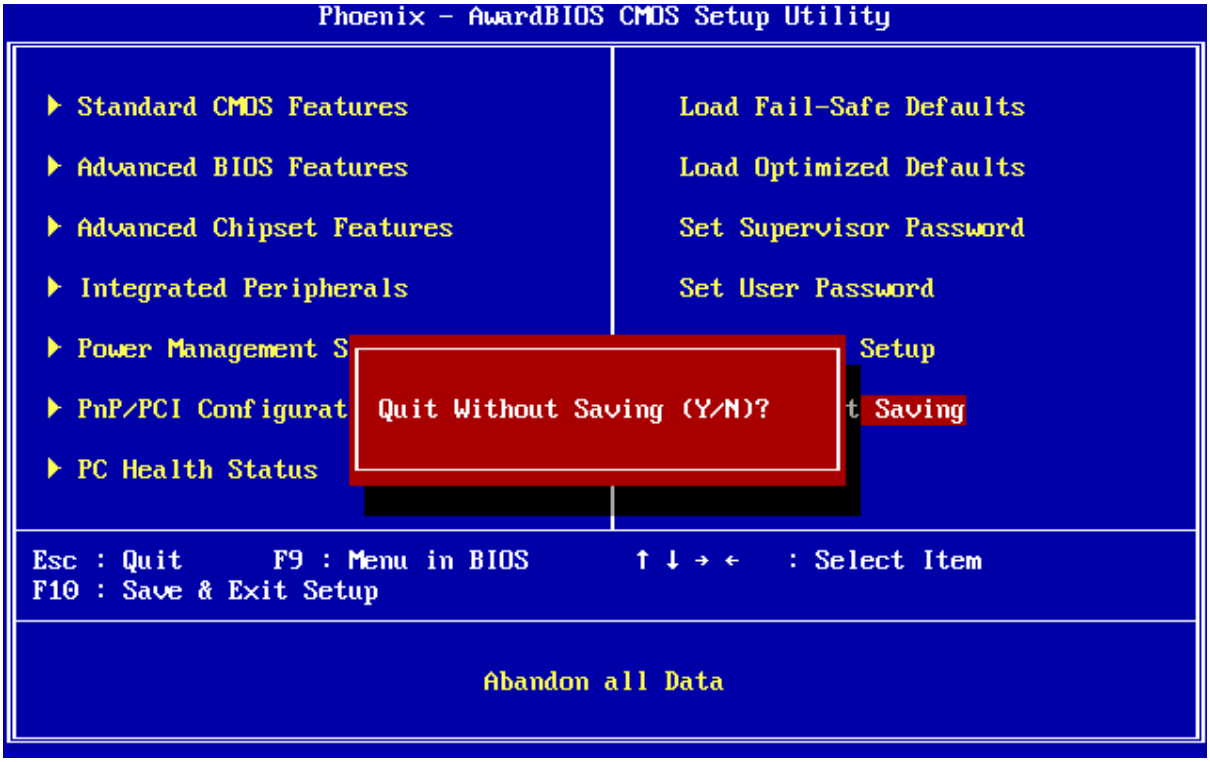
Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

The system is restarted after saving the values.



3.5.12 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.



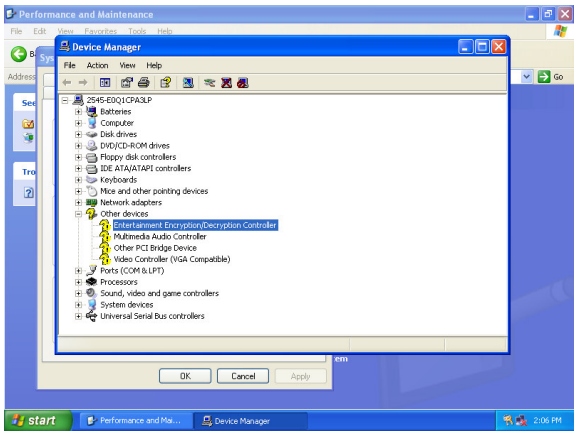
4. Drivers Installation

Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

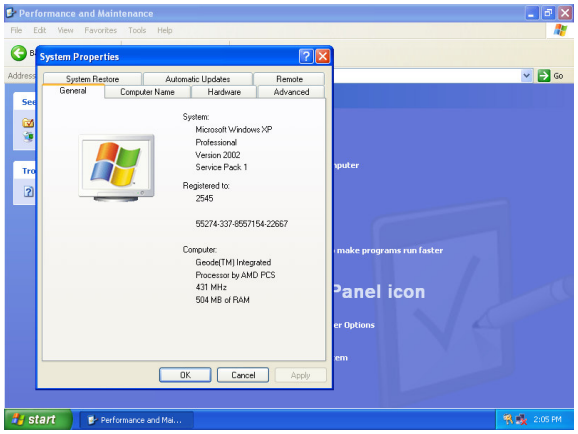
4.1 Install Chipset Driver (For AMD GX3)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\AMD\GX3**.

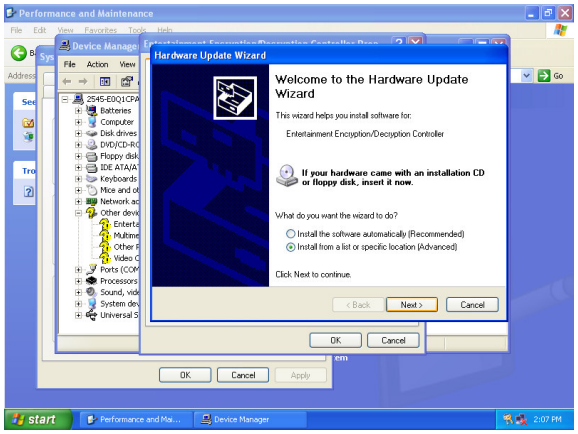
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



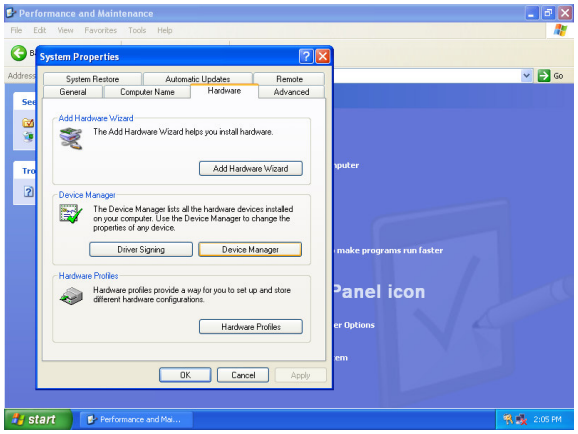
Step 3. Select **Entertainment…** to **Reinstall Driver**.



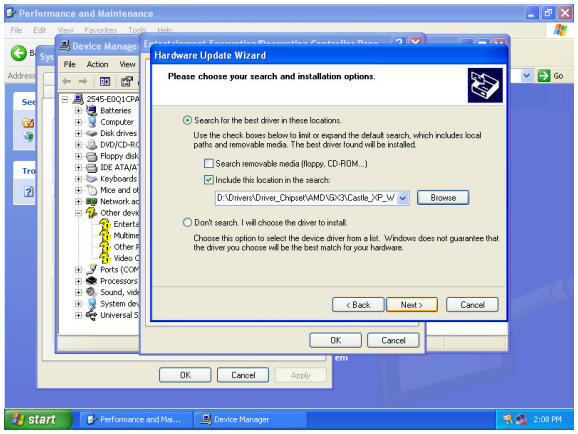
Step1. Click **Start** of the task bar, then the **System** of **Performance and Maintenance** in **Control Panel**.



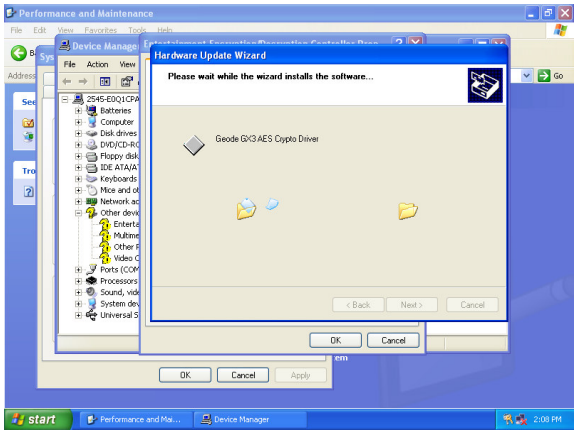
Step 4. Select the **Advanced** item and click **Next**.



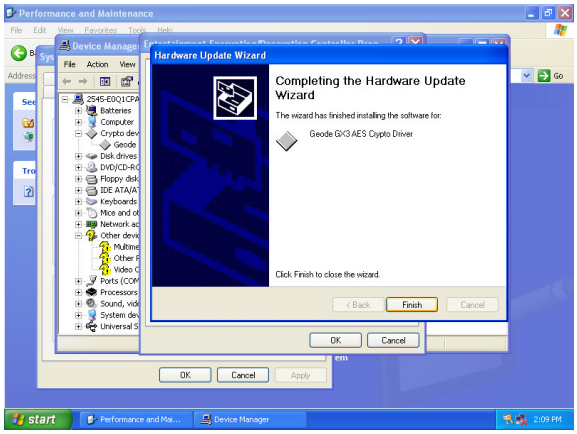
Step 2. Click **Device Manager** of **Hardware**.



Step 5. Select the specific location to **Next**.



Step6. The setup will install automatically.

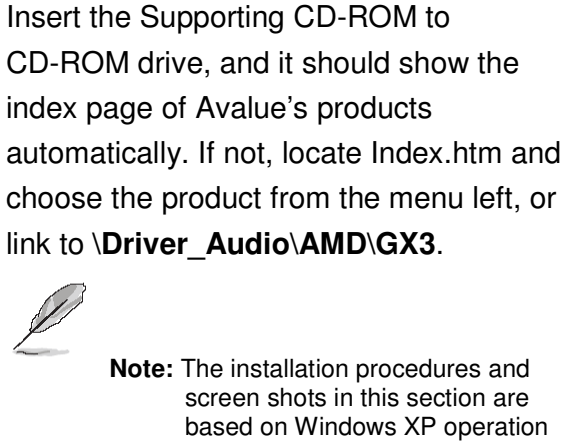


Step7. Click **Finish** to complete the setup.

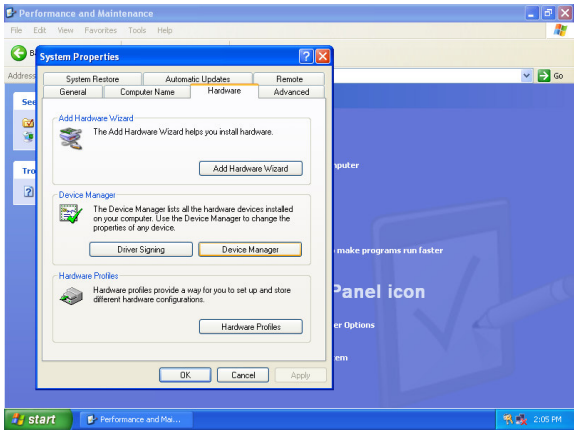
4.2 Install Audio Driver (For AMD GX3)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Audio\AMD\GX3**.

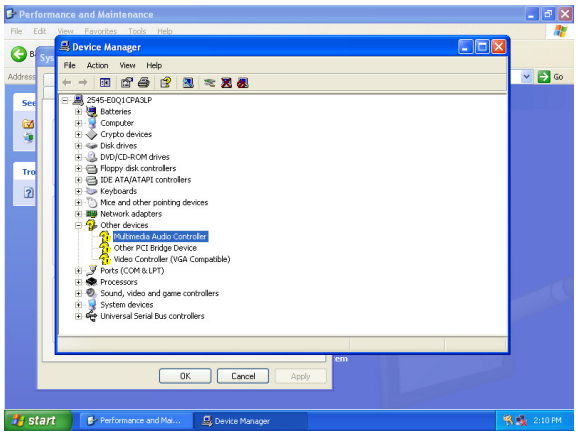
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



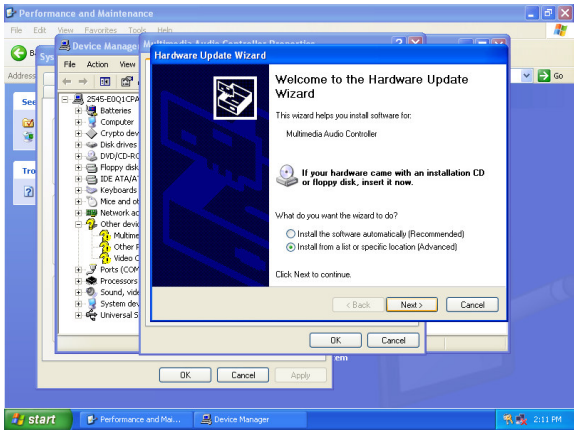
Step1. Click **Start** of the task bar, then the **System** of **Performance and Maintenance** in **Control Panel**.



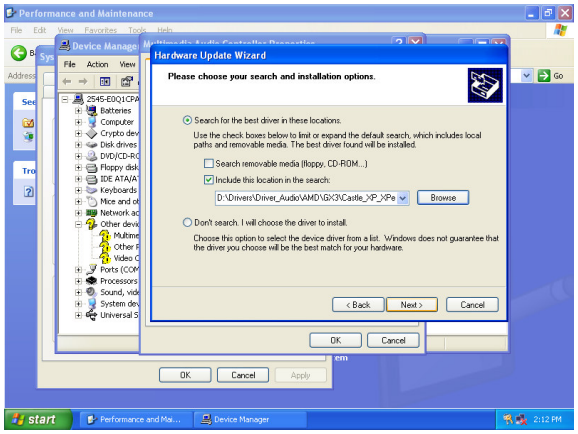
Step 2. Click **Device Manager** of **Hardware**.



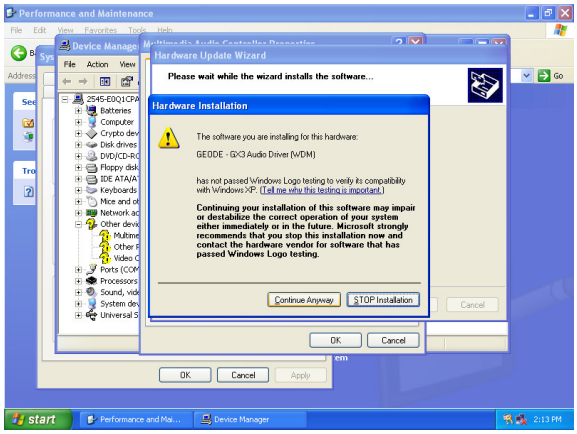
Step 3. Select **Multimedia Audio Controller** to **Reinstall Driver**.



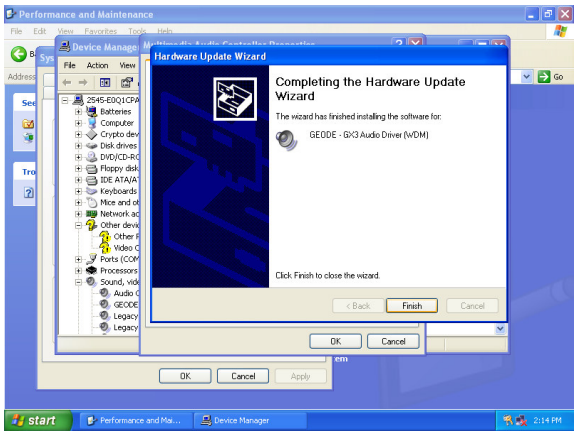
Step 4. Select the **Advanced** item and click **Next**.



Step 5. Select the specific location to **Next**.



Step6. Click **Continue Anyway** to run the installation.

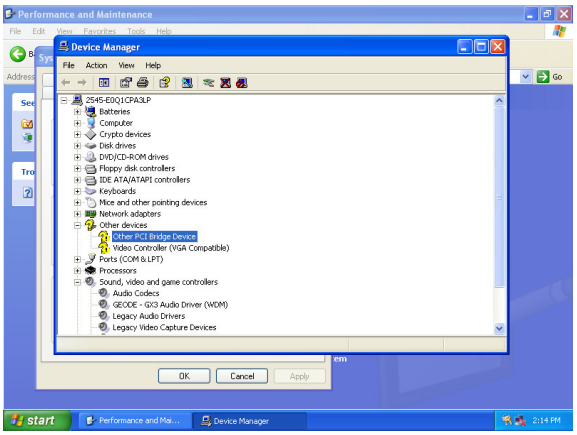


Step7. Click **Finish** to complete the setup.

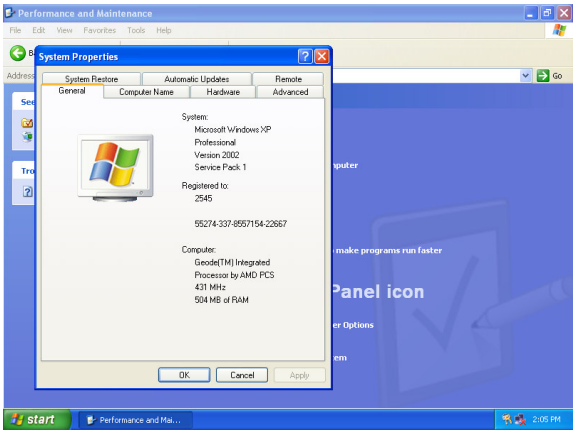
4.3 Install PCI to ISA Bridge Driver (For ITE IT8888)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\AMD\GX3\PCI to ISA Bridge**.

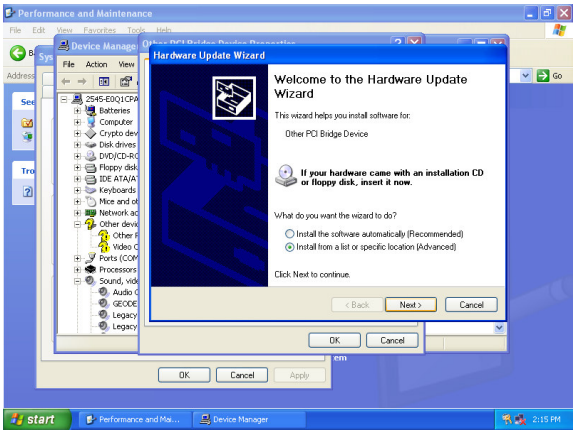
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



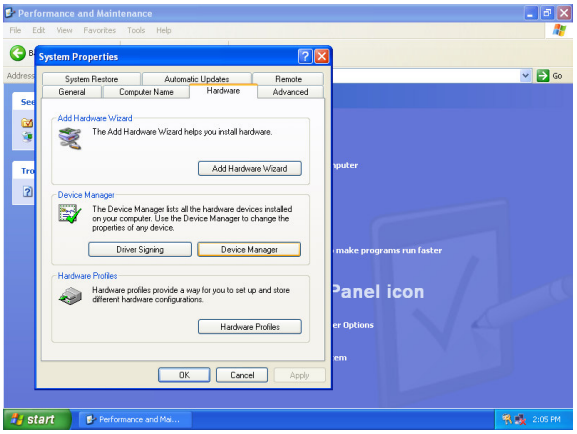
Step 3. Select **Other PCI Bridge Device** to **Reinstall Driver**.



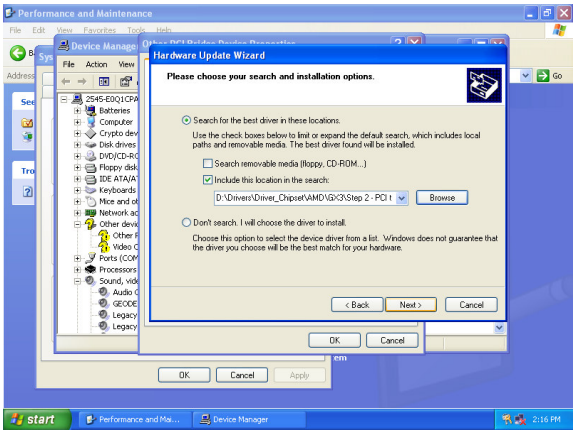
Step1. Click **Start** of the task bar, then the **System** of **Performance and Maintenance** in **Control Panel**.



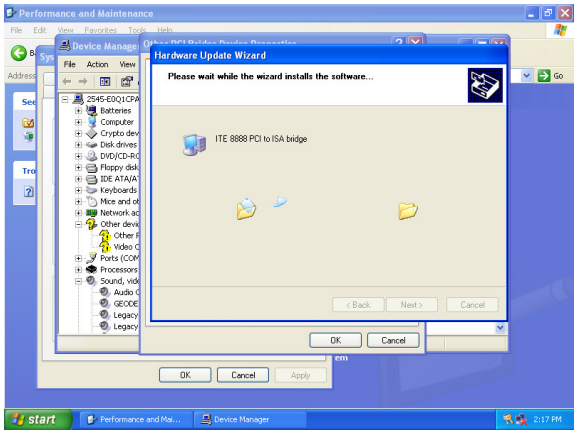
Step 4. Select the **Advanced** item and click **Next**.



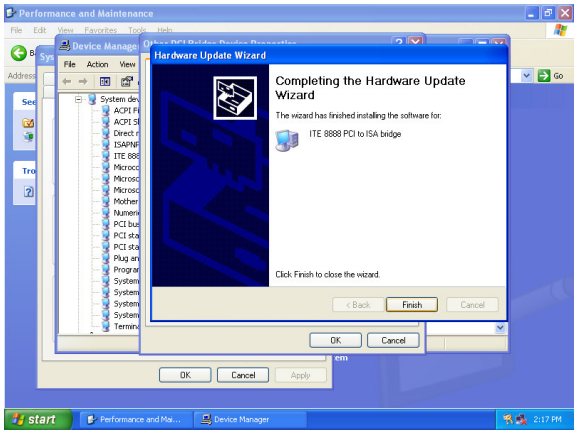
Step 2. Click **Device Manager** of **Hardware**.



Step 5. Select the specific location to **Next**.



Step6. The setup will install automatically.

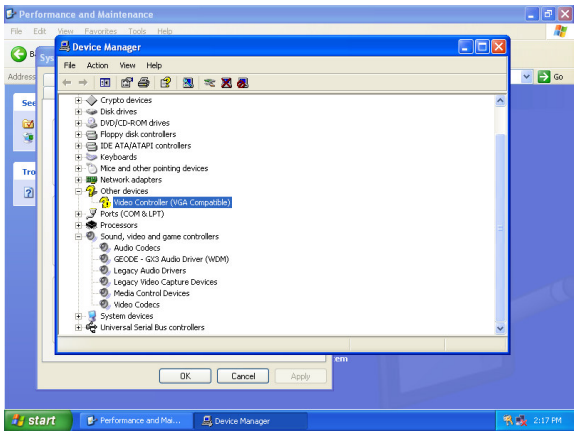


Step7. Click **Finish** to complete the setup.

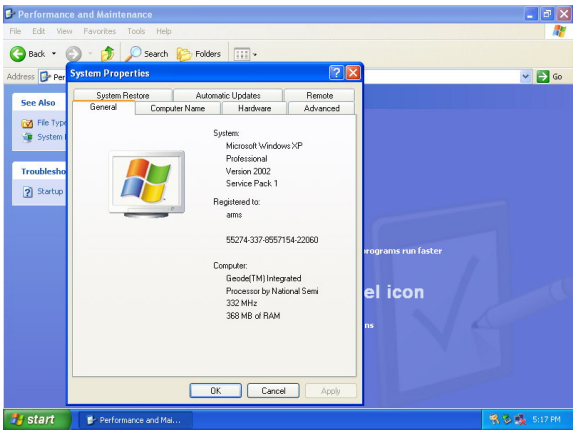
4.4 Install Display Driver (For AMD GX3)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Video\AMD\GX3**.

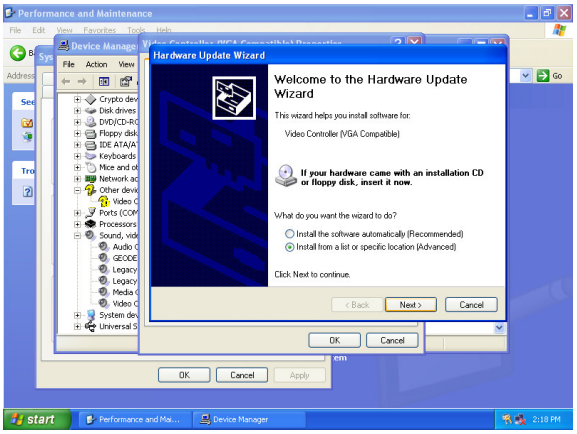
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



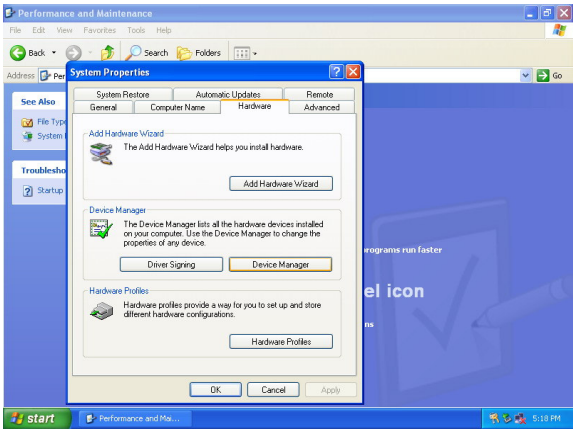
Step 3. Select **Video Controller (VGA Compatible** to **Reinstall Driver**.



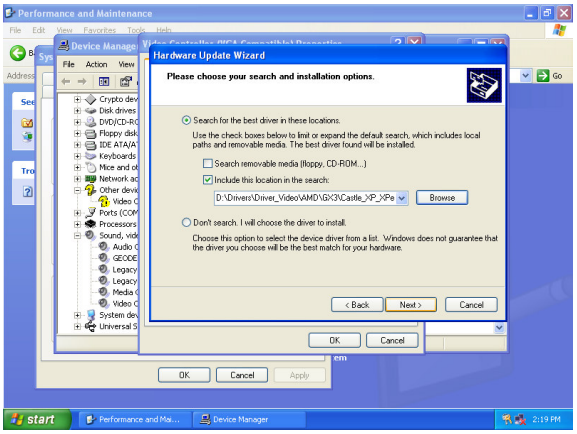
Step1. Click **Start** of the task bar, then the **System** of **Performance and Maintenance** in **Control Panel**.



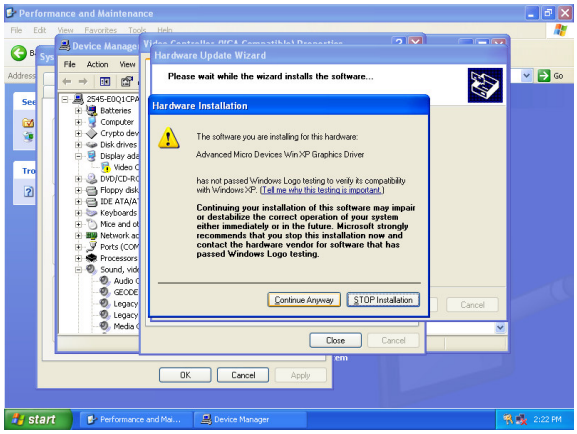
Step 4. Select the **Advanced** item and click **Next**.



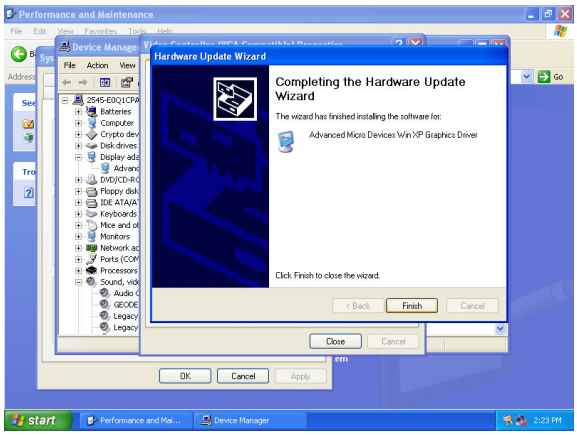
Step 2. Click **Device Manager** of **Hardware**.



Step 5. Select the specific location to **Next**.



Step6. Click **Continue Anyway** to run the installation.

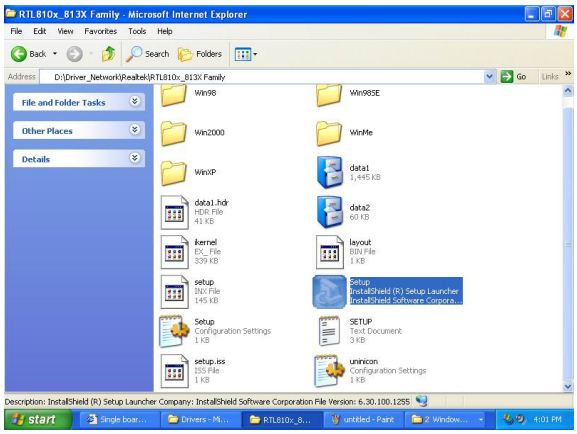


Step7. Click **Finish** to complete the setup.

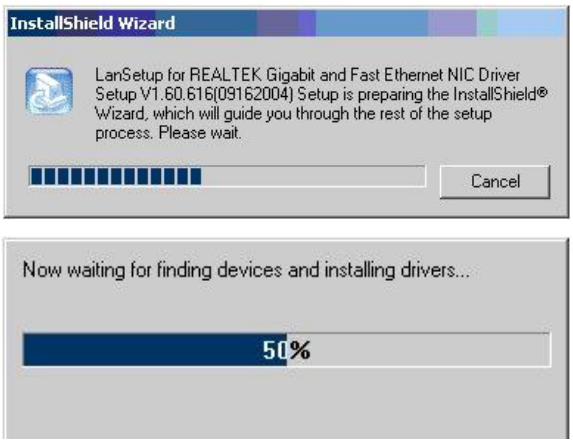
4.5 Install Ethernet Driver (For Realtek RTL810x, RTL813x Family)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **Driver_Network\Realtek\ RTL810x_813X Family**.

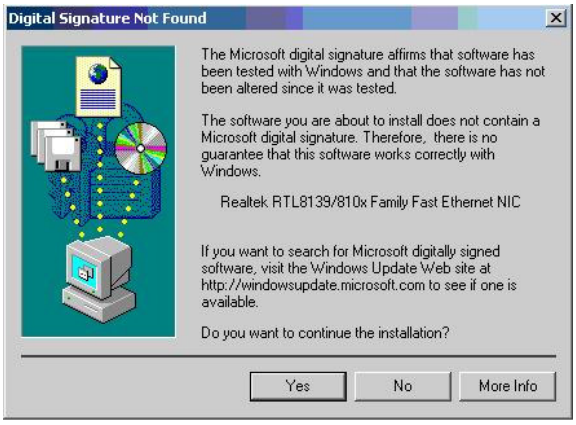
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



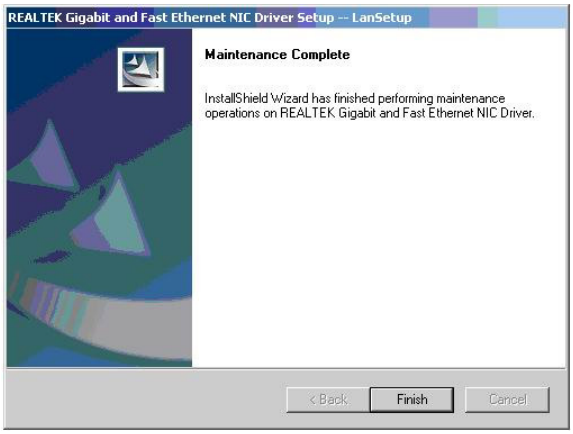
Step 1. Locate 「\Driver_Network\Realtek\ RTL810x_813X Family\Setup.exe」.



Step 2. Setup executing.

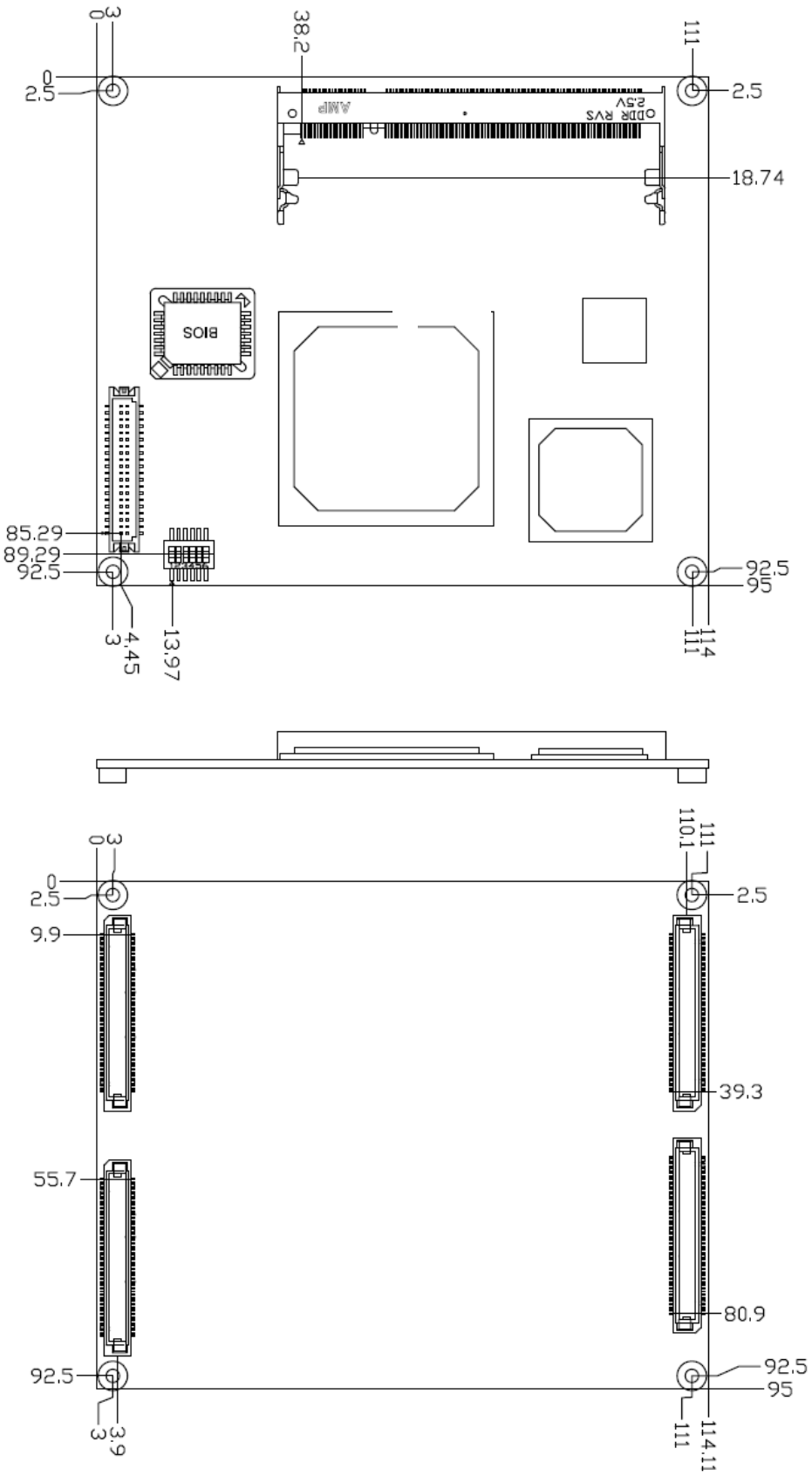


Step 3. Click **Yes** to continue the installation.



Step 4. Click **Finish** to complete the setup.

5. Measurement Drawing


3
0
38.2
111
0
2.5
2.5
18.74
BIOS
85.29
89.29
92.5
92.5
95
3
4.45
13.97
111
114
111
3
0
111
110.1
0
2.5
2.5
9.9
39.3
55.7
80.9
92.5
92.5
95
3
3.9
111
114.11

(Unit: mm)

Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: AWARD BIOS POST Messages

Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE OR PRESS DEL TO ENTER SETUP

Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

The following messages are examples of messages including errors detected by the BIOS during POST and a description of what they mean and/or what you may do to correct the error.

1. CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

2. CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

5. DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

7. EISA Configuration Checksum Error
PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

8. EISA Configuration Is Not Complete
PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

10. ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

12. Invalid EISA Configuration
PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

13. KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

14. Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

15. Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

17. Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

18. OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

19. OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

20. PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

23. Should Be Empty But EISA Board Found
PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

24. Should Have EISA Board But Not Found
PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

25. Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

27. Wrong Board In Slot
PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

28. FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.
29. FLOPPY DISK(S) fail (40) → Floppy Type dismatch.
30. Hard Disk(s) fail (80) → HDD reset failed.
31. Hard Disk(s) fail (40) → HDD controller diagnostics failed.
32. Hard Disk(s) fail (20) → HDD initialization error.
33. Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.
34. Hard Disk(s) fail (08) → Sector Verify failed.
35. Keyboard is locked out - Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

36. Keyboard error or no keyboard present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

37. Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

38. BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFH is bad.

39. Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

40. POST Codes

Please take reference to Phoenix-Award website for the latest post codes.

http://www.phoenix.com/en/Customer+Services/BIOS/AwardBIOS/Award+Error+Codes.htm

40.1 Normal POST Code

Note: EISA POST codes are typically output to port address 300h. ISA POST codes are output to port address 80h.

Code (hex)	Name	Description
C0	Turn Off Chipset and CPU test	OEM Specific-Cache control cache Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, overflow, the BIOS sets each flag, verifies They are set, then turns each flag off and verifies it is off. Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00. RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory Presence	First block memory detect OEM Specific-Test to size on-board memory. Early chip set initialization Memory presence test OEM chip set routines clear low 64K of memory Test first 64K memory.
C2	Early Memory Initialization	OEM Specific- Board Initialization
C3	Extend Memory DRAM select	OEM Specific- Turn on extended memory Initialization Cyrix CPU initialization, Cache initialization
C4	Special Display Handling	OEM Specific- Display/Video Switch handling so that switch handling display switch errors never occurs
C5	Early Shadow	OEM specific- Early shadow enable for fast boot
C6	Cache presence test	External cache size detection
CF	CMOS Check	CMOS checkup
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot.
BF	Program Chip Set	To program chipset from defaults values
E1-EF	Setup Pages	E1- Page 1, E2 - Page 2, etc.
1	Force load Default to chipset	Chipset defaults program
2	Reserved	

Code (hex)	Name	Description
3	Early Superio Init	Early Initialized the super IO
4	Reserved	
5	Blank video	Reset Video controller
6	Reserved	
7	Init KBC	Keyboard controller init
8	KB test	Test the Keyboard
9	Reserved	
A	Mouse Init	Initialized the mouse
B	Onboard Audio init	Onboard audio controller initialize if exist
C	Reserved	
D	Reserved	
E	CheckSum Check	Check the integrity of the ROM, BIOS and message
F	Reserved	
10	Auto detect EEPROM	Check Flash type and copy flash write/erase routines to 0F000h segments
11	Reserved	
12	CMOS Check	Check CMOS Circuitry and reset CMOS
13	Reserved	
14	Chipset Default load	Program the chipset registers with CMOS values
15	Reserved	
16	Clock Init	Init onboard clock generator
17	Reserved	
18	Identify the CPU	Check the CPU ID and init L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM Init	First step initialize if single CPU onboard
1E	Reserved	
1F	Re-initial KB	Re-init KB
20	Reserved	
21	HPM init	If support HPM, HPM get initialized here
22	Reserved	
23	Test CMOS Interface and battery Status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset
24	Reserved	

Code (hex)	Name	Description
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initial KBC and setup BIOS data area
28	Reserved	
29	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 Mouse setup	Setup PS2 Mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Test DMA Controller 0
36	Reserved	
37	Test DMA Controller 1	Test DMA Controller 1
38	Reserved	
39	Test DMA Page Registers	Test DMA Page Registers.
3A	Reserved	
3B	Reserved	
3C	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
3D	Reserved	
3E	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
3F	Reserved	
40	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
41	Reserved	
42	Reserved	

Code (hex)	Name	Description
43	Test Stuck 8259's Interrupt Bits Test 8259 Interrupt Functionality	Turn off interrupts then verify no interrupt mask register is on. Force an interrupt and verify the interrupt occurred.
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests an clear EISA mode flag.
48	Reserved	
49	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns. NOTE: This test is skipped in EISA mode and can be skipped with ESC key in ISA mode.
4F	Reserved	
50	USB init	Initialize USB controller
51	Reserved	
52	Memory Test	Test all memory of memory above 1MB using Virtual 8086 mode, page mode and clear the memory
53	Reserved	
54	Reserved	
55	CPU display	Detect CPU speed and display CPU vendor specific version string and turn on all necessary CPU features
56	Reserved	
57	PnP Init	Display PnP logo and PnP early init
58	Reserved	
59	Setup Virus Protect	Setup virus protect according to Setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializing onboard superIO

Code (hex)	Name	Description
5E	Reserved	
5F	Reserved	
60	Setup enable	Display setup message and enable setup functions
61	Reserved	
62	Reserved	
63	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
64	Reserved	
65	PS2 Mouse special	Special treatment to PS2 Mouse port
66	Reserved	
67	ACPI init	ACPI sub-system initializing
68	Reserved	
69	Setup Cache Controller	Initialize cache controller.
6A	Reserved	
6B	Setup Entering	Enter setup check and auto- configuration check up
6C	Reserved	
6D	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives.
6E	Reserved	
6F	FDD install	Install FDD and setup BIOS data area parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialize Hard Drive & Controller	Initialize hard drive controller and any drives.
74	Reserved	
75	Install HDD	IDE device detection and install
76	Reserved	
77	Detect & Initialize Serial/Parallel Port	Initialize any serial and parallel ports (also game port).
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
7B	Reserved	
7C	HDD Check for Write protection	HDD check out

Code (hex)	Name	Description
7D	Reserved	
7E	Reserved	
7F	POST error check	Check POST error and display them and ask for user intervention
80	Reserved	
81	Reserved	
82	Security Check	Ask password security (optional).
83	Write CMOS	Write all CMOS values back to RAM and clear screen.
84	Pre-boot Enable	Enable parity checker. Enable NMI, Enable cache before boot.
85	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
86	Reserved	
87	Reserved	
88	Reserved	
89	Reserved	
8A	Reserved	
8B	Reserved	
8C	Reserved	
8D	Reserved	
8E	Reserved	
8F	Reserved	
90	Reserved	
91	Reserved	
92	Reserved	
93	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
94	Final Init	Final init for last micro details before boot
95	Special KBC patch	Set system speed for boot. Setup NumLock status according to Setup
96	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

40.2 Quick POST Codes

Code (hex)	Name	Description
65	Init onboard device	Early Initialized the super IO. Reset Video controller. Keyboard controller init Test the Keyboard Initialized the mouse Onboard audio controller initialize if exist. Check the integrity of the ROM, BIOS and message Check Flash type and copy flash write/erase routines to 0F000h segments Check CMOS Circuitry and reset CMOS Program the chipset registers with CMOS values Init onboard clock generator
66	Early System setup	Check the CPU ID and init L1/L2 cache. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and 10 initialize INT 00h-1Fh according to INT_TBL First step initialize if single CPU onboard. Re-init KB If support HPM, HPM get initialized here.
67	KBC and CMOS Init	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset. Final Initial KBC and setup BIOS data area.
68	Video Init	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter. Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
69	8259 Init	Init 8259 channel 1 and mask IRQ 9
6A	Memory test	Quick Memory Test
6B	CPU Detect and IO init	CPU vendor specific version string and turn on all necessary CPU features Display PnP logo and PnP early init Setup virus protect according to Setup. If required, will auto load Awdflash.exe in POST Initializing onboard superIO
6C	Reserved	
6D	Reserved	
6E	Reserved	
6F	Reserved	
70	Setup Init	Display setup message and enable setup functions Detect if mouse is present, initialize mouse, install interrupt vectors. Special treatment to PS2 Mouse port ACPI sub-system initializing
71	Setup Cache Controller	Initialize cache controller.

Code (hex)	Name	Description
72	Install FDD	Enter setup check and auto11 configuration check up Initialize floppy disk drive controller and any drives. Install FDD and setup BIOS data area parameters
73	Install FDD	Initialize hard drive controller and any drives. IDE device detection and install Initialize any serial and parallel ports (also game port).
74	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
75	HDD Check for Write protection	HDD check out
76	Reserved	
77	Display POST error	Check POST error and display them and ask for user intervention Ask password security (optional).
78	CMOS and Option ROM Init	Write all CMOS values back to RAM and clear screen. Enable parity checker Enable NMI, Enable cache before boot. Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
79	Reserved	
7A	Reserved	
7B	Reserved	
7C	Reserved	
7D	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
7E	Final Init	Final init for last micro details before boot
7F	Special KBC patch	Set system speed for boot. Setup NumLock status according to Setup.
80	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

40.3S4 POST Codes

Code (hex)	Name	Description
5A	Early Chipset Init	Early Initialized the super IO. Reset Video controller. Keyboard controller init. Test the Keyboard Initiated the mouse
5B	CMOS Check	Check CMOS Circuitry and reset CMOS
5C	Chipset default Prog	Program the chipset registers with CMOS values. Init onboard clock generator
5D	Identify the CPU	Check the CPU ID and init L1/L2 cache Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and INT 00h-1Fh according to INT_TBL. First step initialize if single CPU Onboard. Re-init KB If support HPM, HPM get initialized Here.
5E	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and INT 00h-1Fh according to INT_TBL. First step initialize if single CPU Onboard. Re-init KB If support HPM, HPM get initialized here.
5F	Test CMOS Interface and Battery status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset.
60	KBC final Init	Final Initial KBC and setup BIOS data area
61	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
62	Video memory test	Test video memory, write sign-on Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
63	Setup PS2 mouse and test DMA	Setup PS2 Mouse and reset KB Test DMA channel 0
64	Test 8259	Test 8259 channel 1 and mask IRQ 9
65	Init Boot Device	Detect if mouse is present, initialize mouse, install interrupt vectors. Special treatment to PS2 Mouse port ACPI sub-system initializing Initialize cache controller.
66	Install Boot Devices	Enter setup check and auto-configuration check up Initialize floppy disk drive controller and any drives. Install FDD and setup BIOS data area Parameters Initialize hard drive controller and any drives. IDE device detection and install
67	Cache Init	Cache init and USB init
68	PM init	PM initialization
69	PM final Init and issue SMI	Final init Before resume
FF	Full on	

40.4 BootBlock POST Codes

Code (hex)	Name	Description
1	Base memory test	Clear base memory area (0000:0000--9000:ffffh)
5	KB init	Initialized KBC
12	Install interrupt vectors	Install int. vector (0-77), and initialized 00-1fh to their proper place
0D	Init Video	Video initializing
41	Init FDD	Scan floppy and media capacity for onboard superIO
FF	Boot	Load boot sector