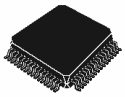
STM32F313xx

ARM Cortex-M4 32b MCU+FPU, up to 256KB Flash+48KB SRAM 4 ADCs, 2 DACs, 7 comp., 4 PGA, timers, 1.8 V operation

Data brief

Features

- Core: ARM® 32-bit Cortex™-M4F CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit).
- Operating conditions:
  - V_{DD}: 1.8V +/- 8%
  - V_{DDA} voltage range: 1.65 to 3.6 V
- Memories
  - 128 to 256 Kbytes of Flash memory
  - Up to 40 Kbytes of SRAM on data bus with HW parity check
  - 8 Kbytes of SRAM on instruction bus with HW parity check (CCM)
- CRC calculation unit
- Reset and supply management
  - Low power modes: Sleep and Stop
  - VBAT supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 87 fast I/Os
  - All mappable on external interrupt vectors
  - Several 5 V-tolerant
- 12-channel DMA controller
- Up to four ADC 0.20 µS (up to 39 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 1.8 to 3.6 V
- Up to two 12-bit DAC channels with analog supply from 2.4 to 3.6 V
- Seven fast rail-to-rail analog comparators with analog supply from 1.65 to 3.6 V
- Up to four operational amplifiers that can be used in PGA mode, all terminal accessible with analog supply from 2.4 to 3.6 V
- Support for up to 23 capacitive sensing keys supporting touchkey, linear and rotary touchsensors



LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)

- Up to 13 timers
  - One 32-bit timer and two 16-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Up to two 16-bit 6-channel advanced-control timers, with up to 6 PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation and emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
  - Up to two 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm, periodic wakeup from Stop
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I^2C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - Up to three SPIs, two with multiplexed I^2S interface, 4 to 16 programmable bit frame
  - Infrared Transmitter
- Serial wire debug, JTAG, Cortex-M4F ETM
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F313xx	STM32F313CC, STM32F313RC, STM32F313VC

Contents

List of tables

List of figures

1 Introduction

This databrief provides the ordering information and mechanical device characteristics of the STM32F31x microcontrollers.

This STM32F31x databrief should be read in conjunction with the STM32F31x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the www.arm.com website at the following address:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.subset.cortexm.m4/index.html

2 Description

The STM32F313xx family is based on the high-performance ARM® Cortex™-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 48 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to four fast 12-bit ADCs (5 Msps), up to seven comparators, up to four operational amplifiers, up to two DAC channels, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and two timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to two I^2Cs, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss on STM32F313xx devices), three USARTs, up to two UARTsand CAN. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F313xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F313xx family offers devices in three packages ranging from 48 pins to 100 pins.

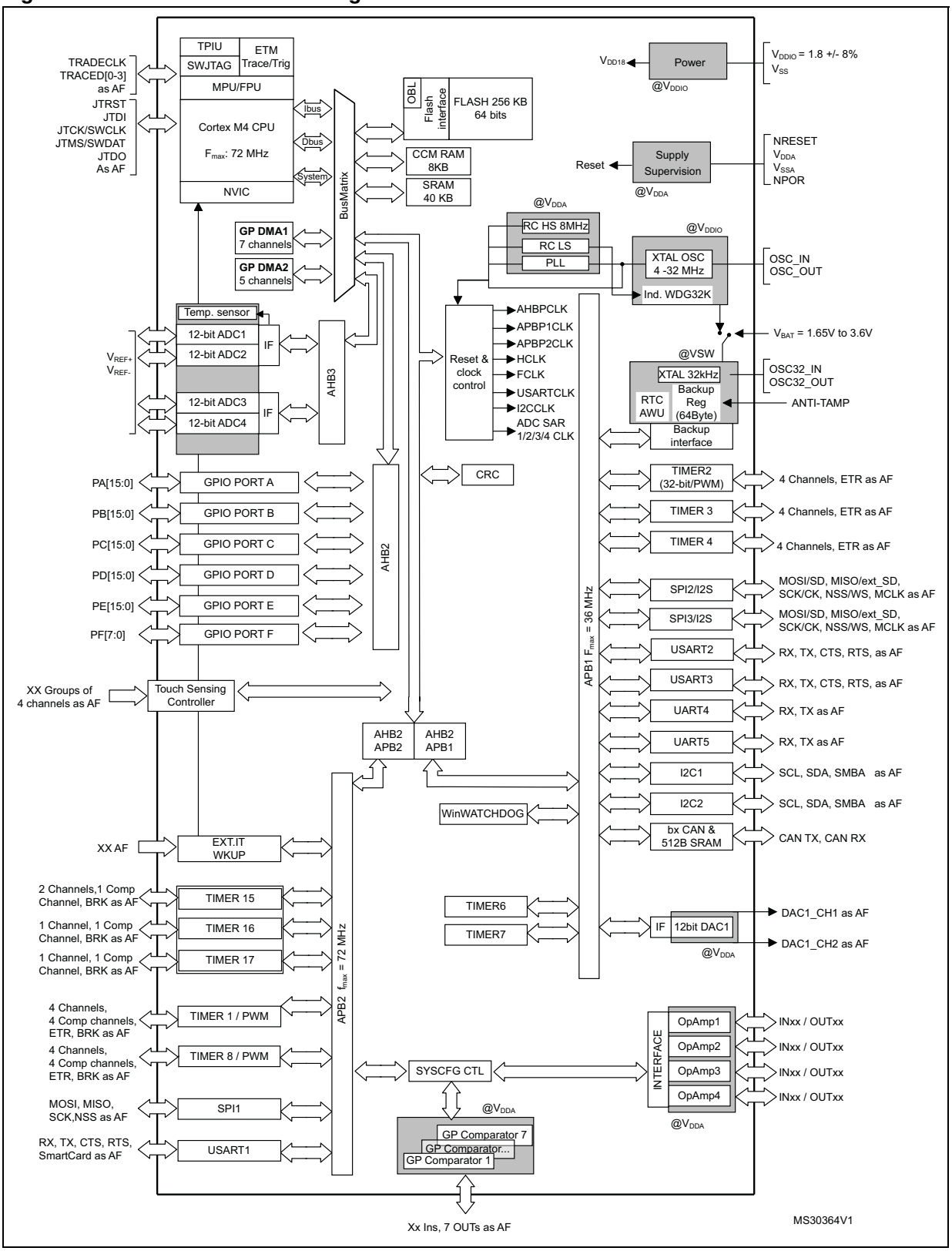
The set of included peripherals changes with the device chosen.

Table 2. STM32F31x family device features and peripheral counts

Peripheral		STM32F 313Cx		STM32F 313Rx		STM32F 313Vx	
Flash (Kbytes)		128	256	128	256	128	256
SRAM (Kbytes) on data bus		32	40	32	40	32	40
SRAM (Kbytes) on instruction bus (CCM: core coupled memory)		8					
Timers	Advanced control	2 (16-bit)					
	General purpose	5 (16-bit) 1 (32 bit)					
	Basic	2 (16-bit)					
Comm. interfaces	SPI(I2S)(1)	3(2)					
	I^2C	2					
	USART	3					
	UART	2					
	CAN	1					
GPIOs	Normal I/Os (TC,TTa)	19		26		44	
	5 volts Tolerant I/Os (FT, Ftf)	17		25		42	
DMA channels		12					
12-bit ADCs		4					
12-bit DAC channels		2					
Analog comparator		7					
Operational amplifiers		4					
CPU frequency		72 MHz					
Operating voltage		V_{DD} = 1.8 V +/- 8%, V_{DDA} = 1.65 V to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP48		LQFP64		LQFP100	

1. In 128K and 256K Flash STM32F313xx devices the SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

Figure 1. STM32F313xx block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F313xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagrams of the STM32F313xx family devices.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4F processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU)

With its embedded ARM core, the STM32F313xx devices are compatible with all ARM development tools and software.

3.3 Embedded Flash memory

All STM32F313xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Embedded SRAM

STM32F313xx devices feature up to 48 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz (when running code from CCM, core coupled memory).

- 8 Kbytes of SRAM mapped on the instruction bus (Core Coupled Memory (CCM)), used to execute critical routines or to access data (parity check on all of CCM RAM).
- 40 Kbytes of SRAM mapped on the data bus (parity check on first 16 Kbytes of SRAM)

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 or USART2.

3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} =1.8 V+/- 8% : external power supply for I/Os and core. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the DACs and operational amplifiers are used). The V_{DDA} voltage

level must be always greater or equal to the V_{DD} voltage level and must be provided first.

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.7.2 Power supply supervision

The device power on reset is controlled through the external NPOR pin. The device remains in reset state when NPOR pin is held low.

To guarantee a proper power-on reset, the NPOR pin must be held low until V_{DD} is stable. When V_{DD} is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance. NPOR pin has an internal pull up.
- or forcing the pin to high level by connecting it to V_{DDA}.

3.7.3 Low-power modes

The STM32F313xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

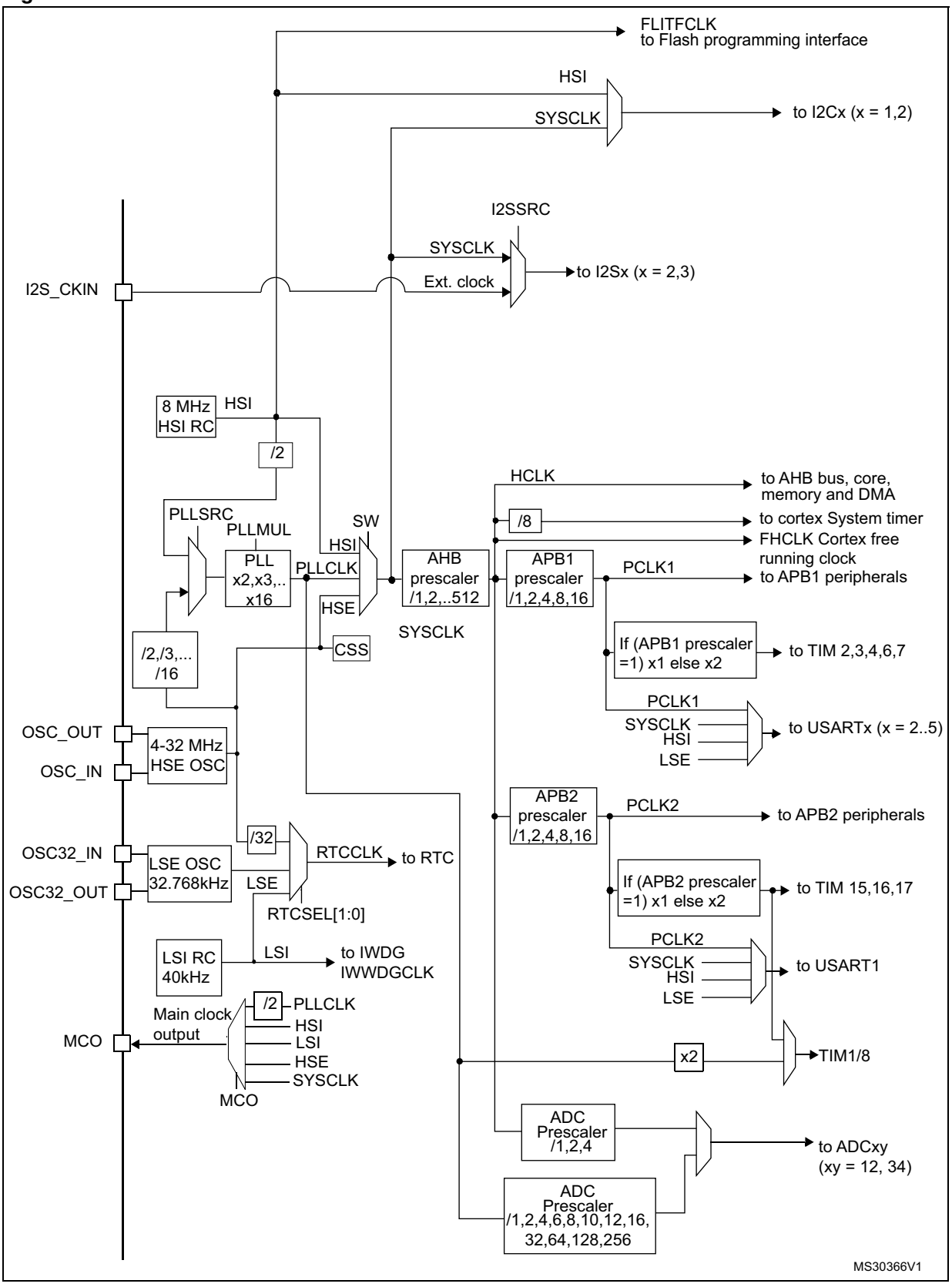
Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Figure 2. Clock tree



3.9 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.10 DMA (direct memory access)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F313xx devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.12 Fast ADC (analog-to-digital converter)

Up to four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F313xx family devices. The ADCs have up to 39 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, $V_{BAT/2}$ connected to ADC1 channel 17, Voltage reference V_{REFINT} connected to the 4 ADCs channel 18, VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 on all devices and TIM8 on STM32F313xx devices) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN18 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Temperature sensor calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12.4 OPAMP reference voltage (VOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17.

3.13 DAC (digital-to-analog converter)

Up to two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels on STM32F313xx devices
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability on STM32F313xx devices
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions on STM32F313xx devices
- DMA capability (for each channel on STM32F313xx devices)
- External triggers for conversion

3.14 Operational amplifier

The STM32F313xx embeds up to four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8 MHz GBP
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.15 Fast comparators

The STM32F313xx devices embed seven fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 27: Embedded internal reference voltage on page 58* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined per pair into a window comparator

3.16 Timers and watchdogs

The STM32F313xx includes up to two advanced control timers, up to 6 general-purpose timers, two basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
Advanced	TIM1, TIM8 (on STM32F313xx devices only)	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7 (on STM32F313xx devices only)	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.16.1 Advanced timers (TIM1, TIM8)

The advanced-control timers (TIM1 on all devices and TIM8 on STM32F313xx devices) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.16.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.16.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F313xx (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.16.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

3.16.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.16.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.17 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.18 I^2C bus

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in I2C1 and I2C2.

Table 7. STM32F31x I^2C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F313xx devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

3.20 Universal asynchronous receiver transmitter (UART)

The STM32F313xx devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features available in all U(S)ARTs interfaces

Table 8. USART features

USART modes/features(1)	USART1	USART2	USART3	USART4	USART5
Hardware flow control for modem	X	X	X		
Continuous communication using DMA	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X		
Smartcard mode	X	X	X		
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X
LIN mode	X	X	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X
Modbus communication	X	X	X	X	X
Auto baud rate detection	X	X	X		
Driver Enable	X	X	X		

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2 and SPI3

Table 9. STM32F31x SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode		X	X
TI mode	X	X	X

1. X = supported.

3.22 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

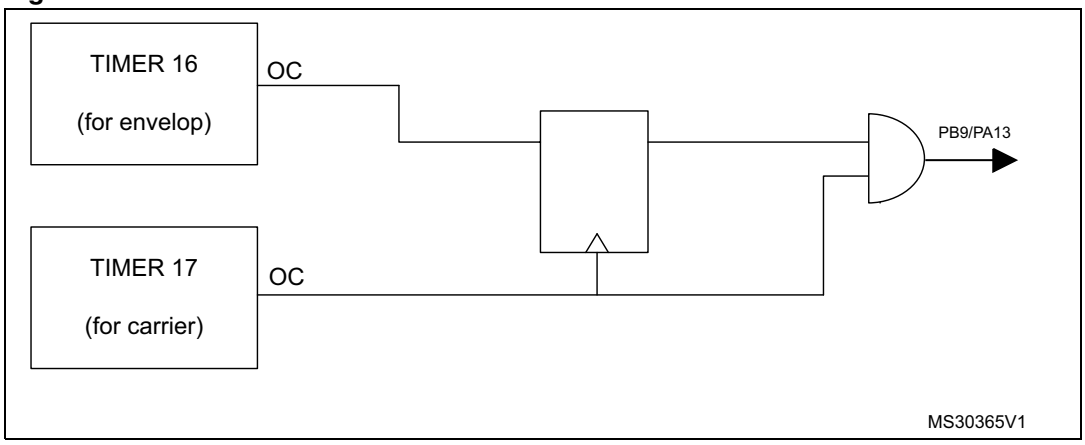
3.23 Infrared Transmitter

The STM32F313xx devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.24 Touch sensing controller (TSC)

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...).The capacitive

variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. The STM32F313xx devices offer up to 23 capacitive sensing channels distributed over 8 analog I/O groups.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F31x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
4	TSC_G4_IO1	PA9		TSC_G7_IO4	PE5
	TSC_G4_IO2	PA10	8	TSC_G8_IO1	PD12
	TSC_G4_IO3	PA13		TSC_G8_IO2	PD13
	TSC_G4_IO4	PA14		TSC_G8_IO3	PD14
				TSC_G8_IO4	PD15

Table 11. No. of capacitive sensing channels available on STM32F313xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F31xVx	STM32F31xRx	STM32F31xCx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	23	17	16

3.25 Development support

3.25.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.25.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F313xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pinouts and pin description

Figure 4. STM32F313xx LQFP48 pinout

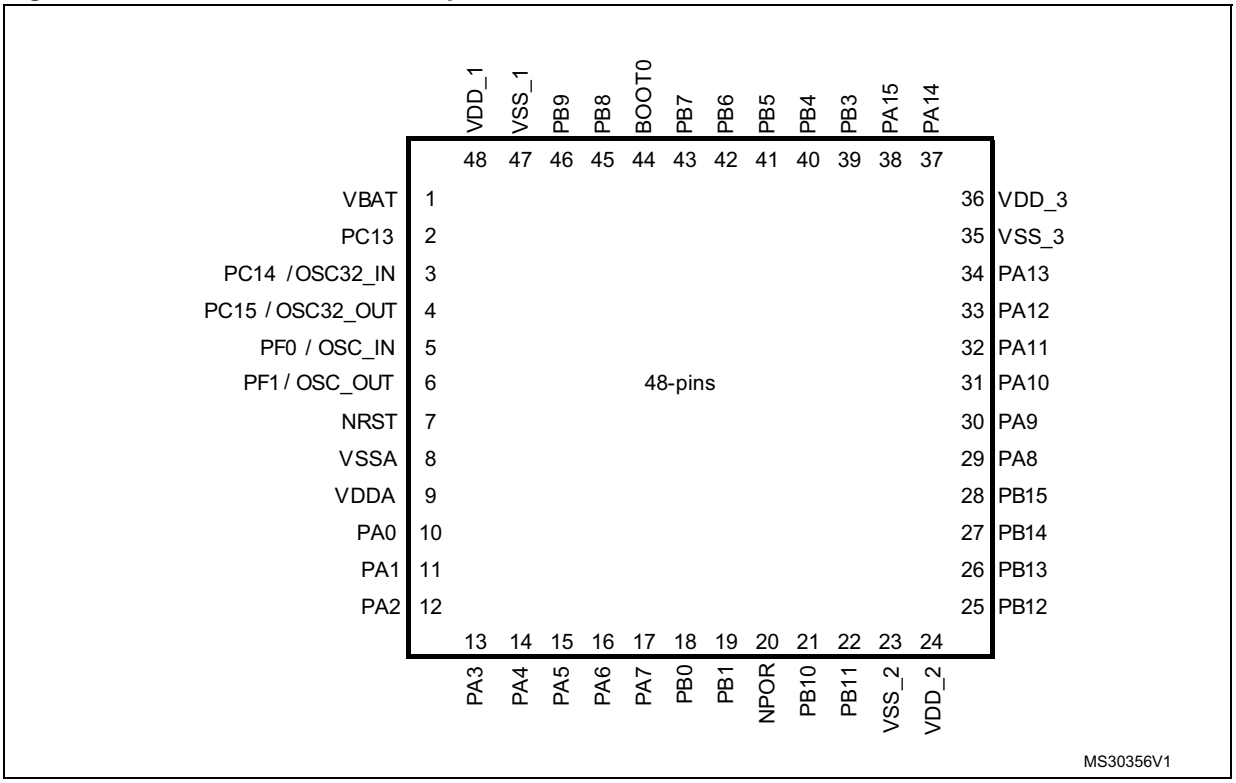


Figure 5. STM32F313xx LQFP64 pinout

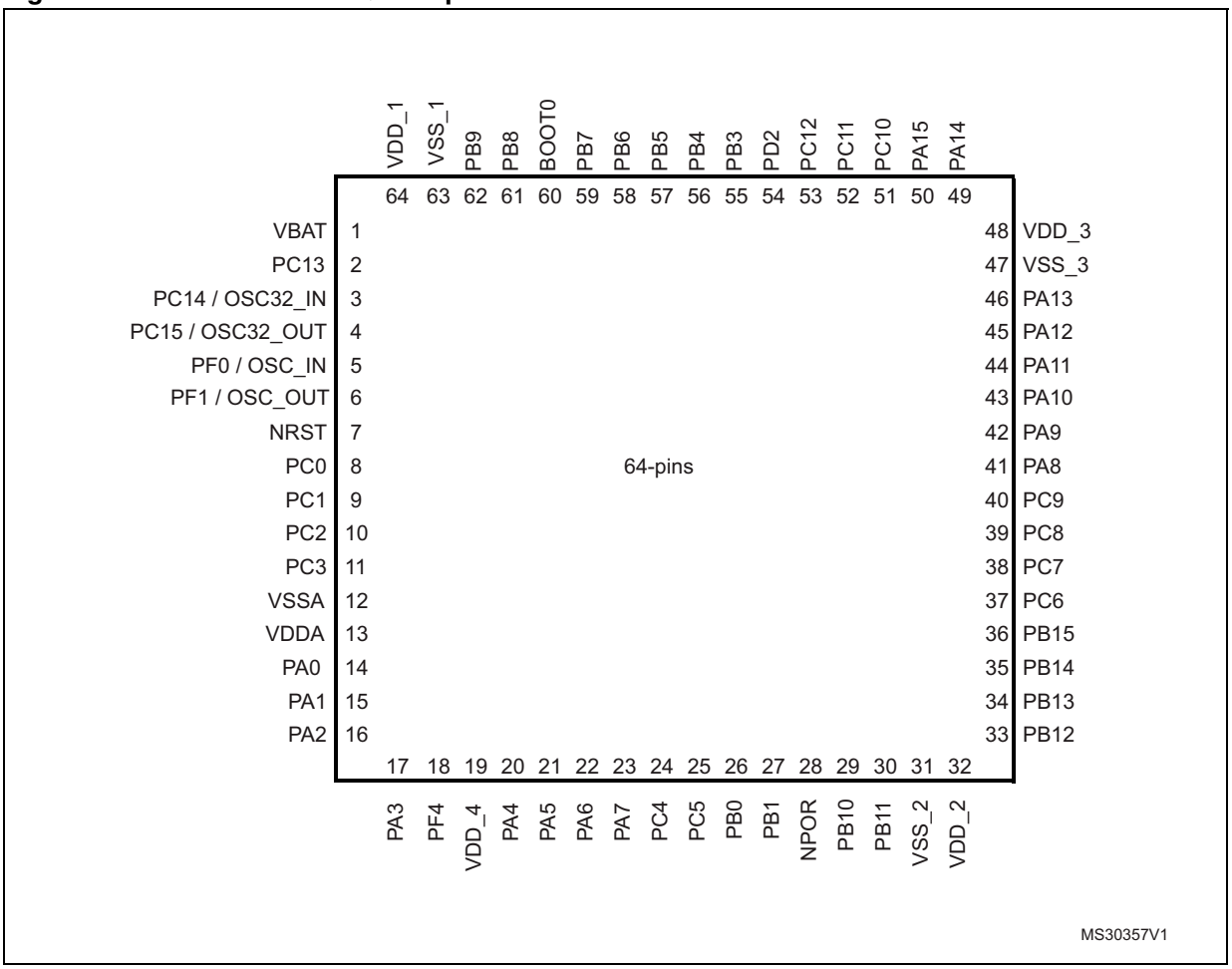


Figure 6. STM32F313xx LQFP100 pinout

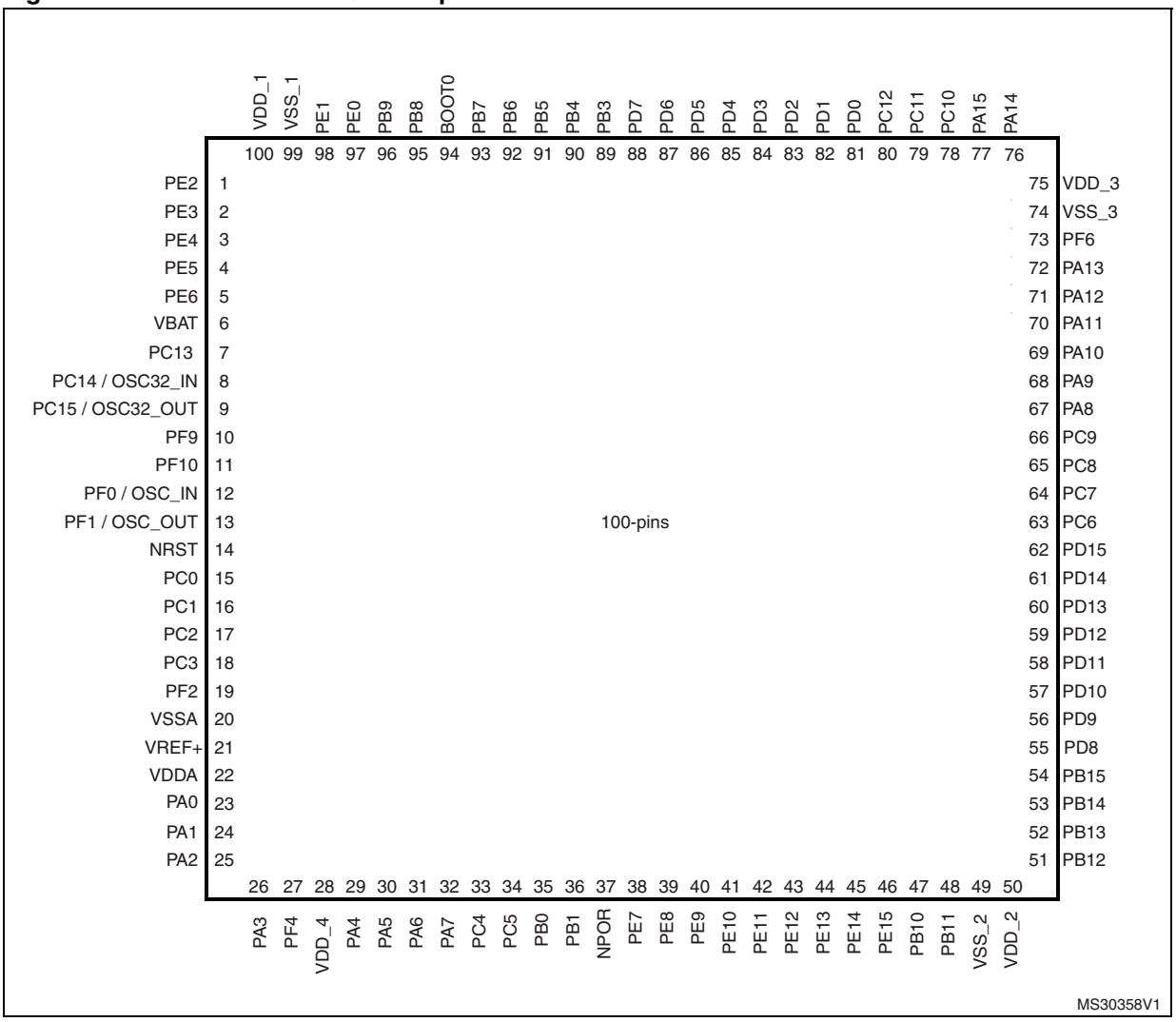


Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F313xx pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
1			PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1	
2			PE3	I/O	FT	(2)(1)	TRACED0, TIM3_CH2, TSC_G7_IO2	
3			PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3	
4			PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4	
5			PE6	I/O	FT	(1)	TRACED3	WKUP3, RTC_TAMP3
6	1	1	V_{BAT}	S			Backup power supply	
7	2	2	PC13	I/O	TC		TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
8	3	3	PC14 - OSC32_IN (PC14)	I/O	TC			OSC32_IN
9	4	4	PC15- OSC32_OUT (PC15)	I/O	TC			OSC32_OUT
10			PF9	I/O	FT	(1)	TIM15_CH1 SPI2_SCK	
11			PF10	I/O	FT	(1)	TIM15_CH2 SPI2_SCK	
12	5	5	PF0- OSC_IN (PF0)	I/O	FTf		TIM1_CH3N, I2C2_SDA	OSC_IN
13	6	6	PF1- OSC_OUT (PF1)	I/O	FTf		I2C2_SCL	OSC_OUT
14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
15	8		PC0	I/O	TTa	(1)		ADC12_IN6, COMP7_INM(3)
16	9		PC1	I/O	TTa	(1)		ADC12_IN7, COMP7_INP(3)
17	10		PC2	I/O	TTa	(1)	COMP7_OUT(3)	ADC12_IN8
18	11		PC3	I/O	TTa	(1)	TIM1_BKIN2	ADC12_IN9
19			PF2	I/O	TTa	(1)		ADC12_IN10
20	12	8	V_{SSA} / V_{REF-}	S			Analog ground/Negative reference voltage	
21			V_{REF+}	S		(1)	Positive reference voltage	
22			V_{DDA}	S		(1)	Analog power supply	
	13	9	V_{DDA}, V_{REF+}	S			Analog power supply/Positive reference voltage	

Table 13. STM32F313xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
23	14	10	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TIM8_BKIN(3), TIM8_ETR(3), TSC_G1_IO1, COMP1_OUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1, COMP7_INP(3)
24	15	11	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TSC_G1_IO2TIM15_CH1N(3)	ADC1_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP(3)
25	16	12	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT	ADC1_IN3, COMP2_INM, AOP1_OUT
26	17	13	PA3	I/O	TTa		USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4,	ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM
27	18		PF4	I/O	TTa	(1)	COMP1_OUT	ADC1_IN5
28	19		V_{DD_4}	S		(1)		
29	20	14	PA4	I/O	TTa		SPI1_NSS, SPI3_NSS/I2S3_WS(3), USART2_CK, TSC_G2_IO1, TIM3_CH2	ADC2_IN1, DAC1_OUT1, OPAMP4_VINP, COMP1_INM4, COMP2_INM4, COMP3_INM4, COMP4_INM4, COMP5_INM4, COMP6_INM4, COMP7_INM4
30	21	15	PA5	I/O	TTa		SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2	ADC2_IN2, DAC1_OUT2(3), OPAMP1_VINP, OPAMP2_VINM, OPAMP3_VINP, COMP1_INM5, COMP2_INM5, COMP3_INM5, COMP4_INM5, COMP5_INM5, COMP6_INM5, COMP7_INM5
31	22	16	PA6	I/O	TTa		SPI1_MISO, TIM3_CH1, TIM8_BKIN(3), TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3	ADC2_IN3, AOP2_OUT
32	23	17	PA7	I/O	TTa		SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, TIM8_CH1N, TSC_G2,_IO4, COMP2_OUT	ADC2_IN4, COMP2_IN, OPAMP2_VINP, OPAMP1_VINP
33	24		PC4	I/O	TTa	(1)	USART1_TX	ADC2_IN5

Table 13. STM32F313xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
34	25		PC5	I/O	TTa	(1)	USART1_RX, TSC_G3_IO1	ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM
35	26	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TIM8_CH2N(3), TSC_G3_IO2	ADC3_IN12(3), COMP4_INP, OPAMP3_VINP(3), OPAMP2_VINP
36	27	19	PB1	I/O	TTa		TIM3_CH4, TIM1_CH3N, TIM8_CH3N(3), COMP4_OUT, TSC_G3_IO3	ADC3_IN1(3), AOP3_OUT
37	28	20	NPOR					
38			PE7	I/O	TTa	(1)	TIM1_ETR	ADC3_IN13(3), COMP4_INP
39			PE8	I/O	TTa	(1)	TIM1_CH1N	COMP4_INM,ADC34_IN6(3)
40			PE9	I/O	TTa	(1)	TIM1_CH1	ADC3_IN2(3)
41			PE10	I/O	TTa	(1)	TIM1_CH2N	ADC3_IN14(3)
42			PE11	I/O	TTa	(1)	TIM1_CH2	ADC3_IN15(3)
43			PE12	I/O	TTa	(1)	TIM1_CH3N	ADC3_IN16(3)
44			PE13	I/O	TTa	(1)	TIM1_CH3	ADC3_IN3(3)
45			PE14	I/O	TTa	(1)	TIM1_CH4, TIM1_BKIN2	ADC4_IN1(3)
46			PE15	I/O	TTa	(1)	USART3_RX, TIM1_BKIN	ADC4_IN2(3)
47	29	21	PB10	I/O	TTa		USART3_TX, TIM2_CH3, TSC_SYNC	COMP5_INM(3), OPAMP4_VINM(3), OPAMP3_VINM(3)
48	30	22	PB11	I/O	TTa		USART3_RX, TIM2_CH4, TSC_G6_IO1	COMP6_INP, OPAMP4_VINP(3)
49	31	23	VSS_2	S			Digital ground	
50	32	24	VDD_2	S			Digital power supply	
51	33	25	PB12	I/O	TTa		SPI2_NSS/I2S2_WS(3), I2C2_SMBA, USART3_CK, TIM1_BKIN, TSC_G6_IO2	ADC4_IN3(3), COMP3_INM, AOP4_OUT,
52	34	26	PB13	I/O	TTa		SPI2_SCK/I2S2_CK(3), USART3_CTS, TIM1_CH1N, TSC_G6_IO3	ADC3_IN5(3), COMP5_INP(3), OPAMP4_VINP(3), OPAMP3_VINP(3)
53	35	27	PB14	I/O	TTa		SPI2_MISO/I2S2ext_SD(3), USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	COMP3_INP(3), ADC4_IN4(3), OPAMP2_VINP
54	36	28	PB15	I/O	TTa		SPI2_MOSI/I2S2_SD(3), TIM1_CH3N, TIM15_CH1N, TIM15_CH2	ADC4_IN5(3), RTC_REFIN, COMP6_INM
55			PD8	I/O	TTa	(1)	USART3_TX	ADC4_IN12(3), OPAMP4_VINM(3)

Table 13. STM32F313xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
56			PD9	I/O	TTa	(1)	USART3_RX	ADC4_IN13(3)
57			PD10	I/O	TTa	(1)	USART3_CK	ADC34_IN7(3),COMP6_INM
58			PD11	I/O	TTa	(1)	USART3_CTS	ADC34_IN8(3),COMP6_INP, OPAMP4_VINP(3)
59			PD12	I/O	TTa	(1)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	ADC34_IN9(3), COMP5_INP(3)
60			PD13	I/O	TTa	(1)	TIM4_CH2, TSC_G8_IO2	ADC34_IN10(3), COMP5_INM(3)
61			PD14	I/O	TTa	(1)	TIM4_CH3, TSC_G8_IO3	COMP3_INP, ADC34_IN11(3), OPAMP2_VINP
62			PD15	I/O	TTa	(1)	SPI2_NSS, TIM4_CH4, TSC_G8_IO4	COMP3_INM
63	37		PC6	I/O	FT	(1)	I2S2_MCK(3), COMP6_OUT(3), TM8_CH1, TIM3_CH1	
64	38		PC7	I/O	FT	(1)	I2S3_MCK(3), TIM8_CH2(3), TIM3_CH2, COMP5_OUT(3)	
65	39		PC8	I/O	FT	(1)	TIM8_CH3(3), TIM3_CH3, COMP3_OUT	
66	40		PC9	I/O	FT	(1)	TIM8_CH4(3), TIM8_BKIN2(3), TIM3_CH4, I2S_CKIN(3)	
67	41	29	PA8	I/O	FT		I2C2_SMBA, I2S2_MCK(3), USART1_CK, TIM1_CH1, TIM4_ETR, MCO(3), COMP3_OUT(3)	
68	42	30	PA9	I/O	FTf		I2C2_SCL, I2S3_MCK(3), USART1_TX, TIM1_CH2, TIM2_CH3, TIM15_BKIN, TSC_G4_IO1, COMP5_OUT(3)	
69	43	31	PA10	I/O	FTf		I2C2_SDA, USART1_RX, TIM1_CH3, TIM2_CH4, TIM8_BKIN(3), TIM17_BKIN, TSC_G4_IO2, COMP6_OUT	
70	44	32	PA11	I/O	FT		USART1_CTS, CAN_RX, TIM1_CH1N, TIM1_CH4, TIM1_BKIN2, TIM4_CH1, COMP1_OUT	
71	45	33	PA12	I/O	FT		USART1_RTS, CAN_TX, TIM1_CH2N, TIM1_ETR, TIM4_CH2, TIM16_CH1, COMP2_OUT	
72	46	34	PA13	I/O	FT		USART3_CTS, TIM4_CH3, TIM16_CH1N, TSC_G4_IO3, IR_OUT, SWDAT-JTMS	

Table 13. STM32F313xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
73			PF6	I/O	FTf	(1)	I2C2_SCL, USART3_RTS, TIM4_CH4	
74	47	35	VSS_3	S			Ground	
75	48	36	VDD_3	S			Digital power supply	
76	49	37	PA14	I/O	FTf		I2C1_SDA, USART2_TX, TIM8_CH2, TIM1_BKIN, TSC_G4_IO4, SWCLK-JTCK	
77	50	38	PA15	I/O	FTf		I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, JTDI, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, TIM8_CH1	
78	51		PC10	I/O	FT	(1)	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, TIM8_CH1N	
79	52		PC11	I/O	FT	(1)	SPI3_MISO/I2S3ext_SD(3), USART3_RX, UART4_RX, TIM8_CH2N(3)	
80	53		PC12	I/O	FT	(1)	SPI3_MOSI/I2S3_SD(3), USART3_CK, UART5_TX, TIM8_CH3N(3)	
81			PD0	I/O	FT	(1)	CAN_RX	
82			PD1	I/O	FT	(1)	CAN_TX, TIM8_CH4, TIM8_BKIN2(3)	
83	54		PD2	I/O	FT	(1)	UART5_RX, TIM3_ETR, TIM8_BKIN(3)	
84			PD3	I/O	FT	(1)	USART2_CTS, TIM2_CH1_ETR	
85			PD4	I/O	FT	(1)	USART2_RTS, TIM2_CH2	
86			PD5	I/O	FT	(1)	USART2_TX	
87			PD6	I/O	FT	(1)	USART2_RX, TIM2_CH4	
88			PD7	I/O	FT	(1)	USART2_CK, TIM2_CH3	
89	55	39	PB3	I/O	FT		SPI3_SCK/I2S3_CK(3), SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM8_CH1N(3), TSC_G5_IO1, JTDO-TRACESWO	
90	56	40	PB4	I/O	FT		SPI3_MISO/I2S3ext_SD(3), SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N(3), TSC_G5_IO2, NJTRST	

Table 13. STM32F313xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
91	57	41	PB5	I/O	FT		SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N(3), TIM17_CH1	
92	58	42	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TIM8_CH1(3), TSC_G5_IO3, TIM8_ETR, TIM8_BKIN2(3)	
93	59	43	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM3_CH4, TIM4_CH2, TIM17_CH1N, TIM8_BKIN, TSC_G5_IO4	
94	60	44	BOOT0	I	B		Boot memory selection	
95	61	45	PB8	I/O	FTf		I2C1_SCL, CAN_RX, TIM16_CH1, TIM4_CH3, TIM8_CH2(3), TIM1_BKIN, TSC_SYNC, COMP1_OUT	
96	62	46	PB9	I/O	FTf		I2C1_SDA, CAN_TX, TIM17_CH1, TIM4_CH4, TIM8_CH3(3), IR_OUT, COMP2_OUT	
97			PE0	I/O	FT	(1)	USART1_TX, TIM4_ETR, TIM16_CH1	
98			PE1	I/O	FT	(1)	USART1_RX, TIM17_CH1	
99	63	47	VSS_1	S			Ground	
100	64	48	VDD_1	S			Digital power supply	

1. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. Function availability depends on the chosen device.
3. On STM32F313xx devices only.

Table 14. Alternate functions for port A

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
7	PA0		TIM2_CH1_ETR		TSC_G1_IO1				USART2_CTS	COMP1_OUT	TIM8_BKIN	TM8_ETR					EVENTOUT
5	PA1		TIM2_CH2		TSC_G1_IO2				USART2_RTS		TIM15_CH1N						EVENTOUT
6	PA2		TIM2_CH3		TSC_G1_IO3				USART2_TX	COMP2_OUT	TIM15_CH1						EVENTOUT
5	PA3		TIM2_CH4		TSC_G1_IO4				USART2_RX		TIM15_CH2						EVENTOUT
6	PA4			TIM3_CH2	TSC_G2_IO1		SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK								EVENTOUT
4	PA5		TIM2_CH1_ETR		TSC_G2_IO2		SPI1_SCK										EVENTOUT
8	PA6		TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN		COMP1_OUT							EVENTOUT
8	PA7		TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N		COMP2_OUT							EVENTOUT
8	PA8	MCO				I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK	COMP3_OUT		TIM4_ETR					EVENTOUT
9	PA9				TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3					EVENTOUT
9	PA10		TIM17_BKIN		TSC_G4_IO2	I2C2_SDA		TIM1_CH3	USART1_RX	COMP6_OUT		TIM2_CH4	TIM8_BKIN				EVENTOUT
9	PA11							TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2			EVENTOUT

Table 14. Alternate functions for port A

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
9	PA12		TIM16_ CH1					TIM1_ CH2N	USART1 _RTS	COMP2 _OUT	CAN_TX	TIM4_ CH2	TIM1_ ETR				EVENT OUT
7	PA13	JTMS-SWDAT	TIM16_ CH1N		TSC_ G4_IO3		IR-Out		USART3 _CTS			TIM4_ CH3					EVENT OUT
7	PA14	JTCK-SWCLK			TSC_ G4_IO4	I2C1_ SDA	TIM8_ CH2	TIM1_ BKIN	USART2 _TX								EVENT OUT
9	PA15	JTDI	TIM2_ CH1_ ETR	TIM8_ CH1		I2C1_ SCL	SPI1_ NSS	SPI3_ NSS/ I2S3_ WS	USART2 _RX		TIM1_ BKIN						EVENT OUT

Table 15. Alternate functions for port B

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
5	PB0			TIM3_ CH3	TSC_ G3_IO2	TIM8_ CH2N		TIM1_CH2N						EVENT OUT
6	PB1			TIM3_ CH4	TSC_ G3_IO3	TIM8_ CH3N		TIM1_CH3N		COMP4_ OUT				EVENT OUT
10	PB3	JTDO/ TRACE SWO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1	TIM8_ CH1N	SPI1_ SCK	SPI3_SCK /I2S3_CK	USART2_ TX			TIM3_ ETR		EVENT OUT
10	PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2	TIM8_ CH2N	SPI1_ MISO	SPI3_MISO/ I2S3ext_SD	USART2_ RX			TIM17_ BKIN		EVENT OUT
9	PB5		TIM16_ BKIN	TIM3_ CH2	TIM8_ CH3N	I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI/ I2S3_SD	USART2_ CK			TIM17_ CH1		EVENT OUT
9	PB6		TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL	TIM8_CH1	TIM8_ ETR	USART1_ TX			TIM8_ BKIN2		EVENT OUT
8	PB7		TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA	TIM8_ BKIN		USART1_ RX			TIM3_ CH4		EVENT OUT
10	PB8		TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL				COMP1_ OUT	CAN_RX	TIM8_ CH2	TIM1_ BKIN	EVENT OUT
9	PB9		TIM17_ CH1	TIM4_ CH4		I2C1_ SDA		IR-OUT		COMP2_ OUT	CAN_TX	TIM8_ CH3		EVENT OUT
4	PB10		TIM2_ CH3		TSC_ SYNC				USART3_ TX					EVENT OUT
4	PB11		TIM2_ CH4		TSC_ G6_IO1				USART3_ RX					EVENT OUT
6	PB12				TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS/ I2S2_WS	TIM1_ BKIN	USART3_ CK					EVENT OUT
5	PB13				TSC_ G6_IO3		SPI2_SCK/ I2S2_CK	TIM1_ CH1N	USART3_ CTS					EVENT OUT

Table 15. Alternate functions for port B

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
6	PB14		TIM15_ CH1		TSC_ G6_IO4		SPI2_MISO/ I2S2ext_SD	TIM1_ CH2N	USART3_ RTS					EVENT OUT
5	PB15		TIM15_ CH2	TIM15 _CH1N		TIM1_ CH3N	SPI2_MOSI/ I2S2_SD							EVENT OUT

Table 16. Alternate functions for port C

AF n°	Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
1	PC0	EVENTOUT						
1	PC1	EVENTOUT						
2	PC3	EVENTOUT					TIM1_BKIN2	
2	PC4	EVENTOUT						USART1_TX
3	PC5	EVENTOUT		TSC_G3_IO1				USART1_RX
5	PC6	EVENTOUT	TIM3_CH1		TIM8_CH1		I2S2_MCK	COMP6_OUT
5	PC7	EVENTOUT	TIM3_CH2		TIM8_CH2		I2S3_MCK	COMP5_OUT
4	PC8	EVENTOUT	TIM3_CH3		TIM8_CH3			COMP3_OUT
5	PC9	EVENTOUT	TIM3_CH4		TIM8_CH4	I2S_CKIN	TIM8_BKIN2	
5	PC10	EVENTOUT			TIM8_CH1N	UART4_TX	SPI3_SCK/I2S3_CK	USART3_TX
5	PC11	EVENTOUT			TIM8_CH2N	UART4_RX	SPI3_MISO/I2S3ext_SD	USART3_RX
5	PC12	EVENTOUT			TIM8_CH3N	UART5_TX	SPI3_MOSI/I2S3_SD	USART3_CK
	PC13				TIM1_CH1N			
	PC14							
	PC15							

Table 17. Alternate functions for port D

AF n°	Port & Pin Name	AF1	AF2	AF3	AF1	AF5	AF6	AF7
2	PD0	EVENTOUT						CAN_RX
4	PD1	EVENTOUT			TIM8_CH4		TIM8_BKIN2	CAN_TX
3	PD3	EVENTOUT	TIM2_CH1_ETR					USART2_CTS
3	PD4	EVENTOUT	TIM2_CH2					USART2_RTS
2	PD5	EVENTOUT						USART2_TX
3	PD6	EVENTOUT	TIM2_CH4					USART2_RX
3	PD7	EVENTOUT	TIM2_CH3					USART2_CK
2	PD8	EVENTOUT						USART3_TX
2	PD9	EVENTOUT						USART3_RX
2	PD10	EVENTOUT						USART3_CK
2	PD11	EVENTOUT						USART3_CTS
4	PD12	EVENTOUT	TIM4_CH1	TSC_G8_IO1				USART3_RTS
3	PD13	EVENTOUT	TIM4_CH2	TSC_G8_IO2				
3	PD14	EVENTOUT	TIM4_CH3	TSC_G8_IO3				
4	PD15	EVENTOUT	TIM4_CH4	TSC_G8_IO4			SPI2_NSS	

Table 18. Alternate functions for port E

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF6	AF7
4	PE0		EVENTOUT	TIM4_ETR		TIM16_CH1		USART1_TX
3	PE1		EVENTOUT			TIM17_CH1		USART1_RX
4	PE3	TRACED0	EVENTOUT	TIM3_CH2	TSC_G7_IO2			
4	PE4	TRACED1	EVENTOUT	TIM3_CH3	TSC_G7_IO3			
4	PE5	TRACED2	EVENTOUT	TIM3_CH4	TSC_G7_IO4			
2	PE6	TRACED3	EVENTOUT					
2	PE7		EVENTOUT	TIM1_ETR				
2	PE8		EVENTOUT	TIM1_CH1N				
2	PE9		EVENTOUT	TIM1_CH1				
2	PE10		EVENTOUT	TIM1_CH2N				
2	PE11		EVENTOUT	TIM1_CH2				
2	PE12		EVENTOUT	TIM1_CH3N				
2	PE13		EVENTOUT	TIM1_CH3				
3	PE14		EVENTOUT	TIM1_CH4			TIM1_BKIN2	
3	PE15		EVENTOUT	TIM1_BKIN				USART3_RX

Table 19. Alternate functions for port F

AF n°	Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
2	PF0				I2C2_SDA		TIM1_CH3N	
1	PF1				I2C2_SCL			
2	PF4	EVENTOUT	COMP1_OUT					
4	PF6	EVENTOUT	TIM4_CH4		I2C2_SCL			USART3_RTS
3	PF9	EVENTOUT		TIM15_CH1		SPI2_SCK		
3	PF10	EVENTOUT		TIM15_CH2		SPI2_SCK		

5 Memory mapping

Figure 7. STM32F31x memory map

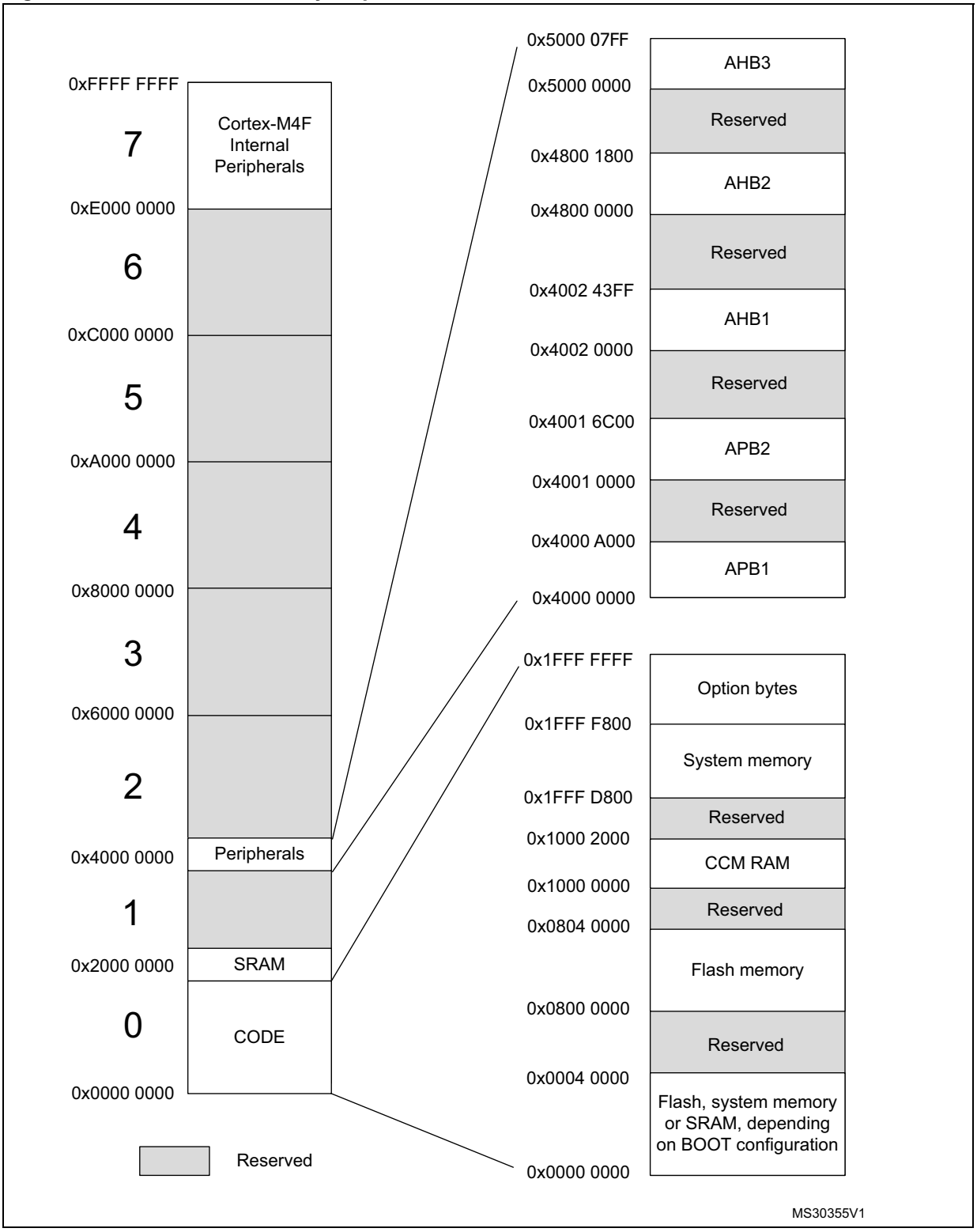


Table 20. STM32F31x memory map and peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0400 - 0x5000 07FF	1 K	ADC3 - ADC4
	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

Table 20. STM32F31x memory map and peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4000 8000 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7FFF	2 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC (dual)
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6C00 - 0x4000 6FFF	1 K	Reserved
	0x4000 6800 - 0x4000 6BFF	1 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 5C00 - 0x4000 63FF	2 K	Reserved
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 8. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline(1)

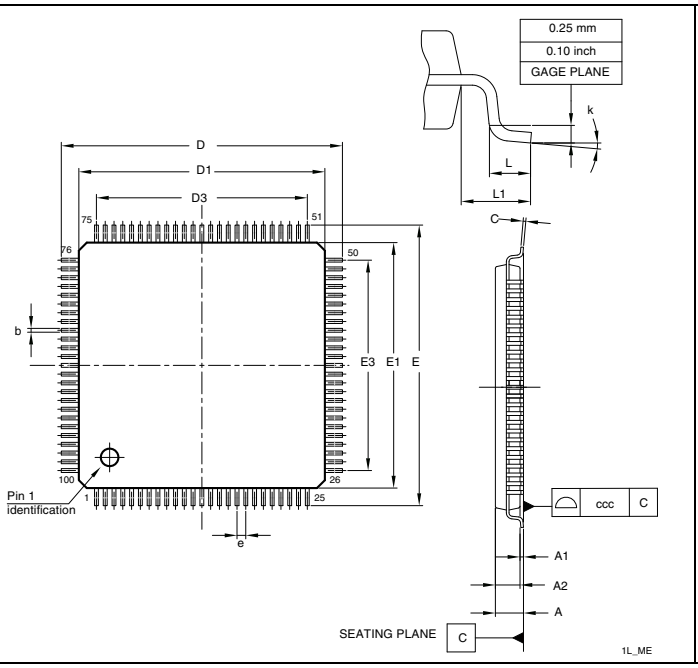
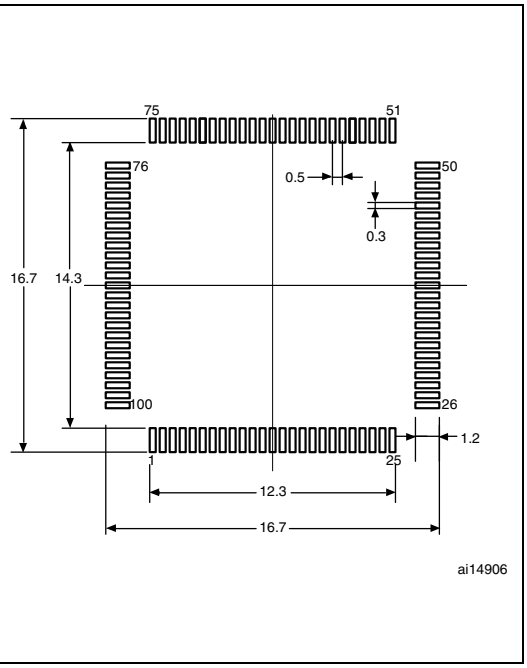


Figure 9. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 21. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3		12.00			0.4724	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0.0°	3.5°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 10. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline(1)

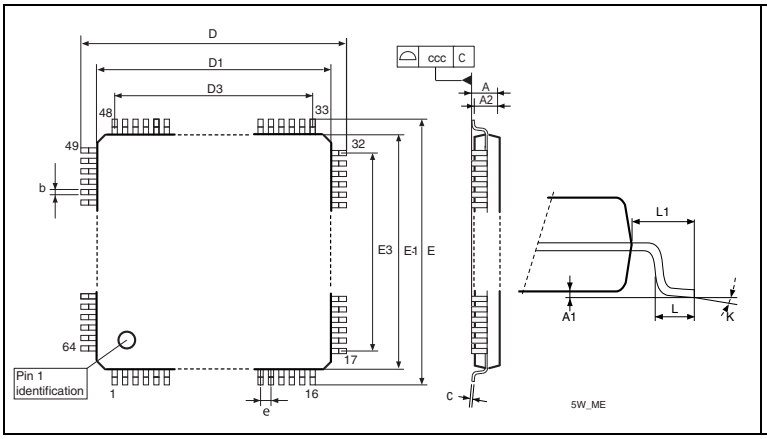
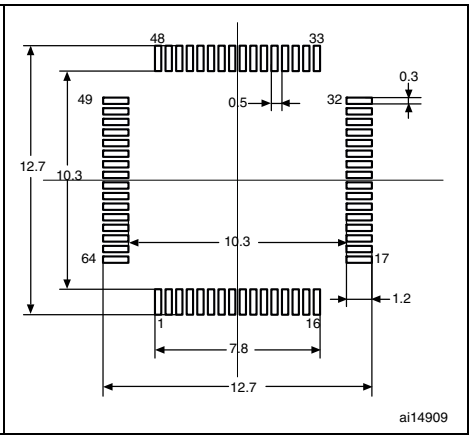


Figure 11. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 22. LQFP64 – 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
Number of pins						
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 12. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline(1)

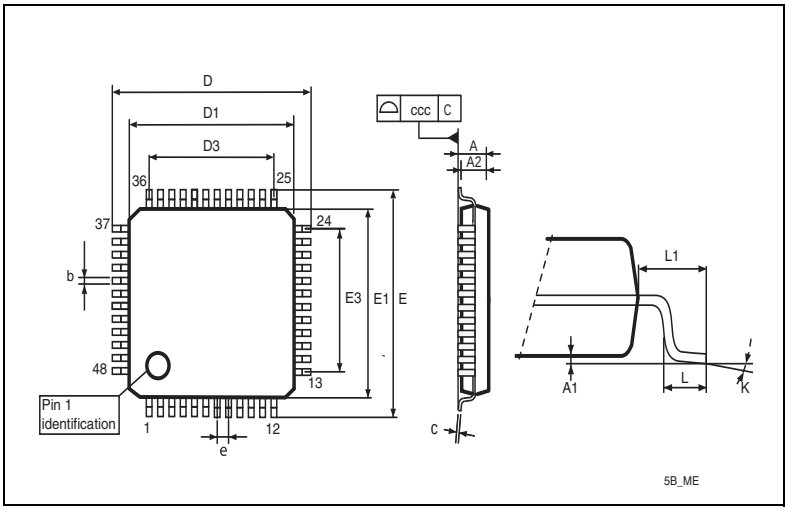
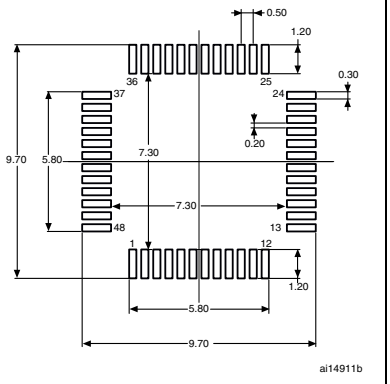


Figure 13. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 23. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 24. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 100 - 14 × 14 mm / 0.5 mm pitch	41	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP 48 - 7 × 7 mm / 0.5 mm pitch	55	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 25: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F313xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 24* T_{Jmax} is calculated as follows:

– For LQFP100, TBD °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 25: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 24* T_{Jmax} is calculated as follows:

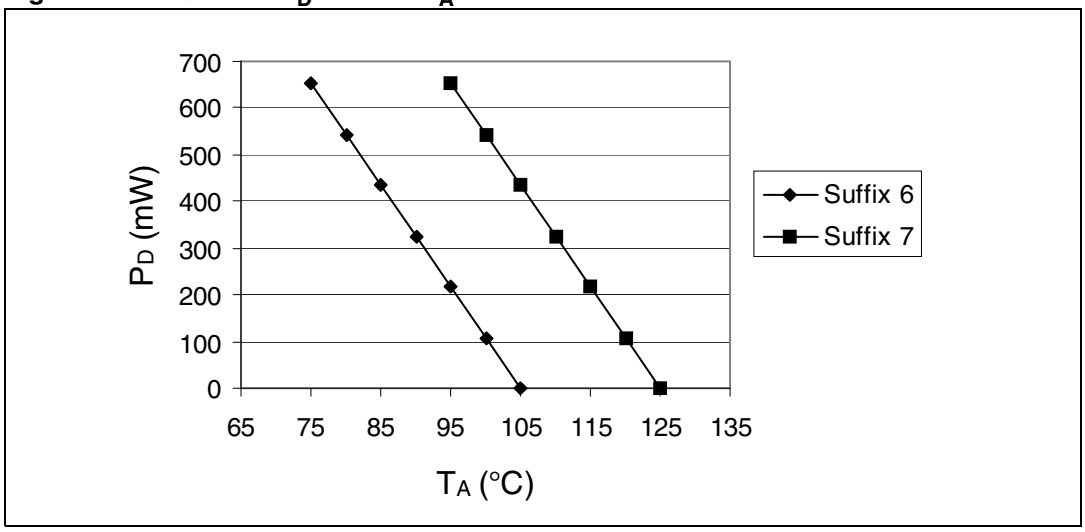
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 25: Ordering information scheme*).

Figure 14. LQFP100 P_D max vs. T_A



7 Part numbering

Table 25. Ordering information scheme

Example: STM32 F 313 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

313 = STM32F313xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory (medium density)
C = 256 Kbytes of Flash memory (high density)

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

8 Revision history

Table 26. Document revision history

Date	Revision	Changes
07-Sep-2012	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com