



STL6N3LLH6

N-channel 30 V, 0.021 Ω typ., 6 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet — preliminary data

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D	P _{TOT}
STL6N3LLH6	30 V	0.025 Ω (V _{GS} =10 V) 0.04 Ω (V _{GS} =4.5 V)	6 A	2.4 W

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

Applications

- Switching application

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

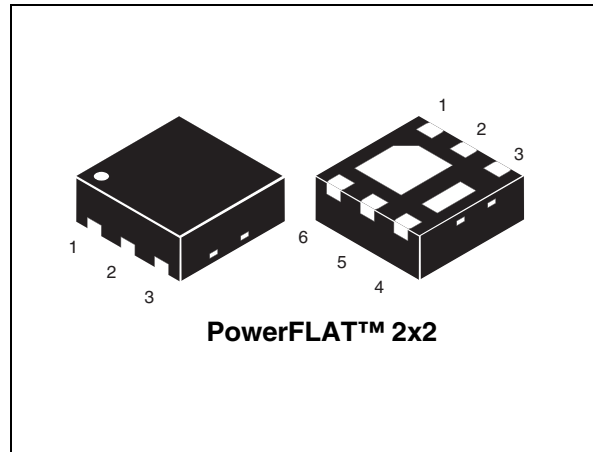


Figure 1. Internal schematic diagram

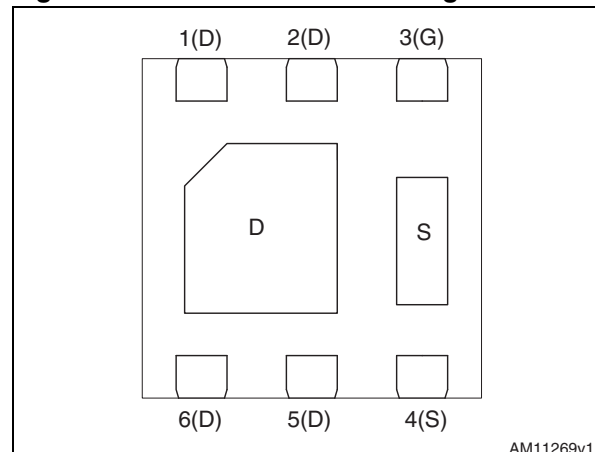


Table 1. Device summary

Order code	Marking	Package	Packaging
STL6N3LLH6	STG1	PowerFLAT™ 2x2	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	6	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	3.75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.4	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	52	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\text{ V}$, $V_{DS} = 30\text{ V}$, $T_J = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 3\text{ A}$		0.021 0.032	0.025 0.04	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 24\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	283	-	pF
C_{oss}	Output capacitance			61		pF
C_{rss}	Reverse transfer capacitance			31		pF
Q_g	Total gate charge	$V_{DD} = 10\text{ V}$, $I_D = 6\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 14)	-	3.6	-	nC
Q_{gs}	Gate-source charge			1.5		nC
Q_{gd}	Gate-drain charge			1.1		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 13)	-	4.8	-	ns
t_r	Rise time			11.2		ns
$t_{d(off)}$	Turn-off delay time			9.4		ns
t_f	Fall time			5.4		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6 \text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 6 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 16 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	10.6		ns
Q_{rr}	Reverse recovery charge			2.8		nC
I_{RRM}	Reverse recovery current			0.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

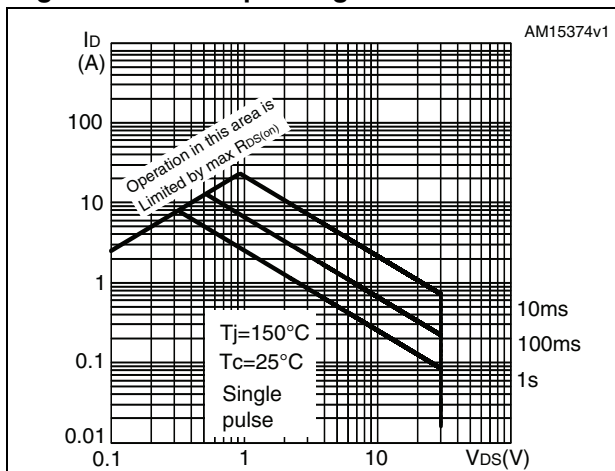


Figure 3. Thermal impedance

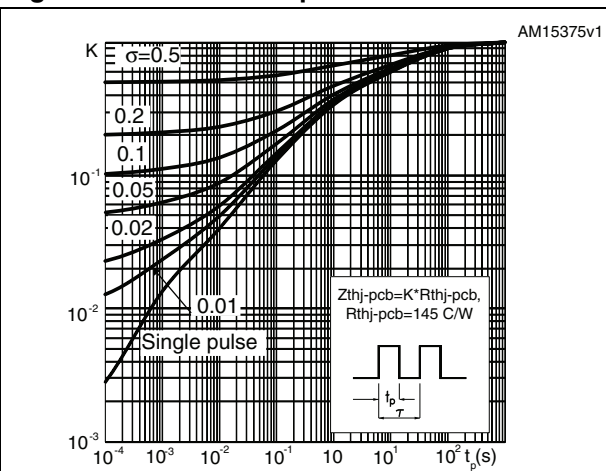


Figure 4. Output characteristics

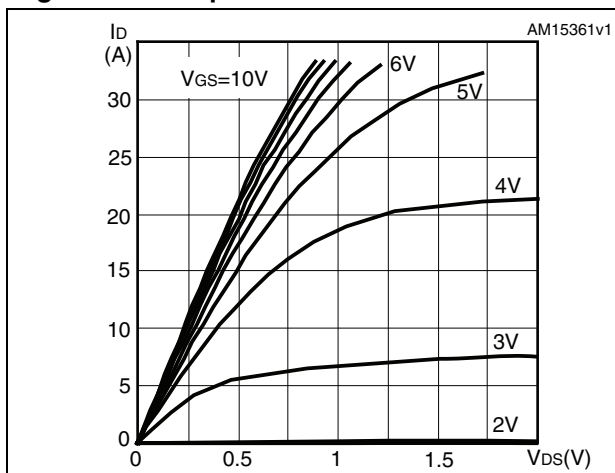


Figure 5. Transfer characteristics

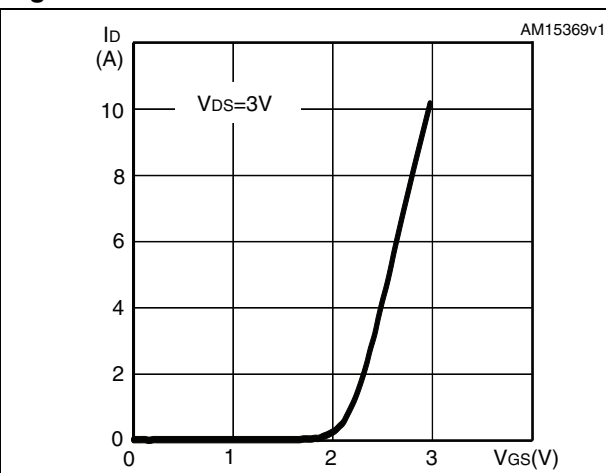


Figure 6. Gate charge vs gate-source voltage

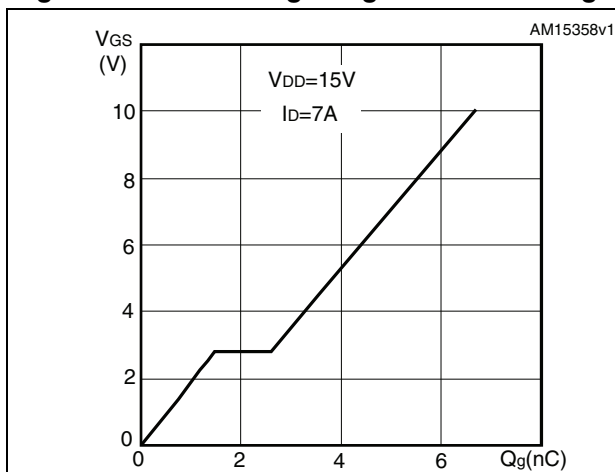


Figure 7. Static drain-source on-resistance

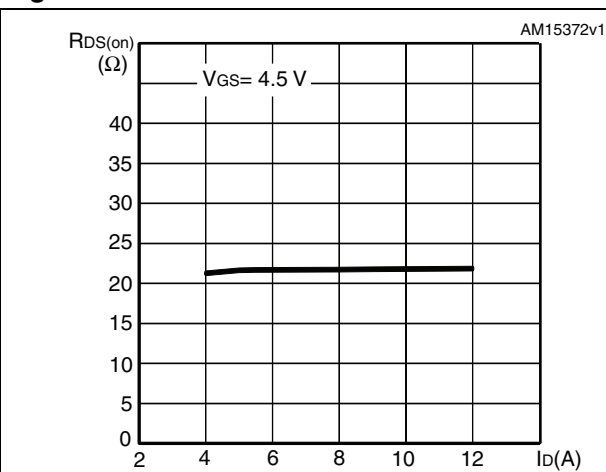


Figure 8. Capacitance variations

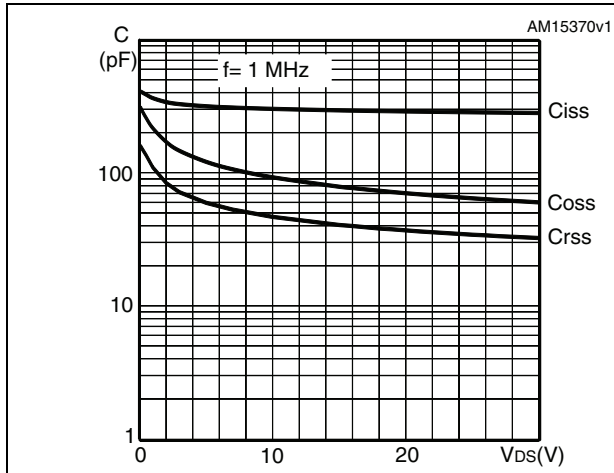


Figure 9. Normalized on-resistance vs temperature

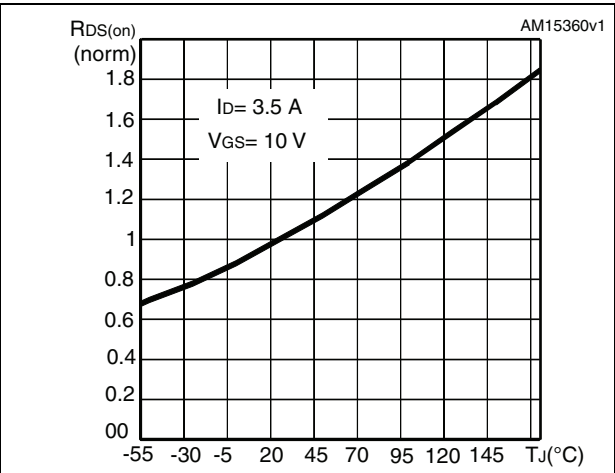


Figure 10. Normalized gate threshold voltage vs temperature

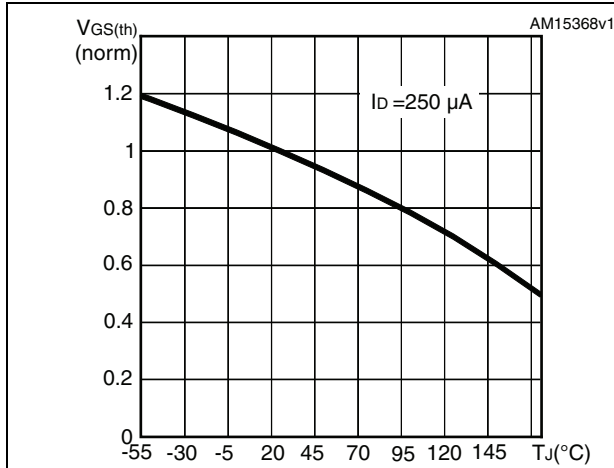


Figure 11. Normalized BVDS vs temperature

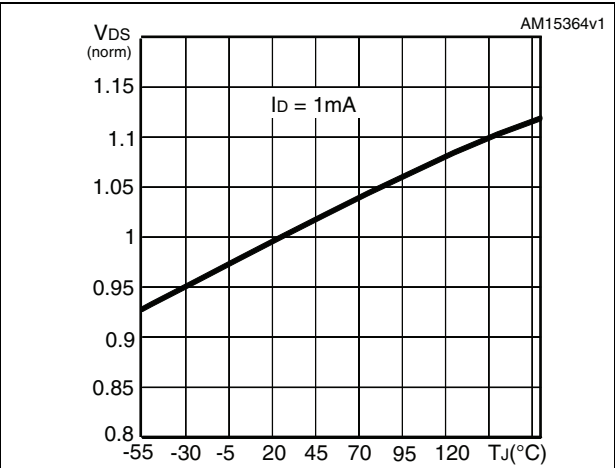
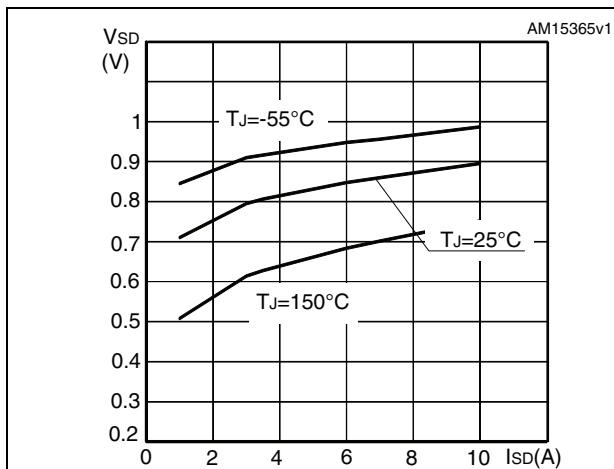


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

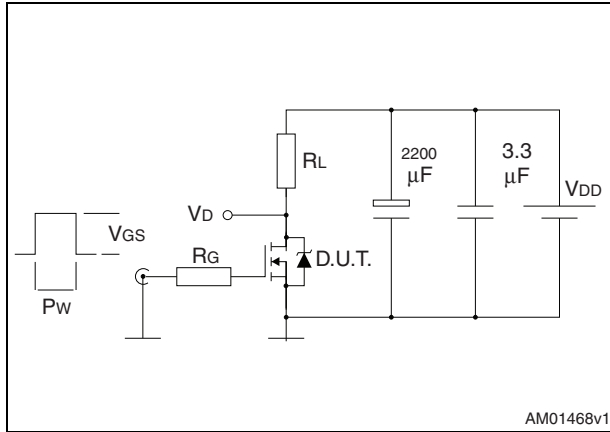


Figure 14. Gate charge test circuit

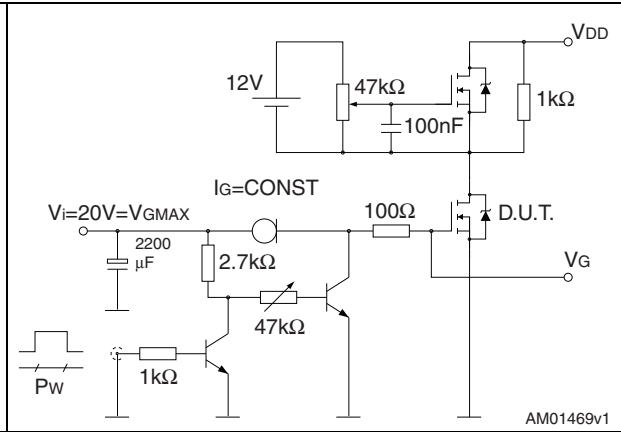


Figure 15. Test circuit for inductive load switching and diode recovery times

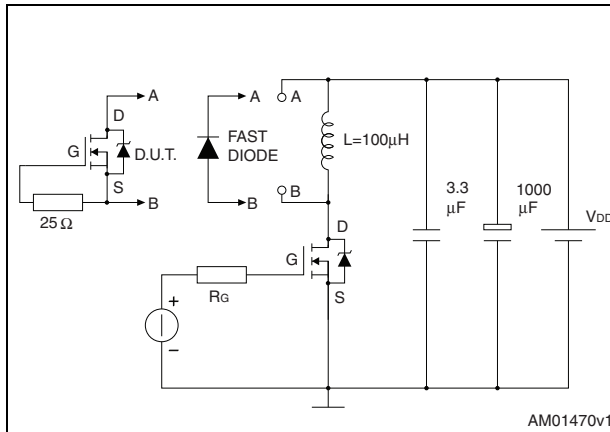


Figure 16. Unclamped inductive load test circuit

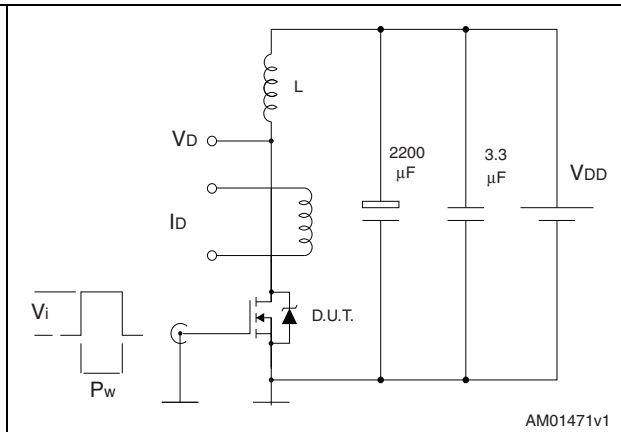


Figure 17. Unclamped inductive waveform

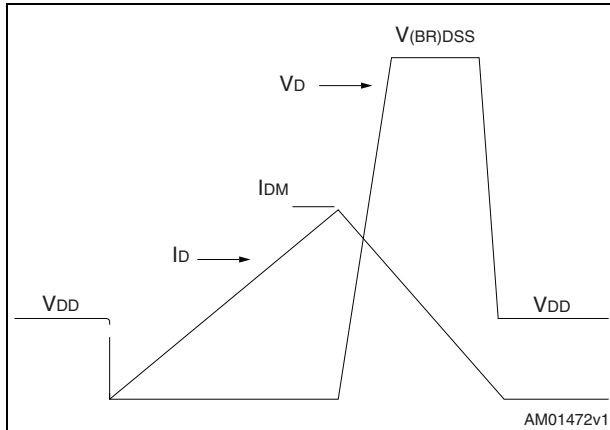
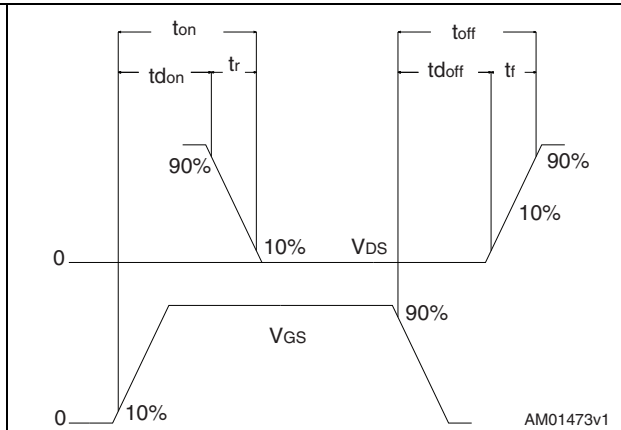


Figure 18. Switching time waveform



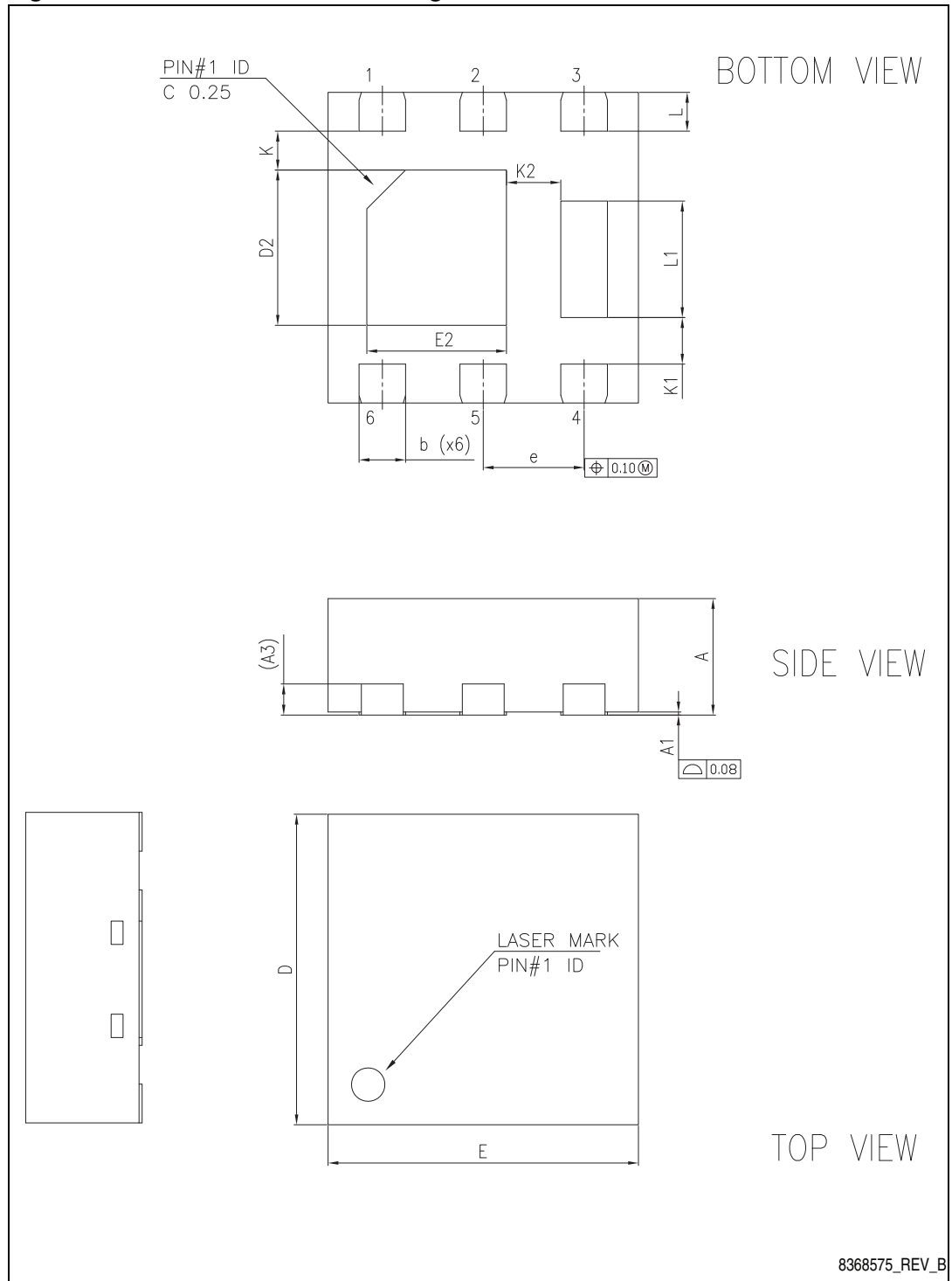
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT™ 2x2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 19. PowerFLAT™ 2 x 2 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-May-2012	1	First release
11-Oct-2012	2	<ul style="list-style-type: none">– Added Section 2.1: Electrical characteristics (curves).– $R_{DS(on)}$ values (typ. and max.) updated– Typical values updated in Table 5, 6 and 7– Minor text changes.

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