USER GUIDE

ATWINC1500-MR210PA Hardware Design Guidelines IEEE 802.11 b/g/n IoT Module

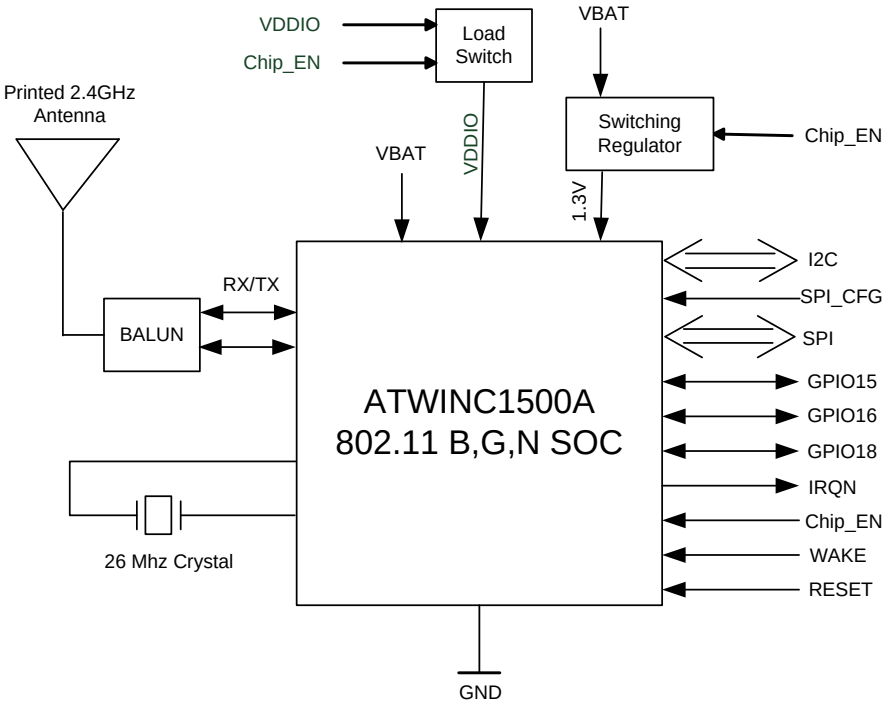
Atmel SmartConnect

Introduction

This document details the hardware design guidelines for a customer to design the Atmel® ATWINC1500-MR210PA module onto their board.

1 Block Diagram

Figure 1-1. Block Diagram of the Module



2 Pinout Information

2.1 Pin Description

Figure 2-1. Pin Assignment

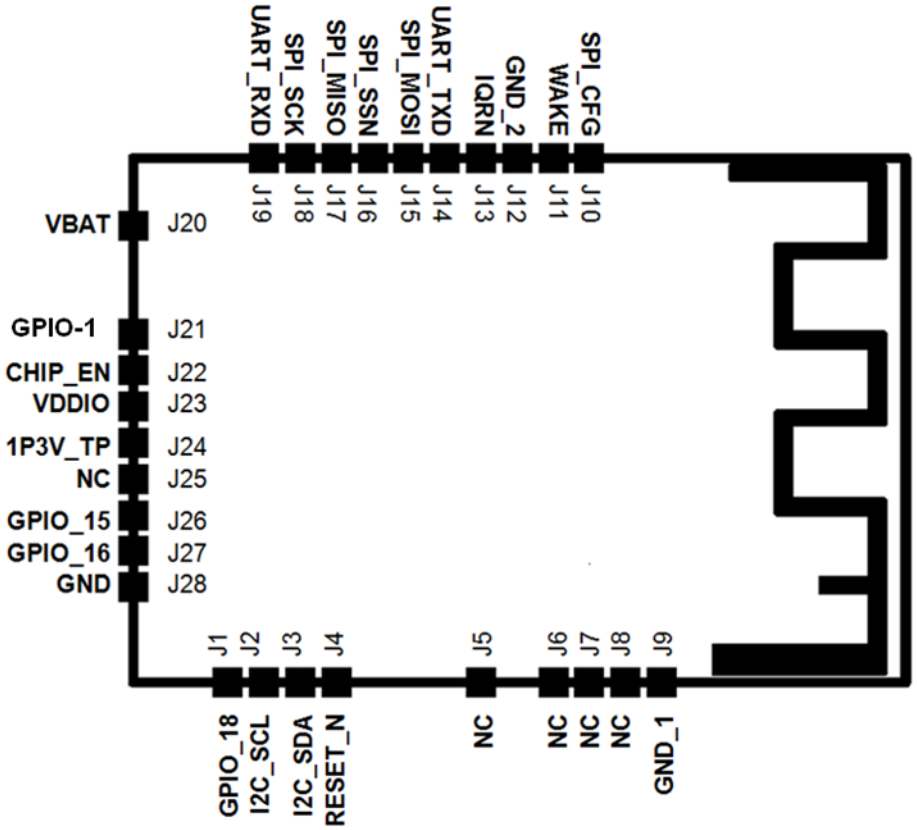


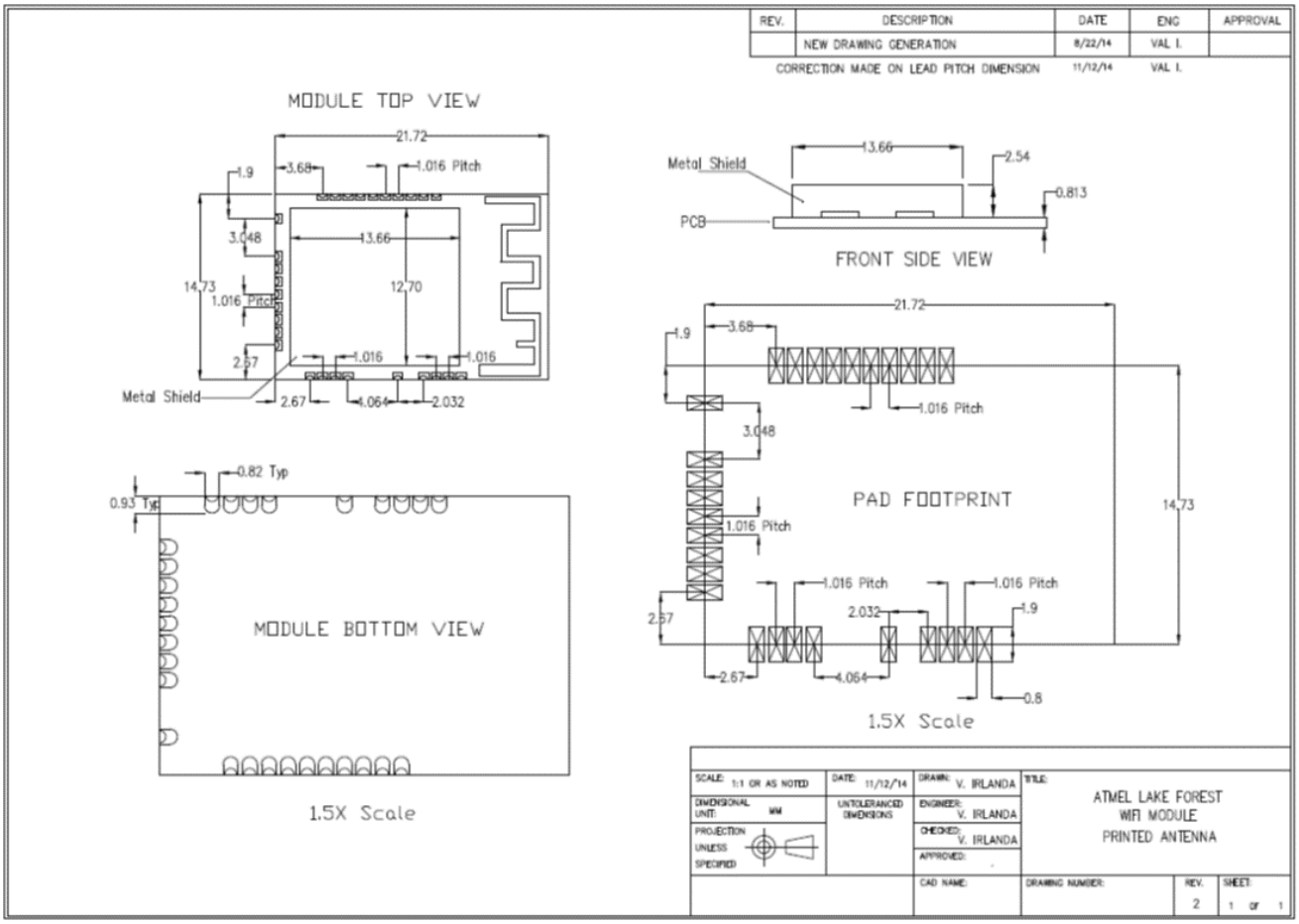
Table 2-1. Pin Description

No.	Name	Type	Description	Programmable Pull-up Resistor
1	GPIO_18	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I^2C Slave Clock. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes
3	I2C_SDA	I/O	I^2C Slave Data. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes
4	RESET_N	I	Active-Low Hard Reset. When asserted to a low level, the module will be placed in a reset state. When asserted to a high level, the module will run normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
5	NC	-	No connect.	
6	NC	-	No connect.	
7	NC	-	No connect.	
8	NC	-	No connect.	

No.	Name	Type	Description	Programmable Pull-up Resistor
9	GND_1	-	GND.	
10	SPI_CFG	I	Tie to VDDIO through a 1MΩ resistor to enable the SPI interface.	No
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	Yes
12	GND_2	-	GND.	
13	IRQN	O	ATWINC1500-MR210PA Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC1500-MR210P.	Yes
15	SPI_RXD	I	SPI MOSI (Master Out Slave In) pin.	Yes
16	SPI_SSN	I	SPI Slave Select. Active low.	Yes
17	SPI_TXD	O	SPI MISO (Master In Slave Out) pin.	Yes
18	SPI_SCK	I	SPI Clock.	Yes
19	UART_RXD	I	UART Receive input to ATWINC1500-MR210P.	Yes
20	VBATT	-	Battery power supply.	
21	GPIO_1	I	General Purpose I/O.	Yes
22	CHIP_EN	I	Module enable. High level enables module, low level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point. Leave unconnected.	
25	NC	-	No connect.	
26	GPIO_15	I/O	General purpose I/O.	Yes
27	GPIO_16	I/O	General purpose I/O.	Yes
28	GND_3	-	GND.	

2.2 Module Outline Drawing

Figure 2-2. Module Drawings – Top and Bottom Views (units = mm)

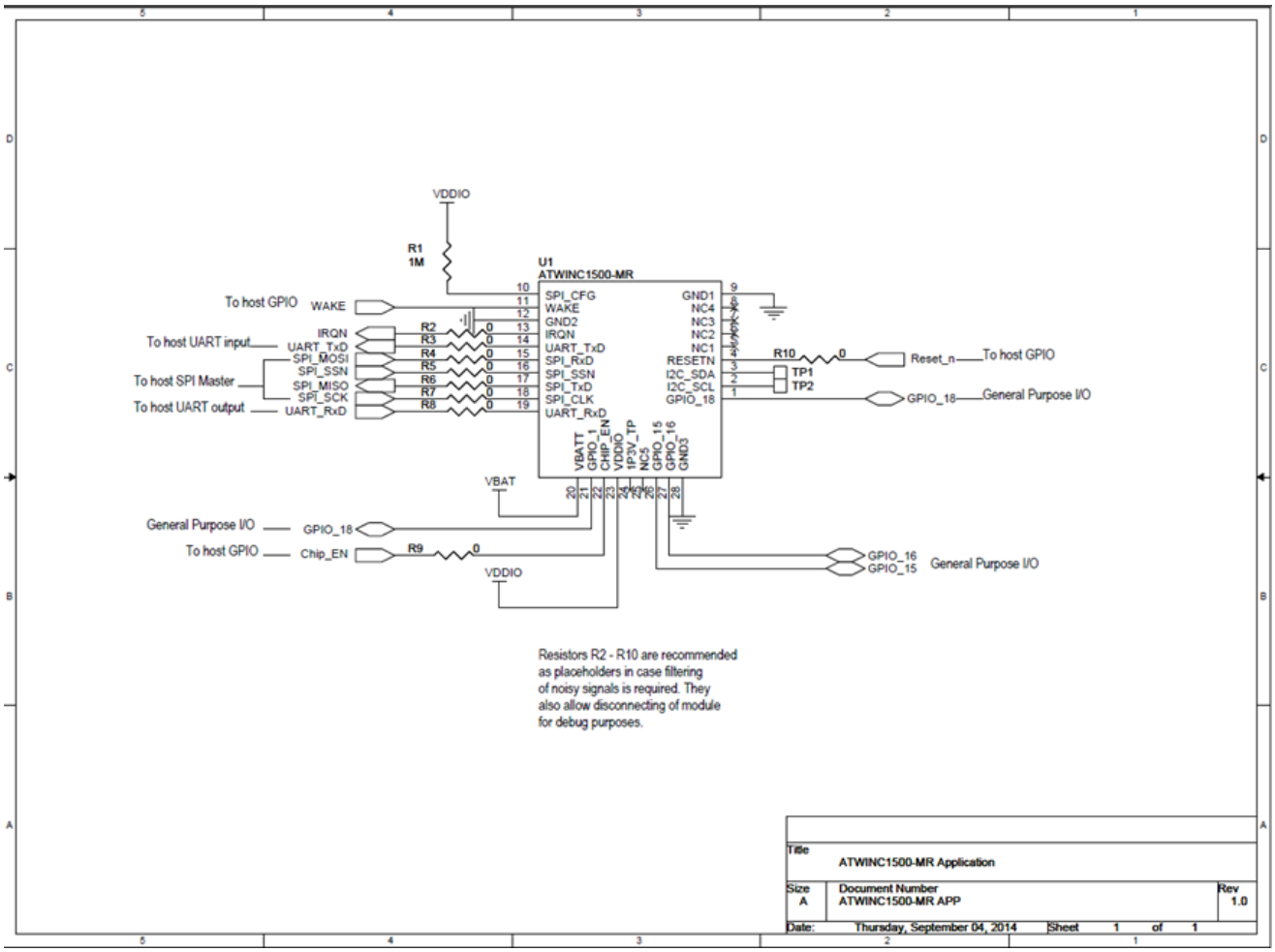


3 Reference Schematic

3.1 Schematic

Figure 3-1 shows the reference schematic for a system using the ATWINC1500-MR210/510 module. Note that there are several 0Ω resistors (R1 – R10) shown in series with signals to the module. These are place holders in case filtering of these lines is necessary due to high frequency in band (2.4GHz) noise is on these lines which can get into the RF path and degrade receiver sensitivity. If the signals coming from the host MCU are noise free, then these placeholders are not required and can be removed.

Figure 3-1. Reference Schematic



4 Notes on Interfacing to the ATWINC1500 Module

4.1 Programmable Pull-up Resistors

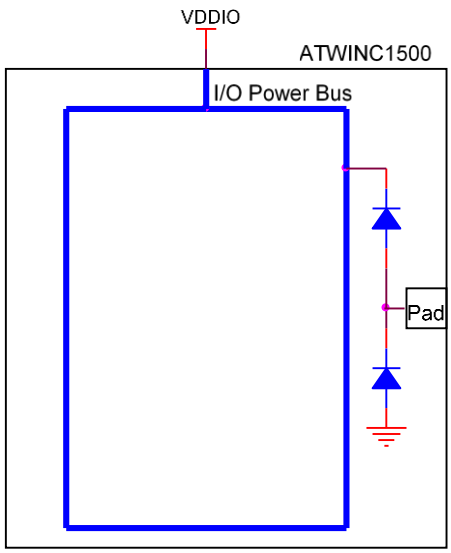
The ATWINC1500-MR210PA provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWINC1500-MR210PA should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC1500-MR210PA is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100kΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100kΩ. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100kΩ = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

See the ATWINC1500-MR210PA Programming Guide for information on enabling/disabling the programmable pull up resistors.

4.2 VDDIO Load Switch

The ATWINC1500-MR210PA module is designed with a load switch in series with the VDDIO supply. The load switch is controlled by the Chip_En pin of the module (Module pin 22). When Chip_En is high, the load switch is turned on. When Chip_En is low the load switch is open and VDDIO is disconnected from the ATWINC1500-MR210P. When the VDDIO supply to the ATWINC1500-MR210PA is disconnected it is important that none of the pins to the ATWINC1500-MR210PA is in a high state. Figure 4-1 shows the ESD structure of the pins of the ATWINC1500 and Figure 4-2 shows the current path through the ESD diode from a pin that is being driven high to the VDDIO supply of the device. In effect, if VDDIO is disconnected from the external power supply and a high level is driven on to a pad of the device, the device will be powered up through the pad.

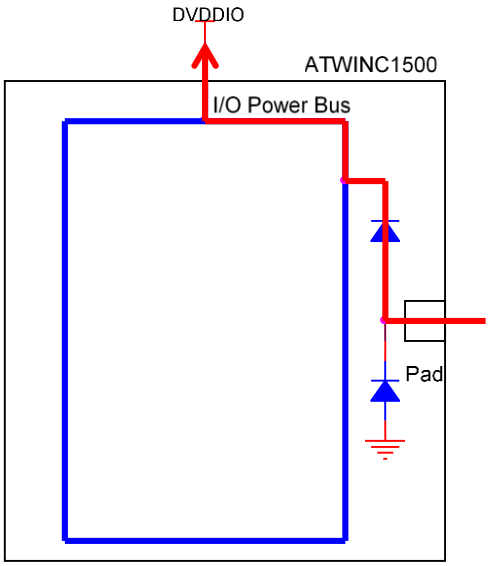
Figure 4-1. ATWINC1500 Pad ESD Structure



This shows why it is important that any time Chip_En to the module is low, all pins interfacing to the module must not be driven or pulled high. They should either be set to a low level or high impedance state. This means

that if any external pull-up resistors are attached to any pins they should be disconnected from the supply when Chip_En is low.

Figure 4-2. Current Path Through ESD Diode



4.3 Restrictions for Power States

When no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

4.4 Power-up/-down Sequence

The power-up/-down sequence for ATWINC1500A is shown in Figure 4-3. The timing parameters are provided in Table 4-1.

Figure 4-3. Power-up/-down Sequence

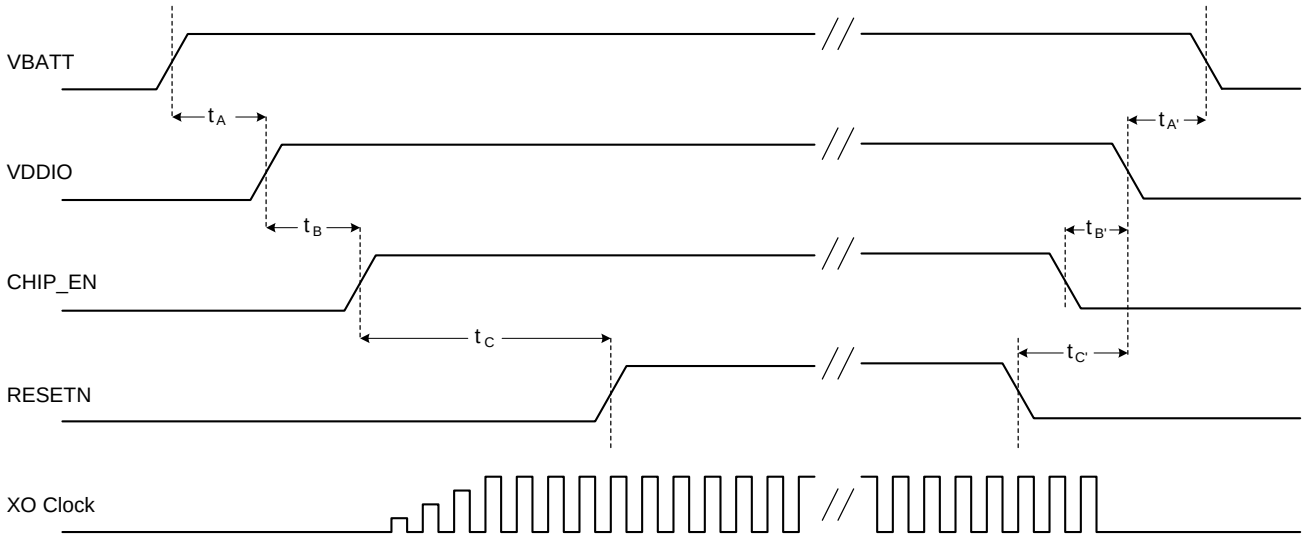


Table 4-1. Power-up/-down Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5			CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0			CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0			RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

4.5 Digital I/O Pin Behavior during Power-Up Sequences

Table 4-2 represents digital I/O pin states corresponding to device power modes.

Table 4-2. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-up/-down Resistor (96kΩ)
Power Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On Sleep/On Transmit/On Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

5 External Interfaces

ATWINC1500-MR210/510 module external interfaces include I²C Slave for control, SPI Slave for control and data transfer, I²C Master for external EEPROM, UART for debug, control, and data transfer, and General Purpose Input / Output (GPIO) pins. For specific programming instructions, refer to ATWINC1500A Programming Guide.

5.1 I²C Slave Interface

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA, Pin J3) and a serial clock (SCL, Pin J2). It responds to the seven bit address value 0x60. The ATWINC1500-MR210 I²C supports I²C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

The I²C Slave timing is provided in Figure 5-1 and Table 5-1.

Figure 5-1. I²C Slave Timing Diagram

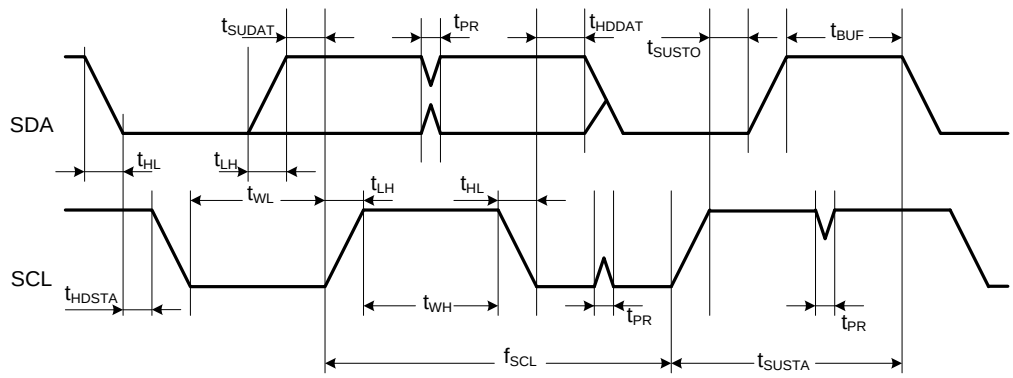


Table 5-1. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming Option

Parameter	Symbol	Min.	Max.	Unit	Remarks
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

5.2 I²C Master Interface

ATWINC1500-MR210 module provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be found on J3. SCL can be found on J2. For more specific instructions, refer to ATWINC1500-MR210 module Programming Guide.

The I²C Master interface supports three speeds:

- Standard mode (100Kb/s)
- Fast mode (400Kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I²C Master interface is the same as that of the I²C Slave interface (see Figure 5-1). The timing parameters of I²C Master are shown in Table 5-2.

Table 5-2. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

5.3 SPI Slave Interface

ATWINC1500-MR210 module provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in Table 5-3. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 5-3. SPI Slave Interface Pin Mapping

Pin #	SPI Function
J10	CFG: Must be tied to VDDIO
J16	SSN: Active Low Slave Select
J18	SCK: Serial Clock
J15	RXD: Serial Data Receive (MOSI)
J17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

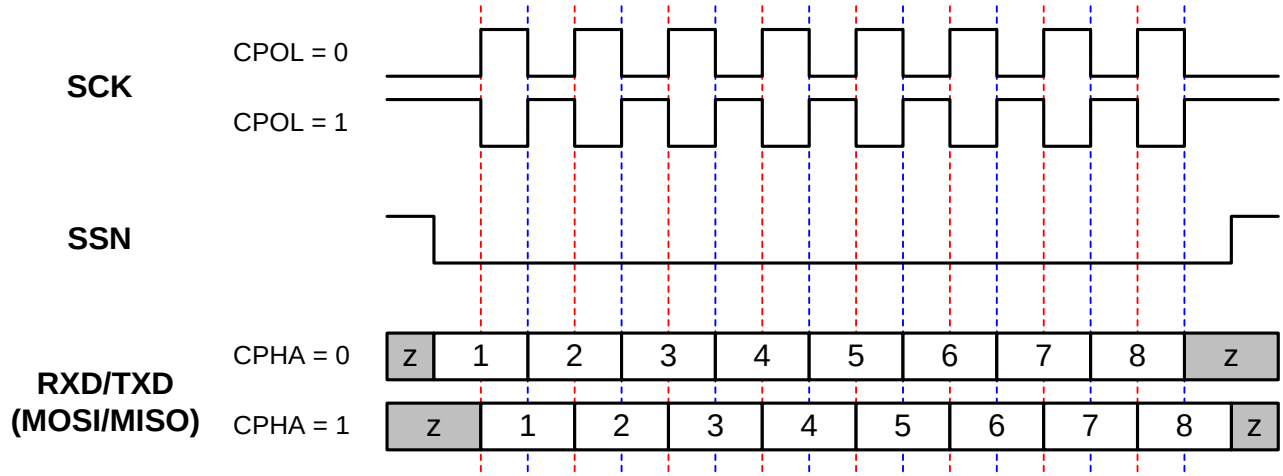
The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions, refer to ATWINC1500-MR210 Programming Guide.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 5-4 and Figure 5-2. The red lines in Figure 5-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 5-4. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 5-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI Slave timing is provided in Figure 5-3 and Table 5-5.

Figure 5-3. SPI Slave Timing Diagram

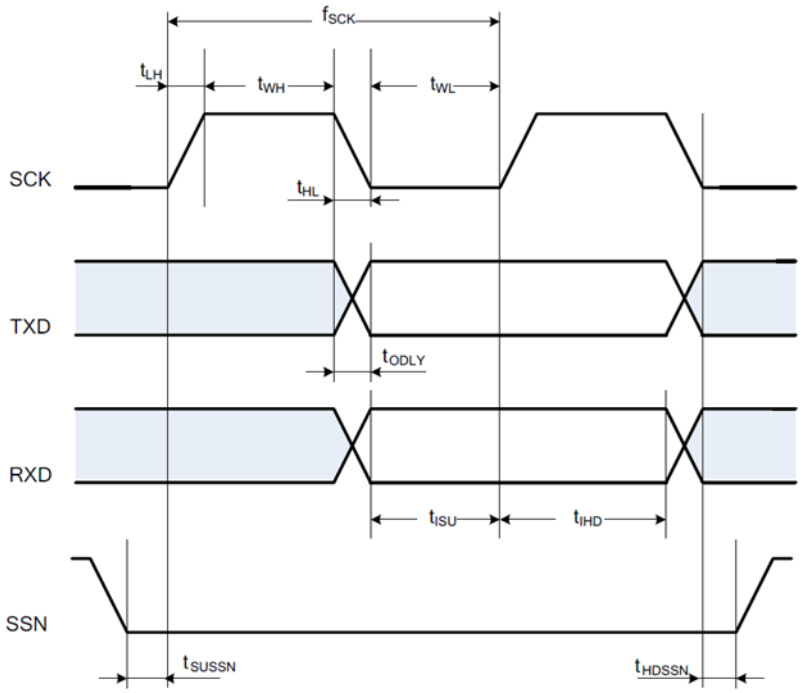


Table 5-5. SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	15		ns
Clock High Pulse Width	t_{WH}	15		
Clock Rise Time	t_{LH}		10	
Clock Fall Time	t_{HL}		10	

Parameter	Symbol	Min.	Max.	Unit
Input Setup Time	t_{ISU}	5		ns
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	20	
Slave Select Setup Time	t_{SUSSN}	5		
Slave Select Hold Time	t_{HDSSN}	5		

5.4 UART

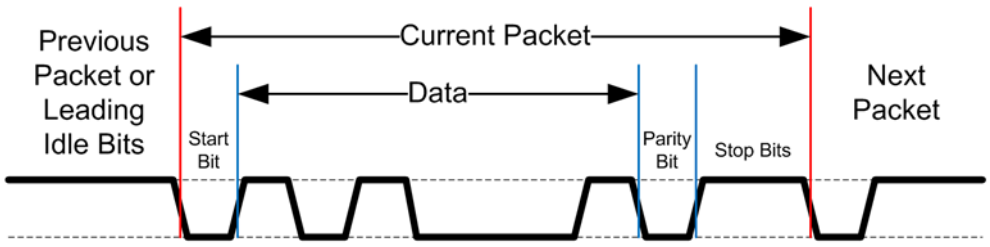
ATWINC1500A has a Universal Asynchronous Receiver/Transmitter (UART) interface for serial communication. It is intended primarily for debugging, and it can also be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWINC1500-MR210 module operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface, where RXD can be found on J14 and TXD can be found on J19. The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz / 8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 5-4. This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions, refer to ATWINC1500-MR210 module Programming Guide.

Figure 5-4. Example of UART RX or TX packet



6 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

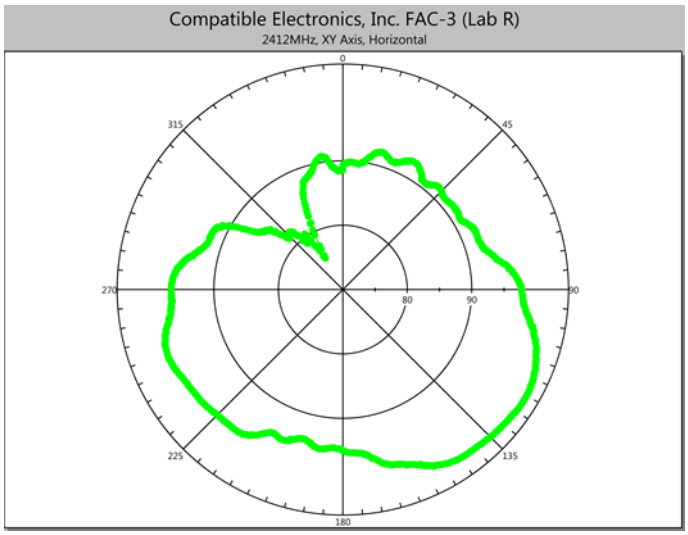
- Module must be placed on main board - printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the main board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board.
- If the module is placed at the edge of the main board, a minimum 22mm by 5mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however deepness of keep-out area must grove to: module edge to main board edge plus 5mm. DO NOT PLACE MODULE IN THE MIDDLE OF THE MAIN BOARD OR FAR AWAY FROM THE MAIN BOARD EDGE.
- The main board should have a solid ground plane. Each ground pin of the module (including each of the center ground pads) should have a via placed either in the pad or right next to the pad going down to the ground plane.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

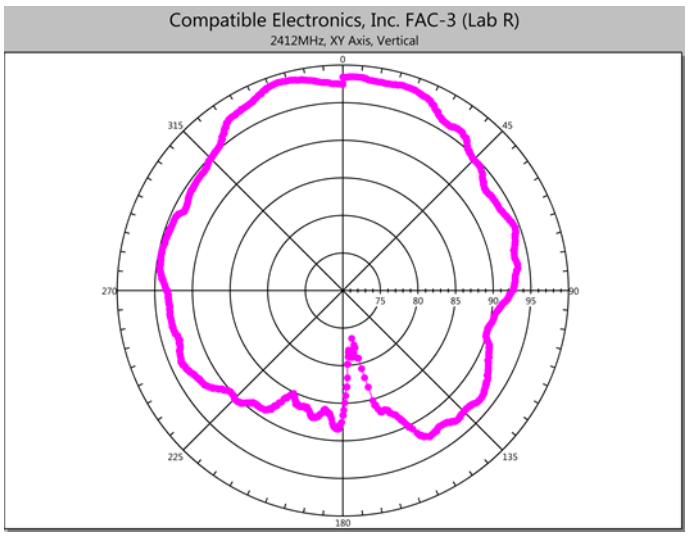
7 Antenna Performance

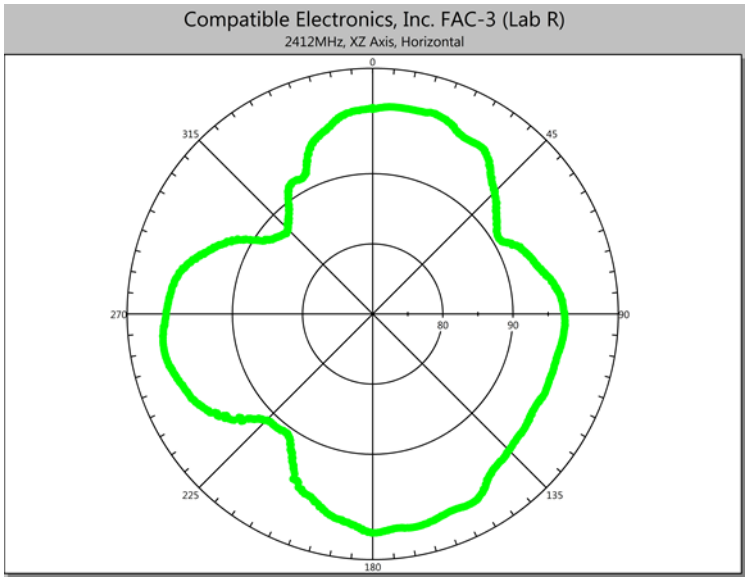
Printed PCB antenna on the ATWINC1500-MR210P is a meandered Inverted F Antenna (IFA). Antenna is fed via matching network which is matched for module installed on 1.5mm thick main board. Main board thickness deviation by ±1mm will change RX/TX performance by ±1dB maximum referring to RX/TX performance with default antenna matching network and installed on 1.5mm thick main board.

Measured antenna gain is -6.16dBi.

Radiated patterns in three directions for horizontal and vertical polarization are shown below.



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2412MHz, XZ Axis, Horizontal
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135
180
225
270
315
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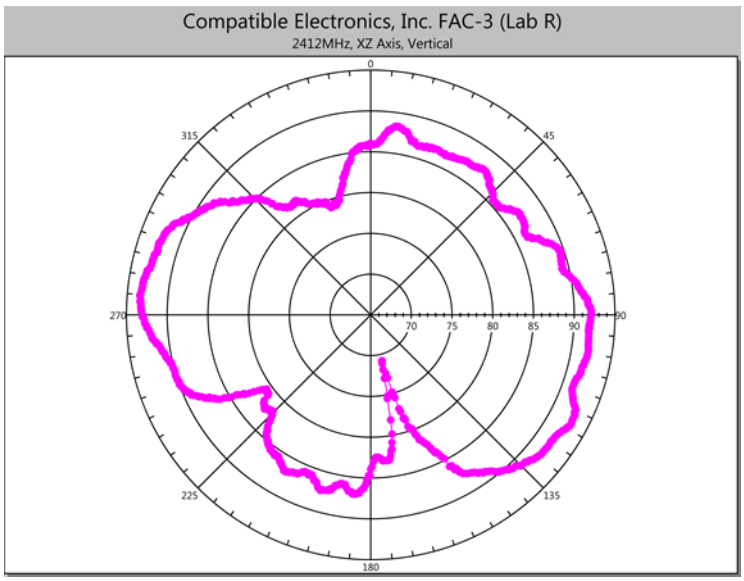
90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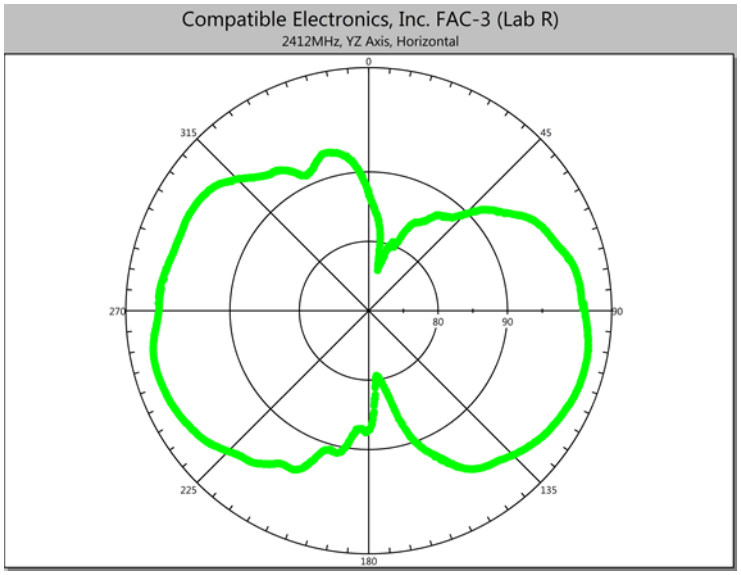
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2412MHz, YZ Axis, Horizontal
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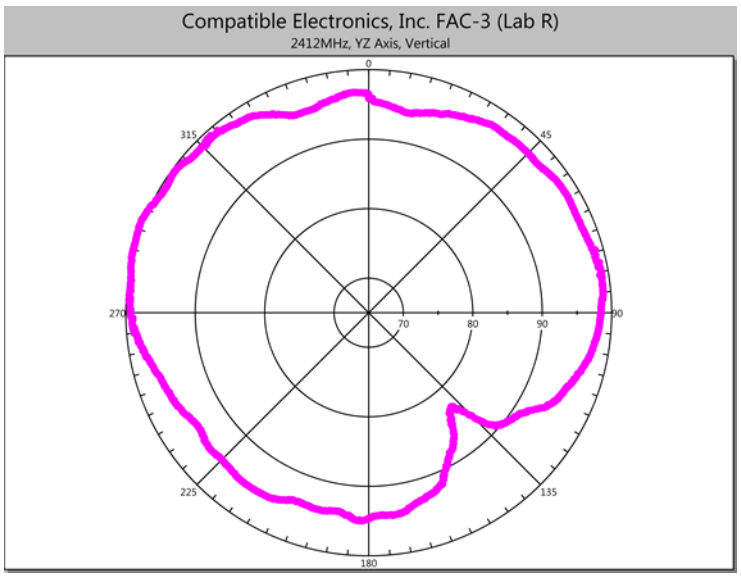
Compatible Electronics, Inc. FAC-3 (Lab R)
2412MHz, YZ Axis, Vertical
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135
180
225
270
315
70
80
90

8 Reference Documentation and Support

8.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents are available on the Atmel web or integrated into development tools.

Table 8-1. Reference Documents

Title	Content
Datasheet	
Design Files	User Guide, Schematic, PCB layout, Gerber, BOM and System notes on: RF/Radio Full Test Report, radiation pattern, design guide-lines, temperature performance, ESD.
Package	How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
Platform Getting started Guide	This document.
HW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Design Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/ or contact the nearest Atmel field representative.

9 Revision History

Doc Rev.	Date	Comments
42430A	03/2015	Initial document release.

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