Precision 5V Reference

FEATURES

- Very Low Drift: 2ppm/°C Max TC
- Pin Compatible with LT1021-5, REF-02, (PDIP Package)
- Output Sources 15mA, Sinks 10mA
- Excellent Transient Response Suitable for A-to-D Reference Inputs
- Noise Reduction Pin
- Excellent Long Term Stability
- Less Than 1ppm $_{P-P}$ Noise (0.1Hz to 10Hz)

APPLICATIONS

- A-to-D and D-to-A Converters
- Digital Voltmeters
- Reference Standard
- Precision Current Source

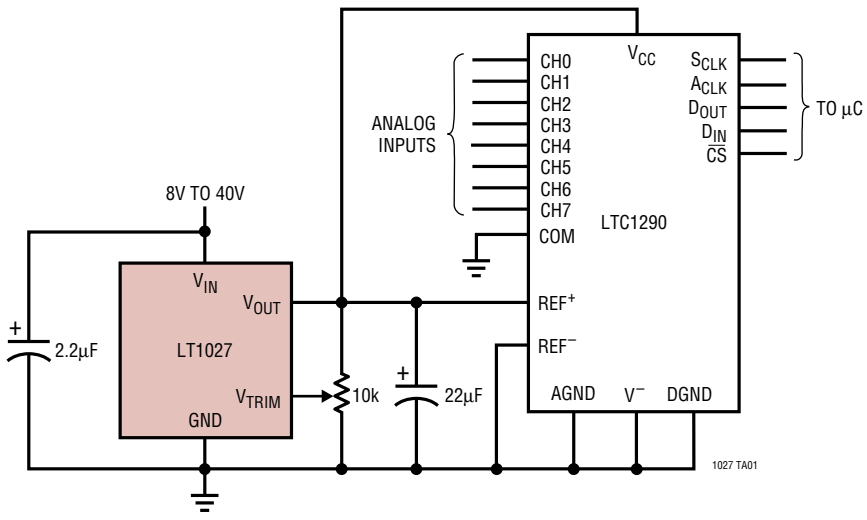
DESCRIPTION

The LT®1027 is a precision reference with extra-low drift, superior accuracy, excellent line and load regulation and low output impedance at high frequency. This device is intended for use in 12- to 16-bit A-to-D and D-to-A systems where demanding accuracy requirements must be met without the use of power hungry, heated substrate references. The fast settling output recovers quickly from load transients such as those presented by A-to-D converter reference inputs. The LT1027 brings together both outstanding accuracy and temperature coefficient specifications.

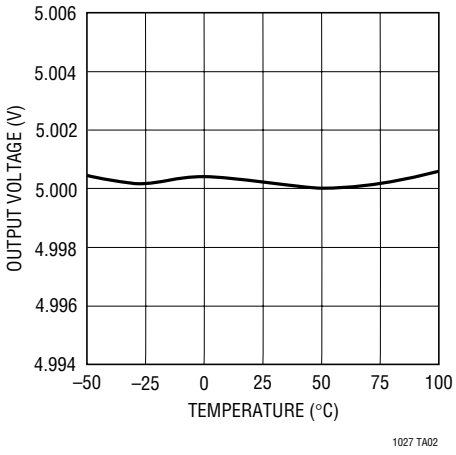
The LT1027 reference is based on LTC's proprietary advanced subsurface Zener bipolar process which eliminates noise and stability problems associated with surface breakdown devices.

TYPICAL APPLICATION

Supplying V_{REF} and V_{CC} to the LTC®1290 12-bit ADC



Output Voltage

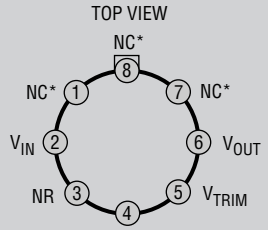


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{IN}) 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage 7V
V_{TRIM} to Ground Voltage
  Positive 5V
  Negative ..... –0.3V
Output Short-Circuit Duration
  V_{IN} > 20V ..... 10 sec
  V_{IN} ≤ 20V ..... Indefinite

Operating Temperature Range
  LT1027C ..... 0°C to 70°C
  LT1027M **(OBSOLETE)** ..... –55°C to 125°C
Storage Temperature Range
  All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

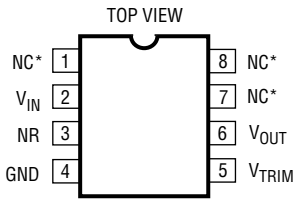


H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

ORDER PART NUMBER
LT1027ACH-5 LT1027BCH-5 LT1027CCH-5 LT1027DCH-5 LT1027ECH-5

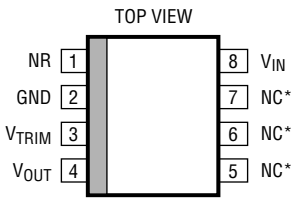
OBSOLETE PACKAGE
Consider the N8 or S8 Packages for Alternate Source



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1027BCN8-5 LT1027CCN8-5 LT1027DCN8-5 LT1027ECN8-5



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 180°C/W

ORDER PART NUMBER
LT1027CCS8-5 LT1027DCS8-5 LT1027ECS8-5
S8 PART MARKING
1027C5 1027D5 1027E5

*Connected internally. Do not connect external circuitry to these pins. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range otherwise specifications are at T_A = 25°C. V_{IN} = 10V, I_{LOAD} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage (Note 2)	LT1027A		4.9990	5.000	5.0010	V
		LT1027B, C, D		4.9975	5.000	5.0025	
		LT1027E		4.9950	5.000	5.0050	
TCV_{OUT}	Output Voltage Temperature Coefficient (Note 3)	LT1027A, B	●		1	2	ppm/°C
		LT1027C	●		2	3	
		LT1027D	●		2	5	
		LT1027E	●		3	7.5	

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range otherwise specifications are at T_A = 25°C. V_{IN} = 10V, I_{LOAD} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Line Regulation (Note 4)	8V ≤ V_{IN} ≤ 10V			6	12	ppm/V
			●			25	ppm/V
		10V ≤ V_{IN} ≤ 40V			3	6	ppm/V
			●			8	ppm/V
	Load Regulation (Notes 4, 6)	Sourcing Current		–8	–3	6	ppm/mA
		0 ≤ I_{OUT} ≤ 15mA	●	–10		8	ppm/mA
		Sinking Current	●		30	120	ppm/mA
		0 ≥ I_{OUT} ≥ –10mA					
	Supply Current				2.2	3.1	mA
			●			3.5	mA
	V_{TRIM} Adjust Range		●	±30	±50		mV
e_n	Output Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			3		μV_{P-P}
		10Hz ≤ f ≤ 1kHz			2.0	6.0	μV_{RMS}
	Temperature Hysteresis	H package; ΔT = 25°C			10		ppm
	Long Term Stability	H package			20		ppm/month

Note 1: Absolute Maximum Ratings are those values beyond which the life of the part may be impaired.

Note 2: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 3: Temperature coefficient is determined by the "box" method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

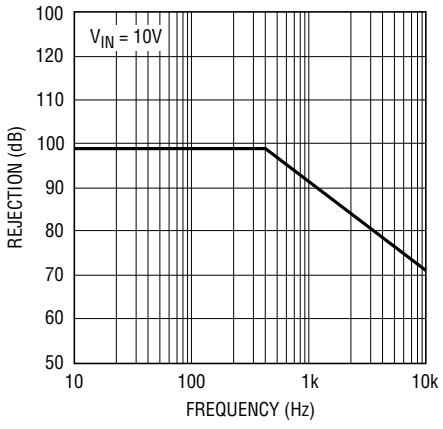
Note 4: Line and load regulation measurements are done on a pulse basis. Output voltage changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W for TO-5 (H), 130°C/W for PDIP (N8), and 180°C/W for plastic SO (SO-8).

Note 5: RMS noise is measured with an 8-pole bandpass filter with a center frequency of 30Hz and a Q of 1.5. The filter output is then rectified and integrated for a fixed time period, resulting in an average, as opposed to RMS voltage. A correction factor is used to convert average to RMS. This value is then used to obtain RMS noise voltage in the 10Hz to 1000Hz frequency band. This test also screens for low frequency "popcorn" noise within the bandwidth of the filter. Consult factory for 100% 0.1Hz to 10Hz noise testing.

Note 6: Devices typically exhibit a slight negative DC output impedance of –0.015Ω. This compensates for PC trace resistance, improving regulation at the load.

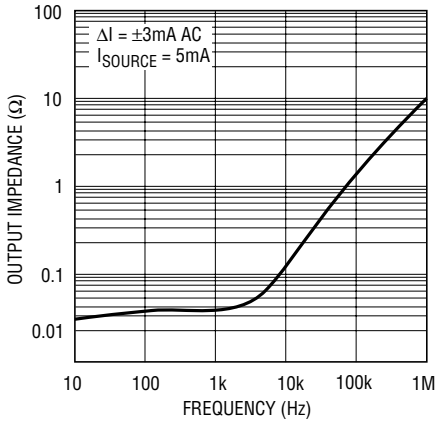
TYPICAL PERFORMANCE CHARACTERISTICS

Ripple Rejection



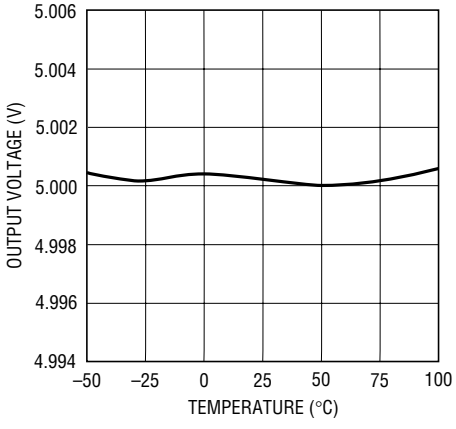
1027 G01

Output Impedance vs Frequency



1027 G02

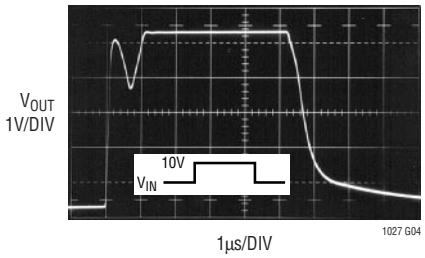
Output Voltage



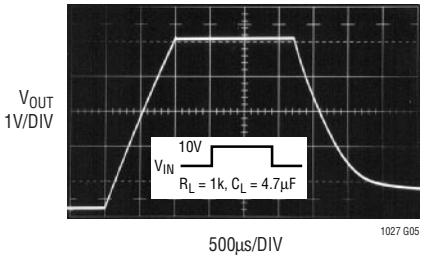
1027 G03

TYPICAL PERFORMANCE CHARACTERISTICS

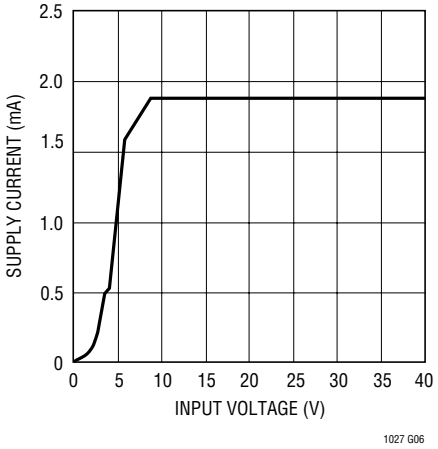
Start-Up and Turn-Off (No Load)



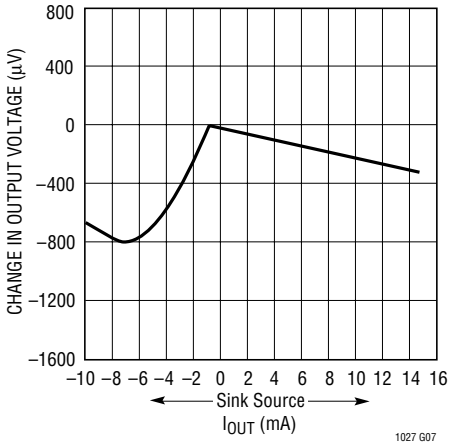
Start-Up and Turn-Off



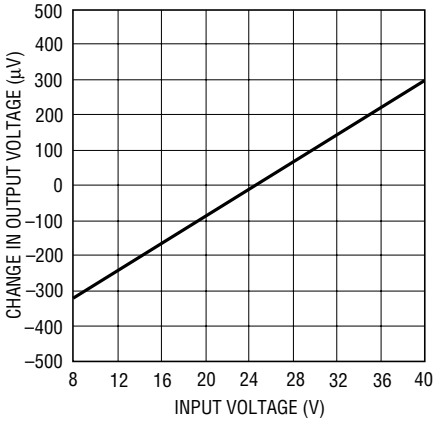
Quiescent Current



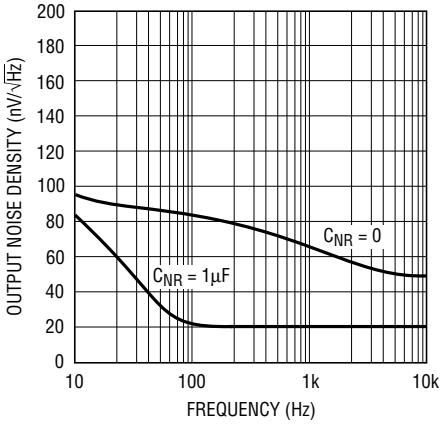
Load Regulation



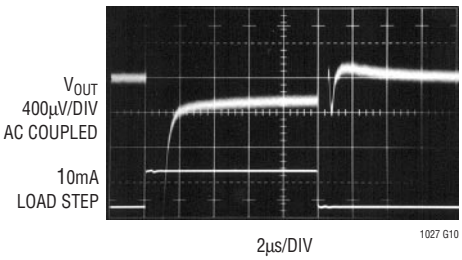
Line Regulation



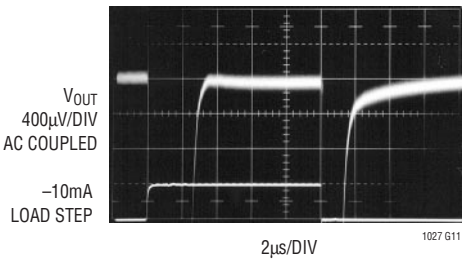
Output Noise Voltage Density



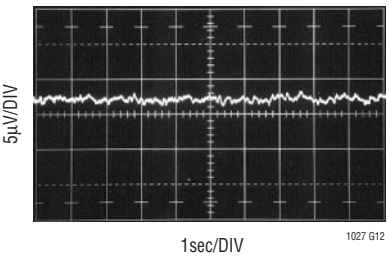
Output Settling Time (Sourcing)



Output Settling Time (Sinking)



0.1Hz to 10Hz Output Noise
Filtering = 1 zero at 0.1Hz
2 poles at 10Hz



APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. Figure 1 indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 0.5LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than 0.5LSB error. For this reason, the LT1027 has been optimized for low drift.

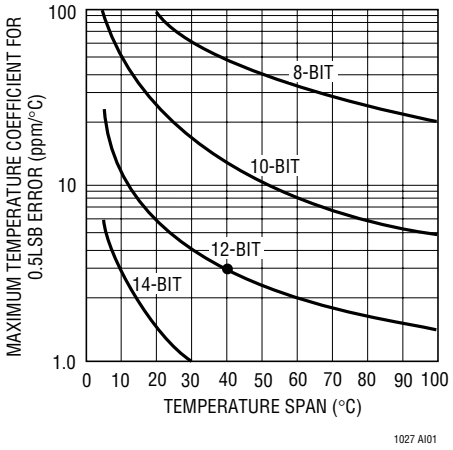


Figure 1. Maximum Allowable Reference Drift

Trimming Output Voltage

The LT1027 has an adjustment pin for trimming output voltage. The impedance of the V_{ADJ} pin is about 20kΩ with an open-circuit voltage of 2.5V. A ±30mV guaranteed trim range is achievable by tying the V_{ADJ} pin to the wiper of a 10k potentiometer connecting between the output and ground. Trimming output voltage does not affect the TC of the device.

Noise Reduction

The positive input of the internal scaling amplifier is brought out as the Noise Reduction (NR) pin. Connecting a 1µF Mylar capacitor between this pin and ground will reduce the wideband noise of the LT1027 from 2.0µV_{RMS} to approximately 1.2µV_{RMS} in a 10Hz to 1kHz bandwidth. Transient response is not affected by this capacitor. Start-up settling time will increase to several milliseconds due to the 7kΩ impedance looking into the NR pin. The capacitor *must* be a low leakage type. Electrolytics are *not* suitable for this application. Just 100nA leakage current will result in a 150ppm error in output voltage. This pin is the most sensitive pin on the device. For maximum protection a guard ring is recommended. The ring should be driven from a resistive divider from V_{OUT} set to 4.4V (the open-circuit voltage on the NR pin).

Transient Response

The LT1027 has been optimized for transient response. Settling time is under 2µs when an AC-coupled 10mA load transient is applied to the output. The LT1027 achieves fast settling by using a class B NPN/PNP output stage. When sinking current, the device may oscillate with capacitive loads greater than 100pF. The LT1027 is stable with all capacitive loads when at no DC load or when sourcing current, although for best settling time either no output bypass capacitor or a 4.7µF tantalum unit is recommended. An 0.1µF ceramic output capacitor will *maximize output ringing* and is *not* recommended.

Kelvin Connections

Although the LT1027 does not have true force-sense capability, proper hook-up can improve line loss and ground loop problems significantly. Since the ground pin of the LT1027 carries only 2mA, it can be used as a low-side sense line, greatly reducing ground loop problems on the low side of the reference. The V_{OUT} pin should be close to the load or connected via a heavy trace as the resistance of this trace directly affects load regulation. It is important to remember that a 1.22mV drop due to trace resistance is equivalent to a 1LSB error in a $5V_{FS}$, 12-bit system.

The circuits in Figures 2 and 3 illustrate proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be further reduced by adding a PNP boost transistor if load current is 5mA or higher. R2 can be added to further reduce current in the output sense load.

APPLICATIONS INFORMATION

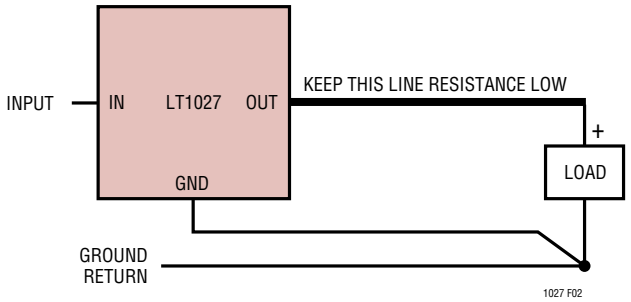
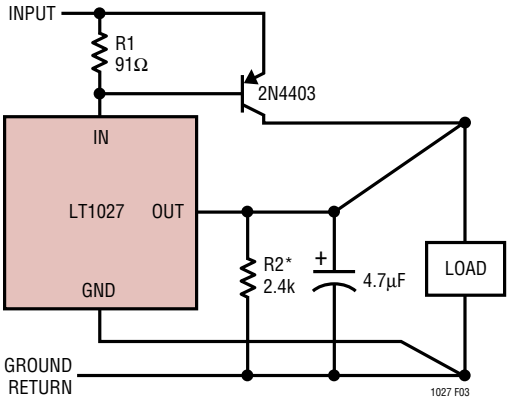


Figure 2. Standard Hook-Up

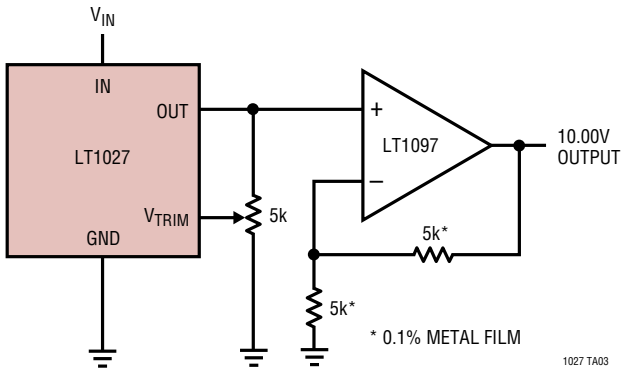


*OPTIONAL–REDUCES CURRENT IN OUTPUT SENSE LEAD

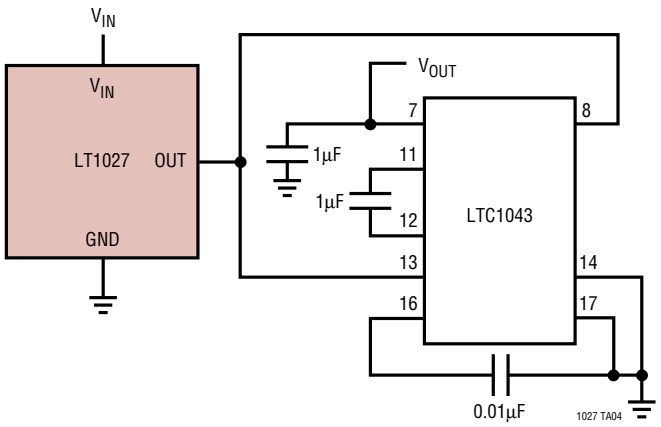
Figure 3. Driving Higher Load Currents

TYPICAL APPLICATIONS

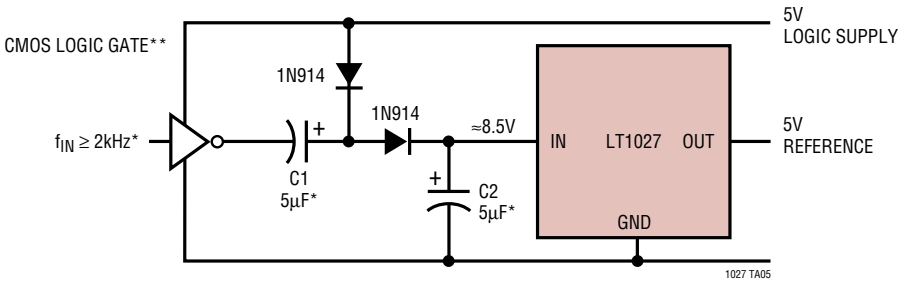
10V Reference



10V Reference

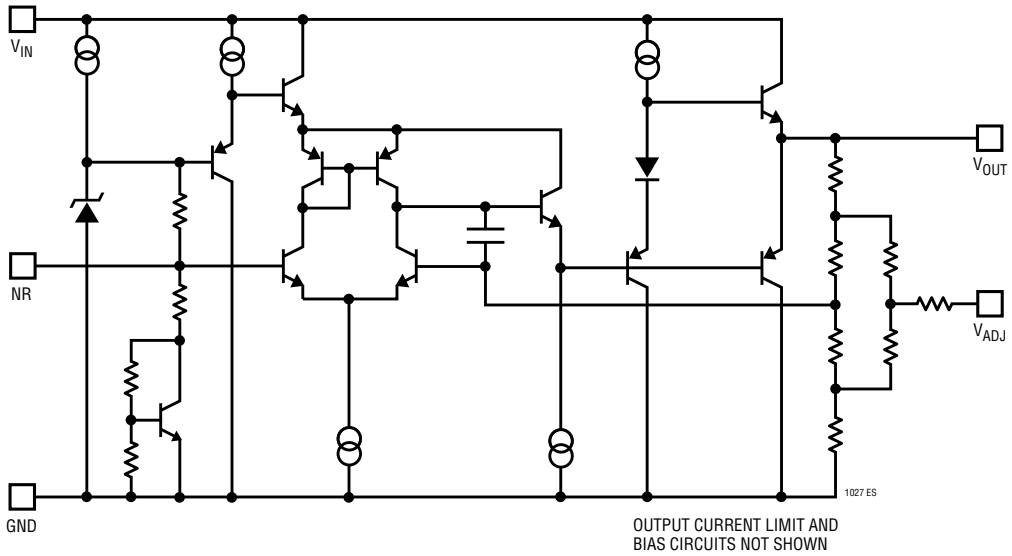


Operating 5V Reference from 5V Supply



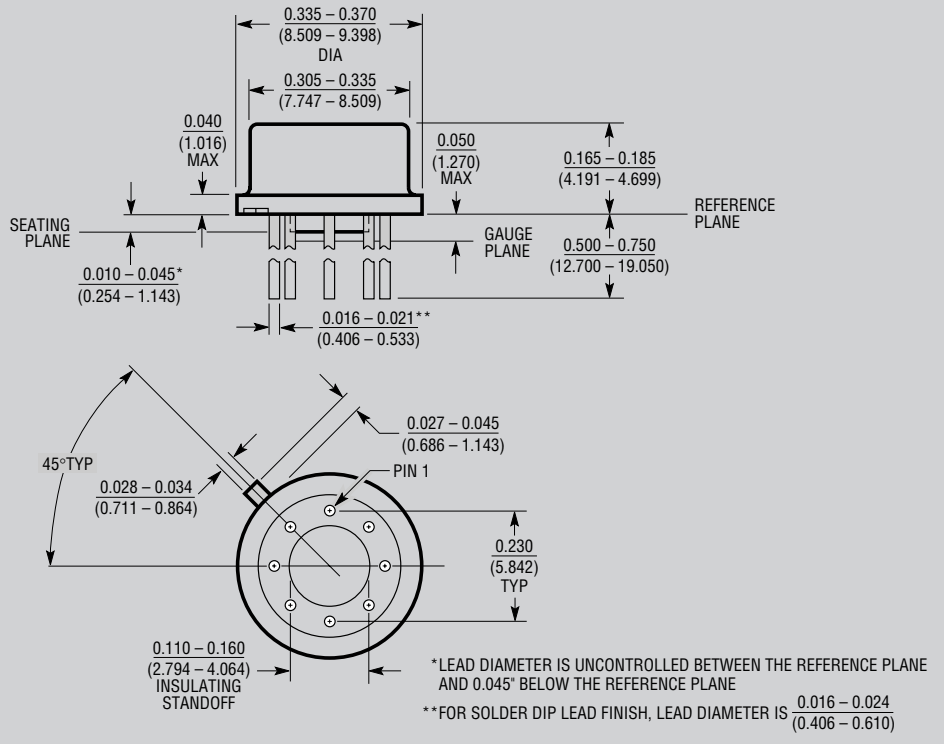
*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING

EQUIVALENT SCHEMATIC



PACKAGE DESCRIPTION

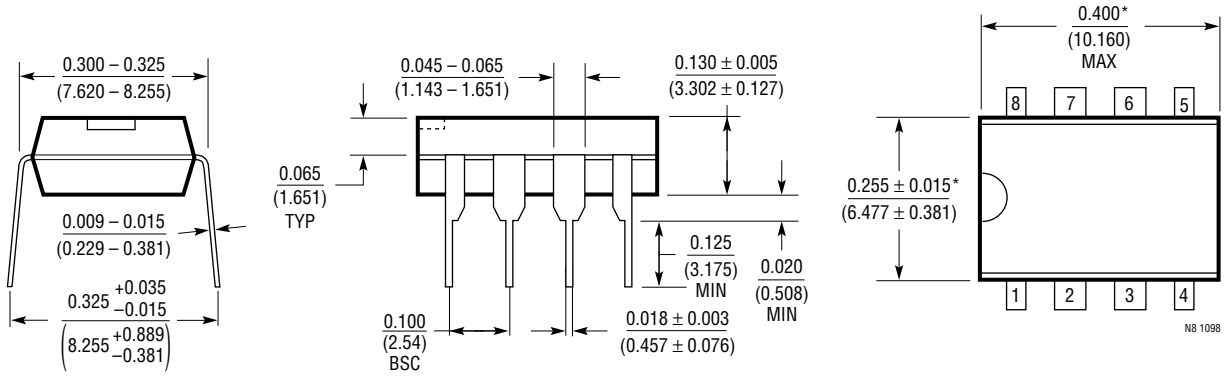
H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
(Reference LTC DWG # 05-08-1321)



OBSOLETE PACKAGE

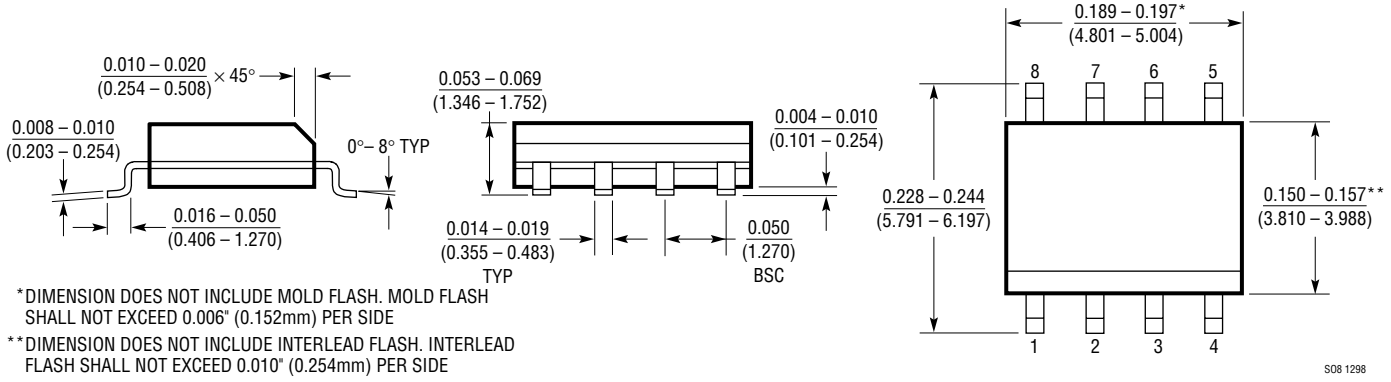
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Series Bandgap Reference, 0.05%, 5ppm/°C Drift	2.5V, 4.5V, 5V, 10V Outputs; Industrial, Military Grades Available
LT1021	Precision Buried Zener Diode Reference, 0.5%, 5ppm/°C Drift	5V, 7V, 10V Outputs; 8-Pin PDIP, SO, TO-5 Packages; Military Grades Available
LT1236	Precision Series Reference, 0.05%, 5ppm/°C Drift	5V, 10V Outputs; 8-Pin PDIP, SO Packages; Industrial Grade Available
LT1460	Micropower Precision Series Bandgap Reference, 0.075%, 10ppm/°C Drift	2.5V, 5V, 10V Outputs; 8-Pin PDIP, SO, MSOP; TO-92 and SOT-23 Packages
LT1461	Low Dropout 3ppm/°C Drift, 0.04% Series Reference	2.5V, SO-8 Package
LT1798	Low Dropout, Micropower Reference	2.5V, 3V, 4.096V, 5V, Adjustable in SO-8

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