µHVIC™

SOT-23 Current Sensing IC

Features

- VDS(on) or VCE(on) sensing
- Eliminates external current sensing resistors
- Enables inductance-less current sensing
- 600V blocking capability
- Programmability and temperature compensation possible
- No VCC required
- Gate drive on/off sync input
- Filter delay at GATE turn-on (200nsec typ.)
- 20.8V zener clamps on GATE and CS pins
- Integrated ESD protection and latch immunity on all pins
- Tiny 5-pin SOT-23 package

Applications

- MOSFET, DirectFET, or IGBT current sensing
- Over-current protection
- Industrial applications
- Motor control
- Power tools
- Brick converters
- Forklifts
- Induction heating

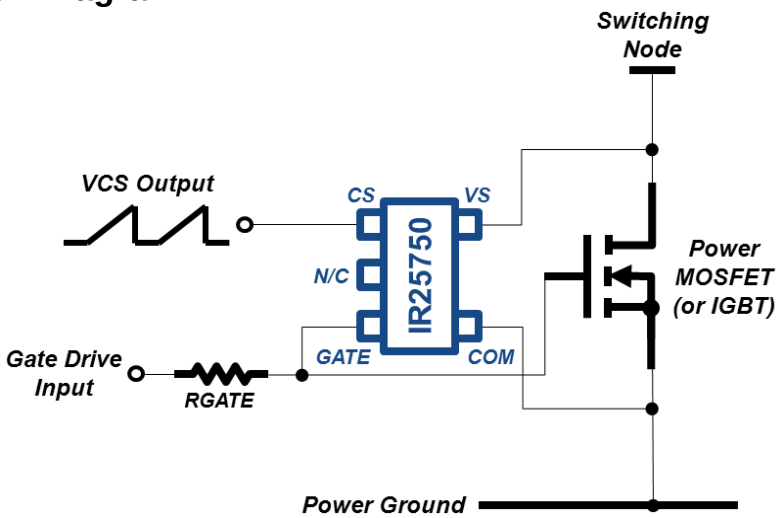
Description

The IR25750L is a novel current sensing IC that extracts the VDS(on) of a power MOSFET, or the VCE(on) of an IGBT, during the switch on-time. IR's proprietary 600V HVIC technology then blocks the high drain voltage to during the MOSFET or IGBT off-time. This IC allows for external current sensing resistors to be eliminated for reducing power losses and increasing overall system efficiency. The IC includes a gate drive input that provides VCC supply voltage to the IC and synchronizes the internal sensing circuit to the on and off times of the switch. Programmability and temperature compensation are also possible.

Package Options

5 Lead SOT 23

Typical Connection Diagram



Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR25750LPBF	SOT23-5L	Tape and Reel	3000	IR25750LTRPBF

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any pin. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_S	VS pin voltage		-20†	625	V
V_{GATE}	GATE pin voltage		-0.3	V_{CLAMP} ††	
V_{CS}	CS pin voltage				
$R\Theta_{JA}$	Thermal resistance, junction to ambient	5L SOT-23	—	191	ºC/W
T_J	Junction temperature		-55	150	ºC
T_S	Storage temperature				
T_L	IC pin temperature (soldering, 10 seconds)		—	300	

† The test condition for the minimum –VS rating is for a pulse width of 1usec. Larger pulse widths will result in a lower –VS voltage rating.

†† This IC contains a 20.8V voltage clamp structure between the GATE and COM pins, and, between the CS and COM pins. Please note that this pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

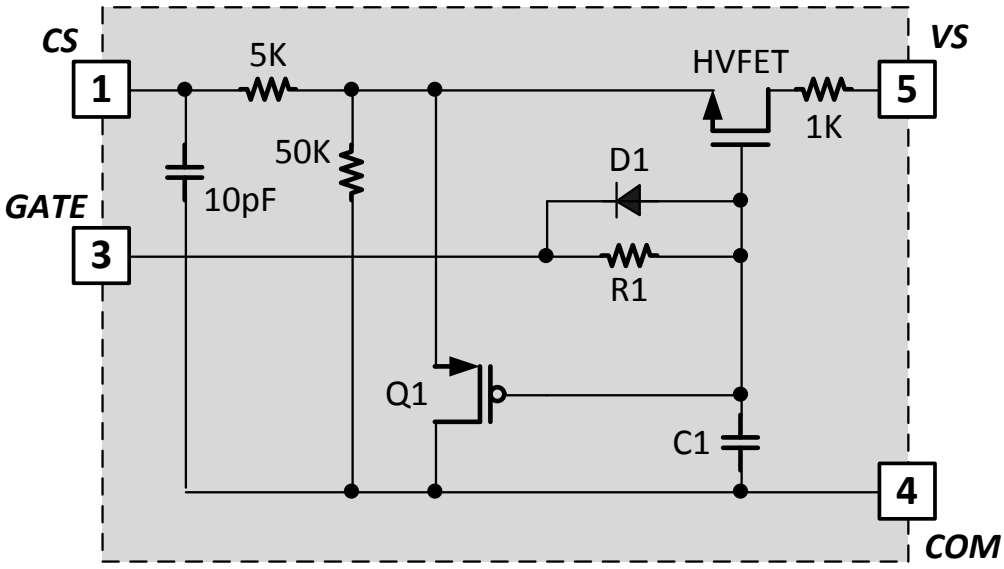
Symbol	Definition	Min	Max	Units
V_S	VS pin voltage	-5.0	600	V
V_{GATE}	GATE pin voltage	COM	V_{CLAMP}	
V_{CS}	CS pin voltage			
T_J	Junction temperature	-40	125	ºC

Electrical Characteristics

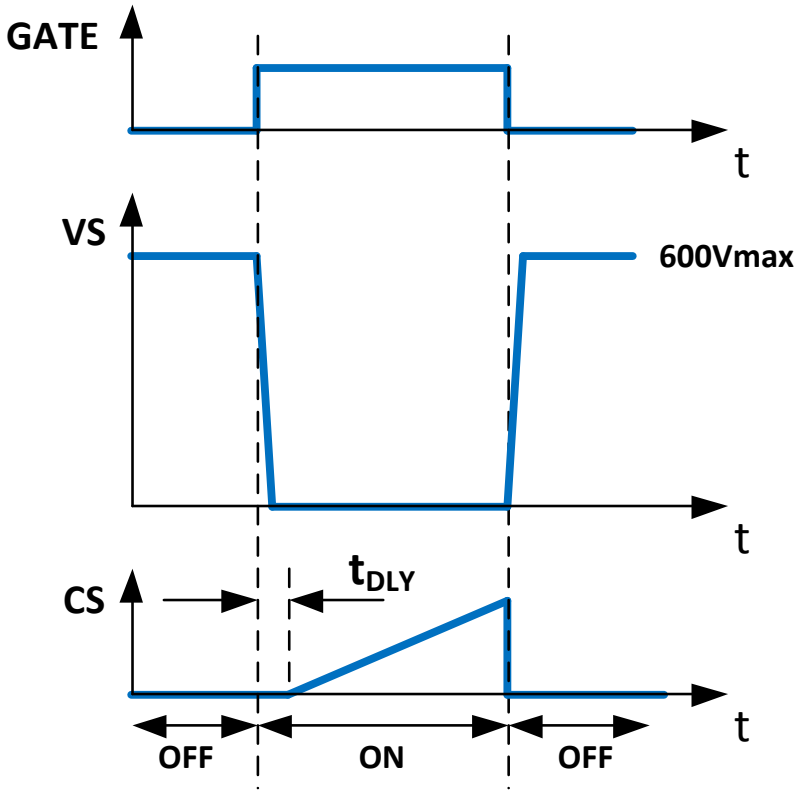
T_A = 25 °C unless otherwise specified. All parameters are referenced to COM.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
GATE Pin Characteristics						
t_{DLY}	GATE-to-CS rising-edge blank delay time	—	200	—	nsec	V_{GATE} = rising edge
V_{CLAMP1}	GATE pin internal Zener clamp voltage	21.1	22.5	24.0	V	I_{GATE} = 1mA
High-Voltage Switching Node Input (VS Pin) Characteristics						
I_{LK}	Offset supply leakage current	—	—	50	µA	V_{GATE} = COM, V_S = 600V
R_{VS_CS}	VS-to-CS 'ON' resistance	—	6.2	—	kΩ	V_{GATE} = 15V
CS Pin Characteristics						
V_{CS_LOW}	CS pin voltage during GATE pin 'low' state	—	COM	—	V	V_{GATE} = COM
V_{CLAMP2}	CS pin internal Zener clamp voltage	—	20.8	—		I_{CS} = 1mA

Functional Block Diagram



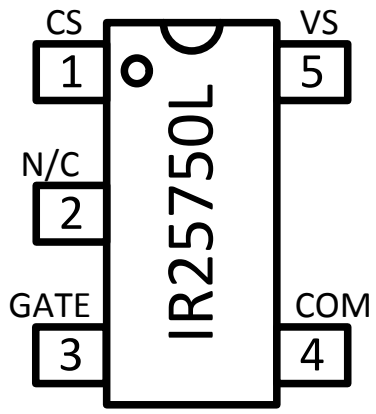
Timing Diagram



Pin Definitions

Pin	Symbol	Description
1	CS	Current sense output
2	N/C	No connect
3	GATE	VCC supply and on/off sync input
4	COM	IC ground
5	VS	Switch drain or collector input sensing node

Pin Assignments



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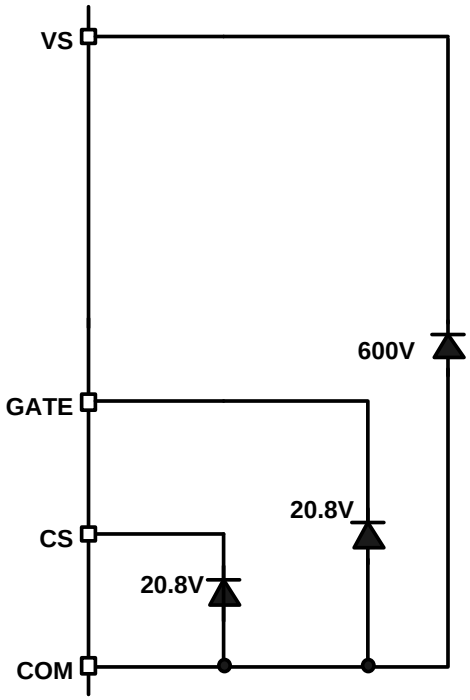
Input / Output Pin Equivalent Circuit Diagrams



Functional Description

I. General Description

The IR25750L current sensing circuit eliminates the traditional series-connected sensing resistor and is connected instead in parallel to the power switch. The circuit measures the VDS(on) of the switching power MOSFET or VCE(on) of an IGBT. The IC has four external connection nodes (VS, GATE, CS, COM) and includes (**Figure 1**): a 600V MOSFET (HVFET); an RC-delay circuit (R1, C1, D1); and a PMOS hold-down transistor (Q1). The circuit does not require a VCC supply node and instead utilizes the existing gate drive signal for powering and turning the circuit on and off. During the off-time of the external power switch (M1), the gate drive signal is at COM, the HVFET is off, Q1 is on, and the CS node is held at COM. Since the internal HVFET is off, any high voltage occurring at the drain of the power MOSFET (600Vmax) will be safely blocked by the HVFET from the rest of the low-voltage circuitry. When M1 is turned on by the gate drive signal, the drain voltage of M1 will decrease to a level given by the VDS(on) of M1. After a short delay time (200nsec, typical) set by the internal R-C delay block (R1, C1), the gate voltage of the HVFET rises up and turns the HVFET on. Q1 turns off, therefore releasing the CS output pin. The VDS(on) of M1 is then transmitted from the VS pin, through the HVFET, to the CS output pin. There is an internal voltage divider formed by a 1Kohm resistor at the VS pin, the RDS(on) of the HVFET (0.2Kohm), and a 50Kohm resistor from the source of HVFET to COM. The ratio of this resistor divider is approximately unity (50/51.2), resulting an excellent matching from the VS pin to the CS pin. A small series R-C filter (5K and 10pF) also exists at the CS pin to help suppress high-frequency noise. Also, important to note, to avoid internal high-voltage damage to the IC, the IR25750L must always turn on after a slight delay from M1 (as set by the internal 200nsec delay block). To ensure this delay, the gate resistor (RGATE) must be placed *before* the GATE pin of the IR25750L and the gate of M1. The GATE pin of the IR25750L and the gate of M1 are then connected together to form a single gate node.

When the gate drive signal of M1 goes low again, M1 turns off, and the gate of the HVFET gets discharged quickly through D1. The HVFET turns off again and blocks any high voltage occurring at the drain of M1. The CS output pin is then held at COM again through Q1. Assuming the drain of M1 is a typical high-voltage switching node that is connected to an inductor, the voltage signal produced at the CS output node will be the same sawtooth waveform that would result from using a traditional current sensing resistor placed at the source of M1 (**Figure 2**). The CS output pin can then be connected to a comparator circuit or used for any other desired current-sensing functions of a PWM controller or MCU circuit.

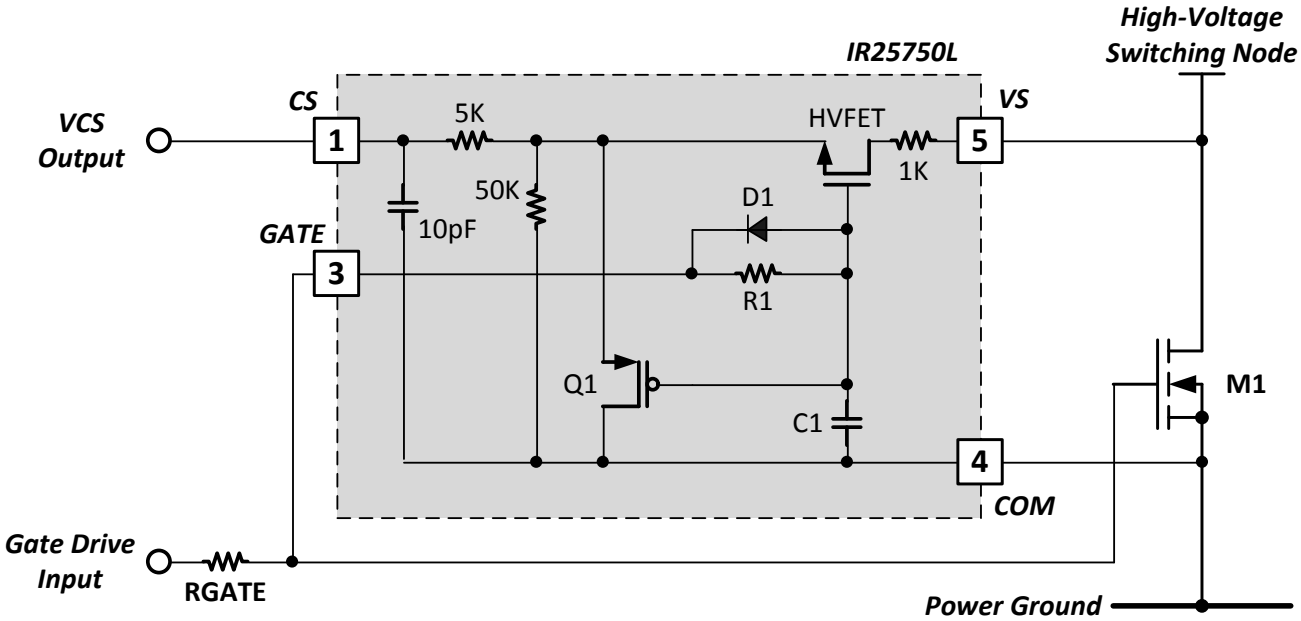


Figure 1: IR25750L internal circuit diagram.

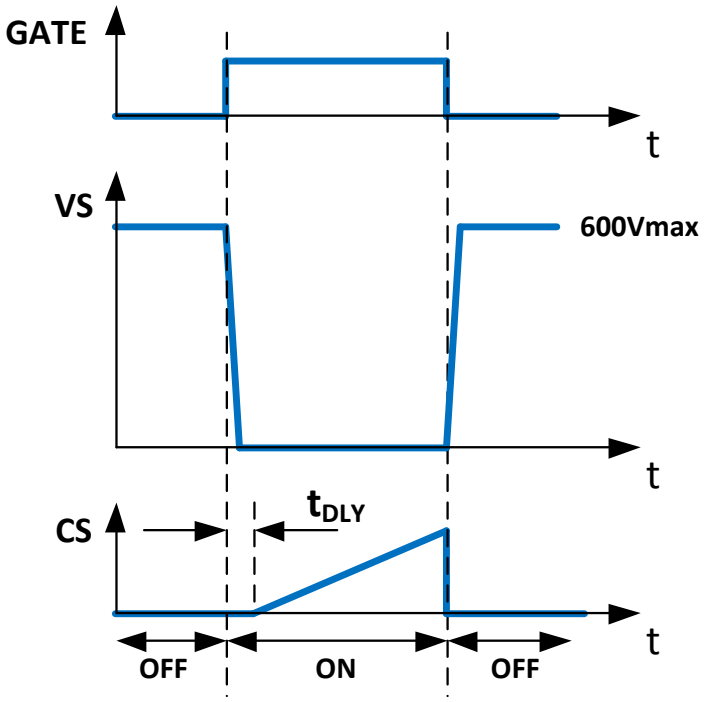


Figure 2: IR25750L timing diagram.

II. PCB Layout Guidelines

Since no VCC node is required for this circuit, the pcb layout becomes very simple to design (**Figure 3**). The IR25750L can be placed conveniently next to the power MOSFET or IGBT and connected easily to the existing pcb traces that are already used for the power switch (GATE, DRAIN, SOURCE). Only the CS trace needs to be routed back to the main PWM controller or MCU of the power supply circuit. Also, important to note, the power ground of the switching circuit must be separate from the COM connection of the IR25750L. The COM pin of the IR25750L should be connected to the source of the power MOSFET with a *single trace only*, and, the power ground *should not* be routed through the COM pin of the IR25750L.

A typical pcb layout is also shown for a DirectFET footprint (**Figure 4**). Again, the IR25750L can be placed directly next to the MOSFET and connected to the existing traces.

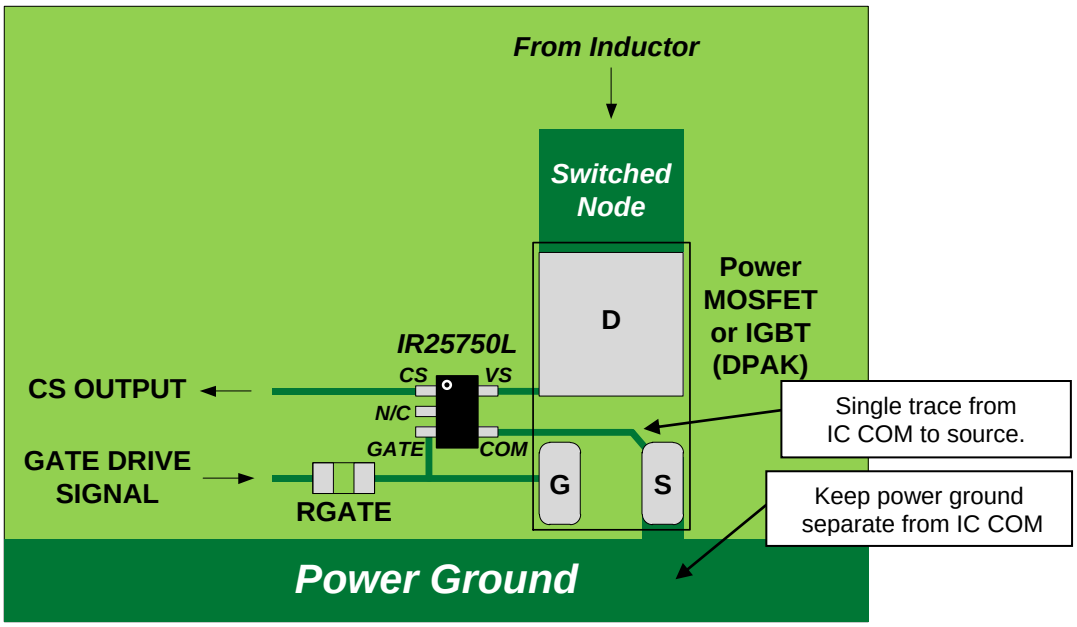


Figure 3: IR25750L typical pcb surface-mount layout (DPAK or D2PAK MOSFET or IGBT).

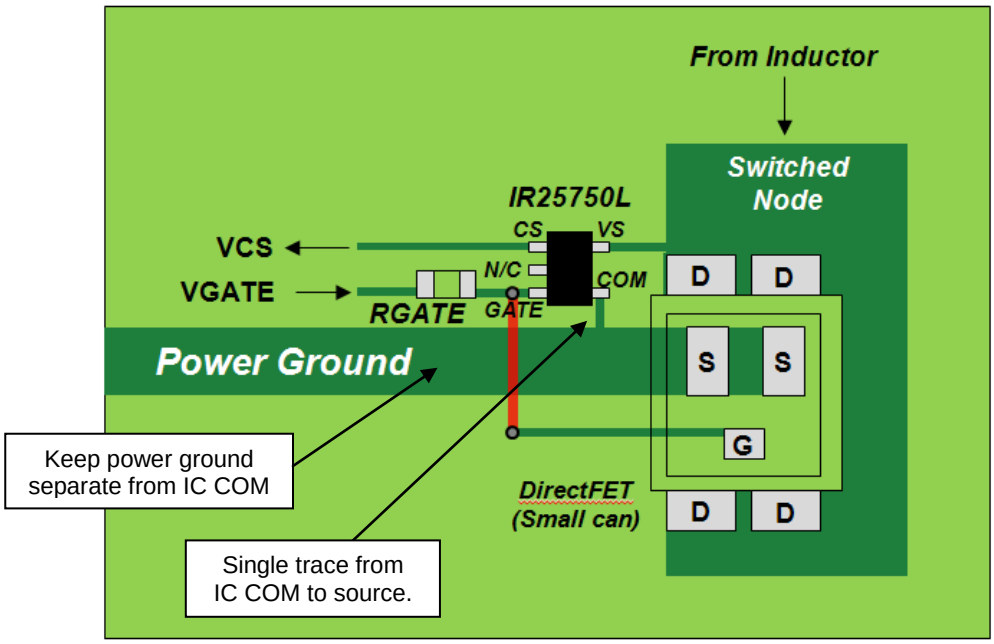


Figure 4: IR25750L typical pcb surface-mount layout (DirectFET).

III. Current Sensing Functionality

With the IR25750L connected properly in a switching circuit application, the waveforms (**Figure 4**) show the functionality of the circuit and the desired current sense signal at the CS pin. Compared to the conventional resistor sensing method, both methods match the actual current shape and both exhibit noise spikes due to switching. Proper filtering or digital blanking of the final PWM or MCU current sensing circuit will easily ignore these noise spikes to prevent any false triggering.

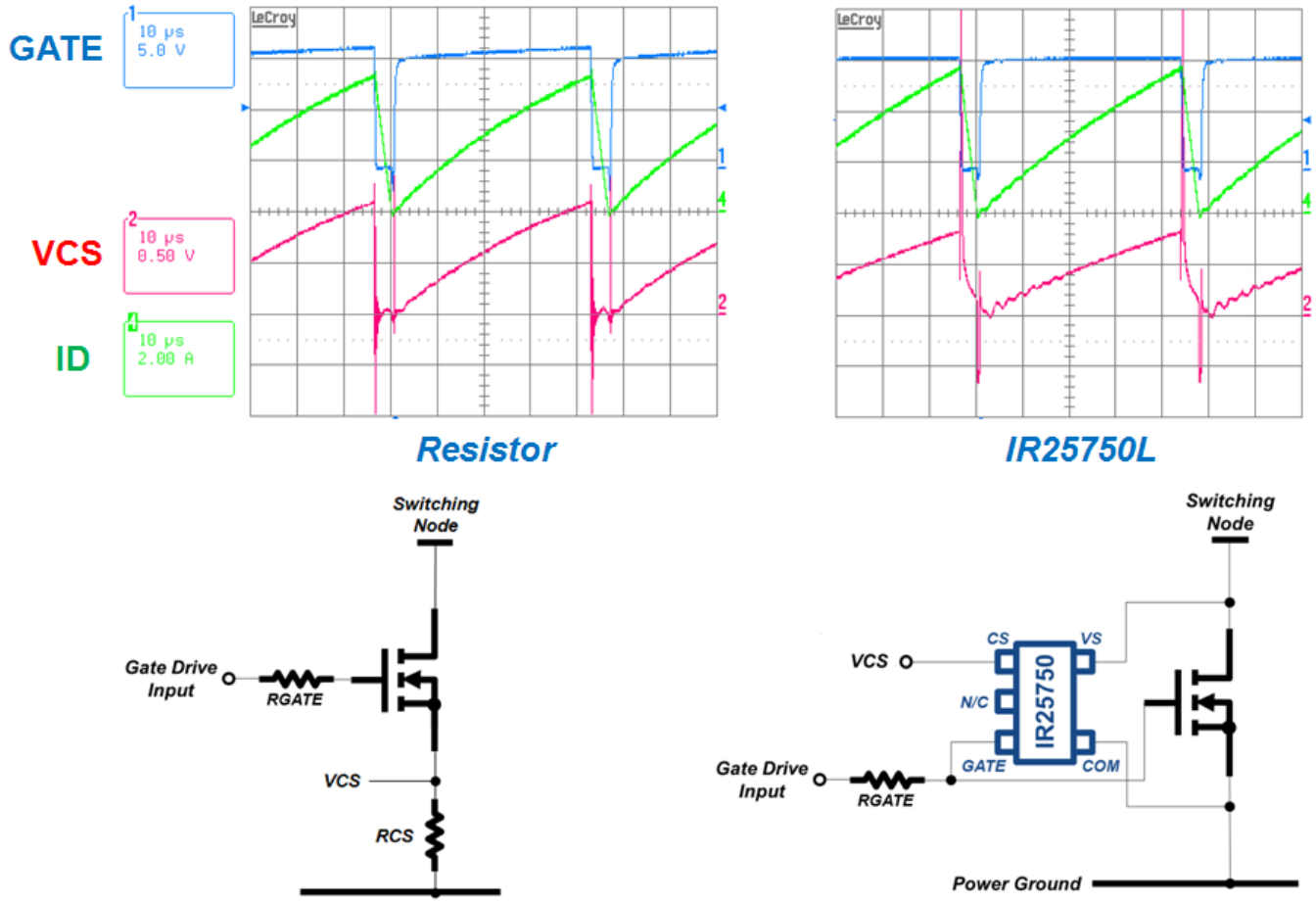
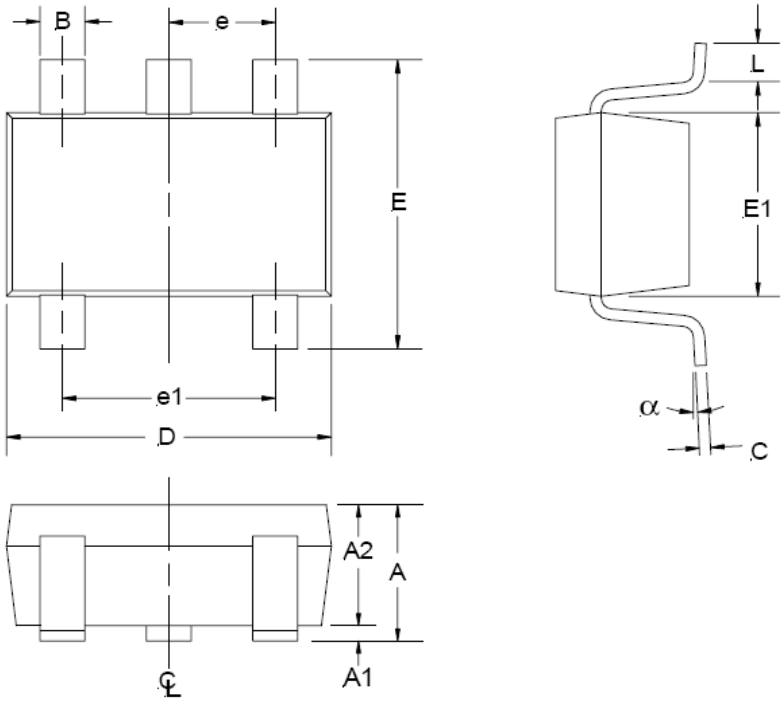


Figure 4: IR25750L switching waveforms vs. resistor method (green=IDRAIN, red=VCS, blue=GATE). (RCS=0.21 ohms, RDS(on)=0.18 ohms)

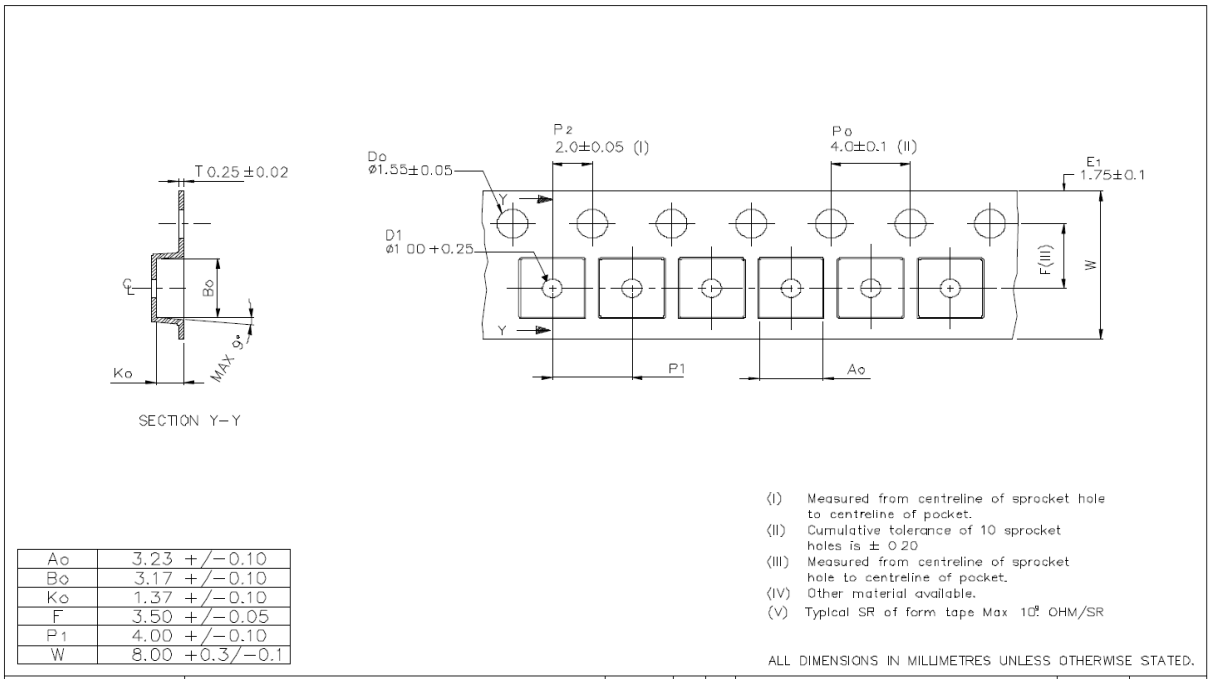
Package Details: 5L SOT-23



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	08	108

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

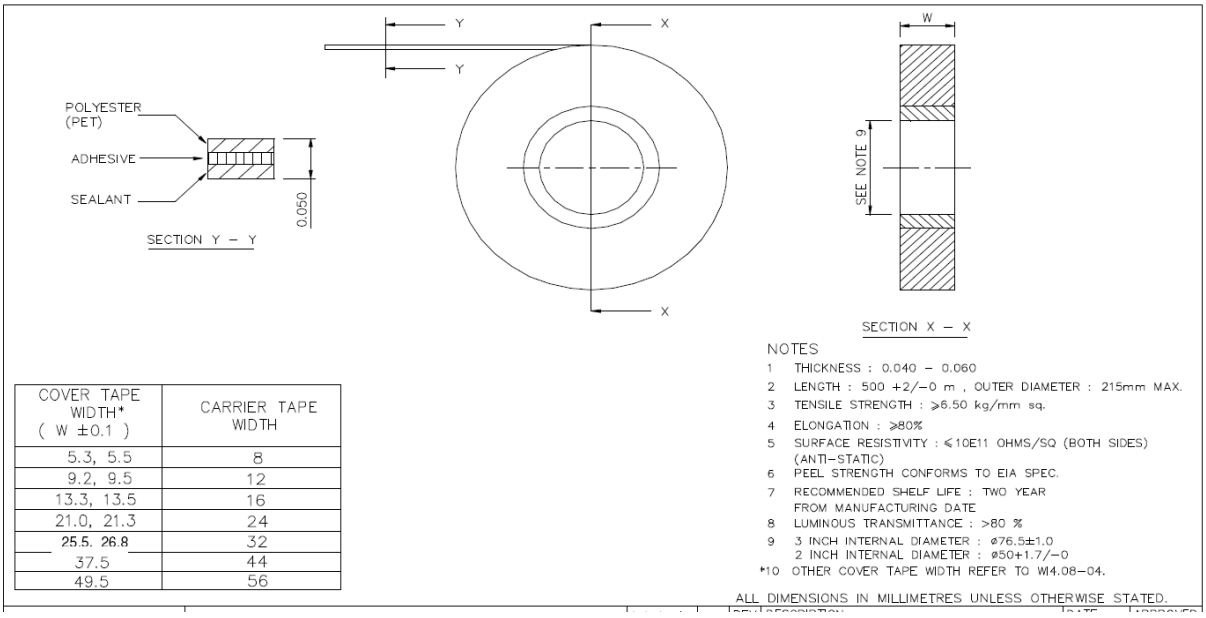
Tape and Reel Details: 5L SOT-23



Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^8 OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

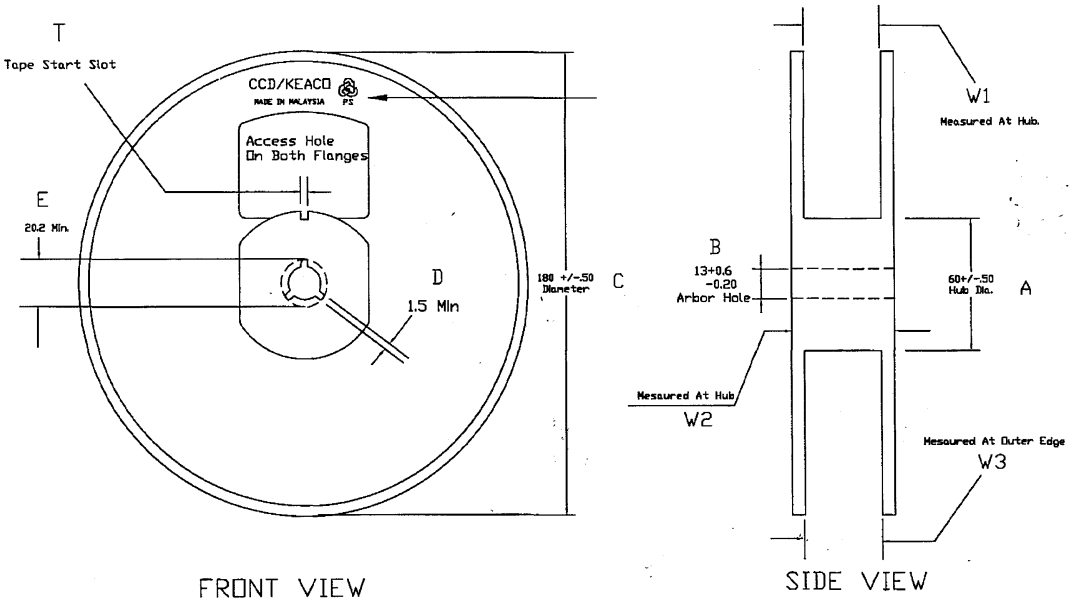


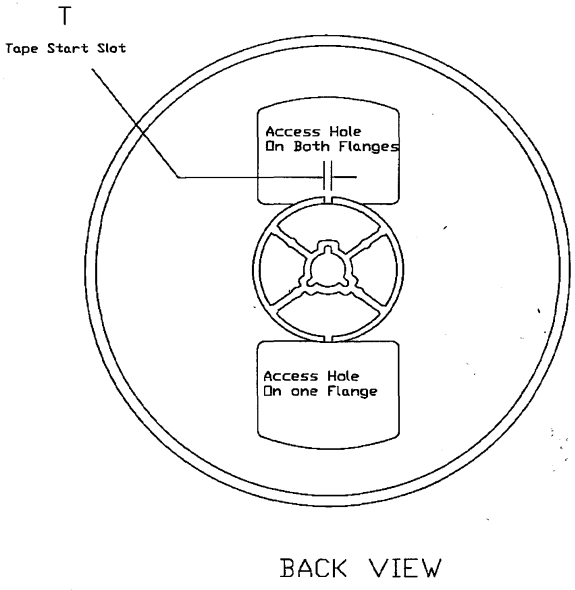
COVER TAPE WIDTH* (W ±0.1)	CARRIER TAPE WIDTH
5.3, 5.5	8
9.2, 9.5	12
13.3, 13.5	16
21.0, 21.3	24
25.5, 26.8	32
37.5	44
49.5	56

NOTES
1 THICKNESS : 0.040 – 0.060
2 LENGTH : 500 +2/−0 m , OUTER DIAMETER : 215mm MAX.
3 TENSILE STRENGTH : ≥6.50 kg/mm sq.
4 ELONGATION : ≥80%
5 SURFACE RESISTIVITY : ≤10E11 OHMS/SQ (BOTH SIDES) (ANTI–STATIC)
6 PEEL STRENGTH CONFORMS TO EIA SPEC.
7 RECOMMENDED SHELF LIFE : TWO YEAR FROM MANUFACTURING DATE
8 LUMINOUS TRANSMITTANCE : >80 %
9 3 INCH INTERNAL DIAMETER : ø76.5±1.0
2 INCH INTERNAL DIAMETER : ø50+1.7/−0
*10 OTHER COVER TAPE WIDTH REFER TO W4.08–04.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Tape and Reel Details: 5L SOT-23

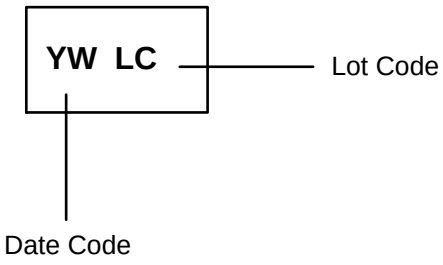




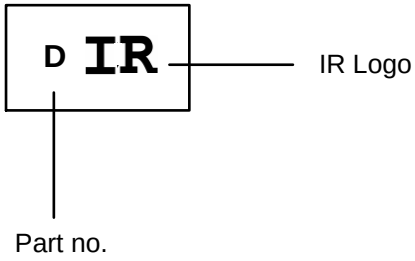
NOTE:
1. MATERIAL : POLYSTRENE
2. SURFACE RESISTIVITY : </= 10E11 OHMS/SQ
(EXTERNAL OR DIPPED)
3. STATIC DECAY : < 2SEC. AT 50%RH

Part Marking Information: 5L SOT-23

Top Marking



Bottom Marking



Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOT-23	MSL1††† (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard EIA/JESD22-A115-A)	
	Human Body Model	Class 1B (per ANSI/ESDA/JEDEC standard JS-001-2012)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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