

## 1:2 LOW-JITTER LVPECL CLOCK BUFFER

### Features

- 2 LVPECL outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: dc to 1250 MHz
- Universal input stage accepts differential or LVCMOS clock
- $V_{DD}$ : 2.5 / 3.3 V
- Small size: 16-QFN (3 mm x 3 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: -40 to +85 °C

### Applications

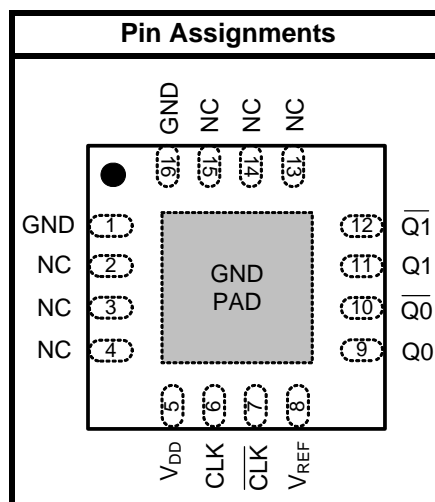
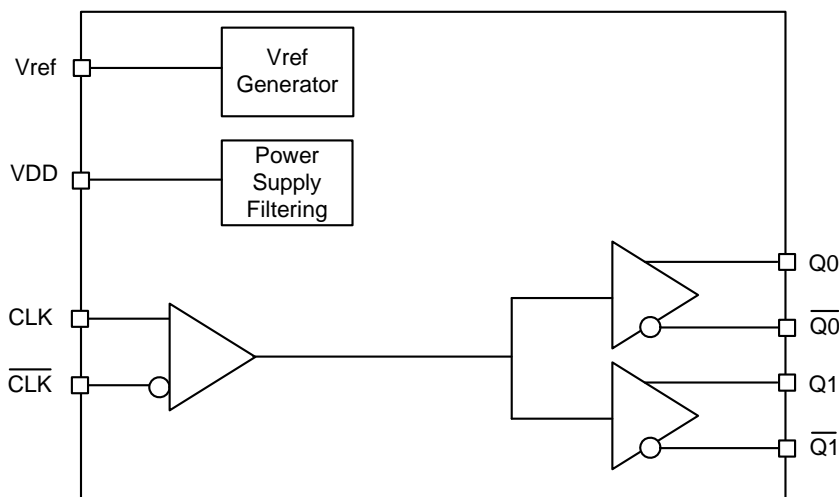
- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

### Description

The Si53322 is an ultra-low-jitter two-output LVPECL buffer. Utilizing Silicon Laboratories' advanced fan-out clock technology, the Si53322 guarantees low additive jitter, low skew, and low propagation delay variability from dc to 1250 MHz.

The Si53322 features minimal cross-talk and excellent supply noise rejection, simplifying low-jitter clock distribution in noisy environments.

### Functional Block Diagram



Patents pending



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## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	$T_A$		-40	—	85	°C
Supply Voltage Range*	$V_{DD}$	LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V

**Table 2. Input Clock Specifications**

( $V_{DD} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	$V_{CM}$	$V_{DD} = 2.5\text{ V} \pm 5\%$ , $3.3\text{ V} \pm 10\%$	0.05	—	—	V
Differential Input Swing (peak-to-peak)	$V_{IN}$		0.2	—	2.2	V
Input High Voltage	$V_{IH}$	$V_{DD} = 2.5\text{ V} \pm 5\%$ , $3.3\text{ V} \pm 10\%$	$V_{DD} \times 0.7$	—	—	V
Input Low Voltage	$V_{IL}$	$V_{DD} = 2.5\text{ V} \pm 5\%$ , $3.3\text{ V} \pm 10\%$	—	—	$V_{DD} \times 0.3$	V
Input Capacitance	$C_{IN}$	CLK pins with respect to GND	—	5	—	pF

**Table 3. DC Common Characteristics** $(V_{DD} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	$I_{DD}$		—	55	100	mA
Output Buffer Supply Current (Per Clock Output) @ 100 MHz	$I_{DDOX}$	LVPECL (3.3 V)	—	35	—	mA
Voltage Reference	$V_{REF}$	$V_{REF}$ output pin ( $V_{DD} = 2.5, 3.3\text{ V}$ )	—	$V_{DD} - 1.3\text{ V}$	—	V
Input High Voltage	$V_{IH}$	CLK_SEL	$0.8 \times V_{DD}$	—	—	V
Input Low Voltage	$V_{IL}$	CLK_SEL	—	—	$0.2 \times V_{DD}$	V
Output Voltage High	$V_{OH}$	$I_{DD} = -1\text{ mA}$	$0.8 \times V_{DD}$	—	—	V
Output Voltage Low	$V_{OL}$	$I_{DD} = 1\text{ mA}$	—	—	$0.2 \times V_{DD}$	V
Internal Pull-down Resistor	$R_{DOWN}$	CLK_SEL	—	25	—	$k\Omega$

**Table 4. Output Characteristics (LVPECL)**

( $V_{DD} = 2.5\text{ V} \pm 5\%$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	$V_{COM}$		$V_{DDOX} - 1.595$	—	$V_{DDOX} - 1.245$	V
Single-Ended Output Swing*	$V_{SE}$		0.35	0.60	1.050	V

**\*Note:** Unused outputs can be left floating. Do not short unused outputs to ground.

**Table 5. AC Characteristics**

( $V_{DD} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL	dc	—	1250	MHz
Duty Cycle <b>Note:</b> 50% input duty cycle.	$D_C$	20/80% $T_R/T_F < 10\%$ of period (LVPECL)	47	50	53	%
Minimum Input Clock Slew Rate	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	$T_R/T_F$	LVPECL	—	—	350	ps
Minimum Input Pulse Width	$T_W$		500	—	—	ps
Additive Jitter (Differential Clock Input)	J	$V_{DD} = 2.5 / 3.3\text{ V}$ , $F = 725\text{ MHz}$ , 0.75 V/ns input slew rate	—	50	65	fs
Propagation Delay	$T_{PLH}$ , $T_{PHL}$	LVPECL	575	775	975	ps
Output to Output Skew <sup>1</sup>	$T_{SK}$	LVPECL	—	20	50	ps
Part to Part Skew <sup>2</sup>	$T_{PS}$	LVPECL	—	—	125	ps
Power Supply Noise Rejection <sup>3</sup>	PSRR	10 kHz sinusoidal noise	—	-70	—	dBc
		100 kHz sinusoidal noise	—	-65	—	dBc
		500 kHz sinusoidal noise	—	-60	—	dBc
		1 MHz sinusoidal noise	—	-57.5	—	dBc

**Notes:**

1. Output to output skew specified for outputs with an identical configuration.
2. Defined as skew between any output on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
3. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DD}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

Table 6. Additive Jitter, Differential Clock Input

V <sub>DD</sub>	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude V <sub>IN</sub> (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	55	75
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
2.5	725	Differential	0.15	0.637	LVPECL	55	75
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185

**Notes:**

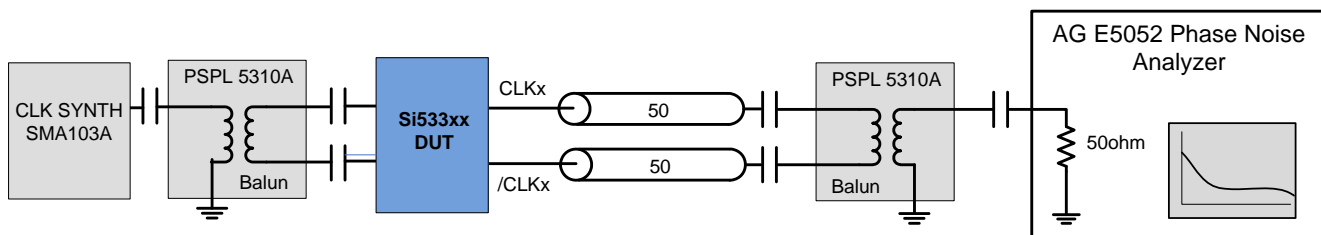
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

**Table 7. Additive Jitter, Single-Ended Clock Input**

V <sub>DD</sub>	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude V <sub>IN</sub> (Single-Ended, Peak to Peak)	SE 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185

**Notes:**

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input (see Figure 1).



**Figure 1. Differential Measurement Method Using a Balun**

Table 8. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Still air	57.6	°C/W
Thermal Resistance, Junction to Case	$\theta_{JC}$	Still air	41.5	°C/W

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	$T_S$		-55	—	150	°C
Supply Voltage	$V_{DD}$		-0.5	—	3.8	V
Input Voltage	$V_{IN}$		-0.5	—	$V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$		—	—	$V_{DD} + 0.3$	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 k $\Omega$	—	—	2000	V
ESD Sensitivity	CDM		—	—	1250	V
Peak Soldering Reflow Temperature	$T_{PEAK}$	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	$T_J$		—	—	125	°C

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2. Functional Description

The Si53322 is a low-jitter, low-skew 1:2 LVPECL buffer. The device has a universal input that accepts most common differential or LVCMOS input signals.

### 2.1. Universal, Any-Format Input

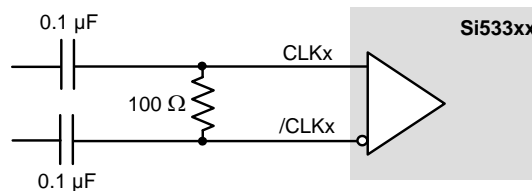
The Si53322 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 10 and 11 summarize the various ac- and dc-coupling options supported by the device. Figures 3 and 4 show the recommended input clock termination options. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended since low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. For more information, see “AN766: Understanding and Optimizing Clock Buffer Additive Jitter Performance”.

**Table 10. LVPECL, LVCMOS, and LVDS**

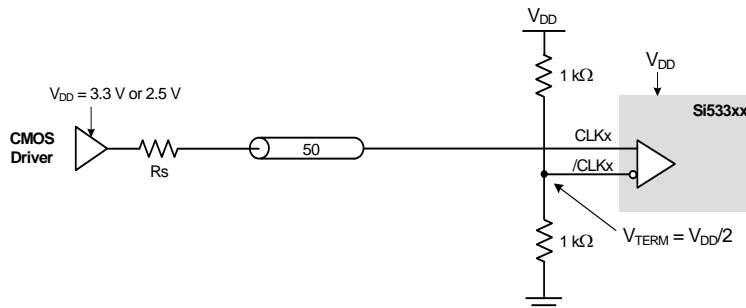
	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

**Table 11. HCSL and CML**

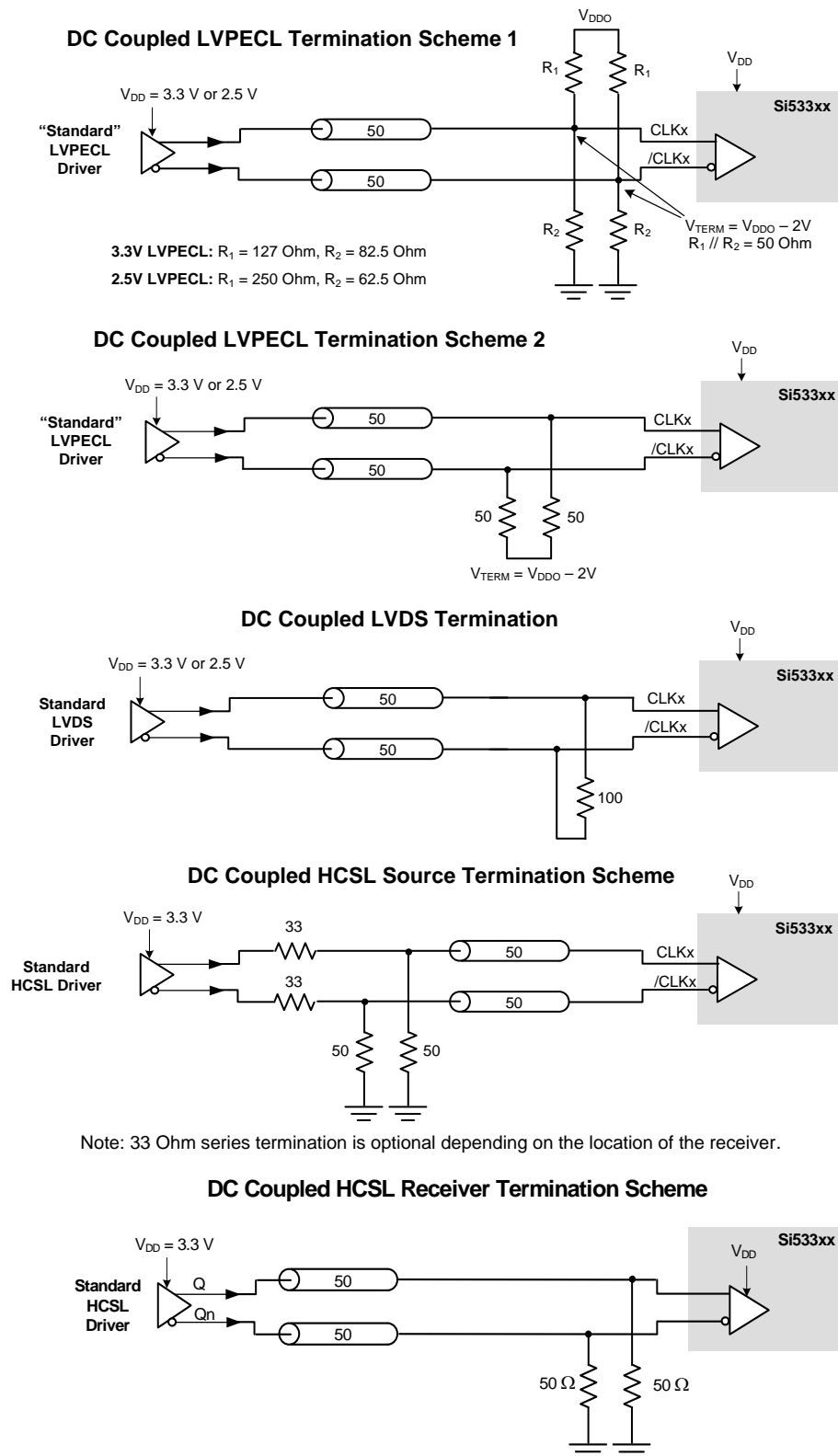
	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
2.5/3.3 V	Yes (3.3 V)	Yes (3.3 V)	Yes	No



**Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination**



**Figure 3. LVCMOS DC-Coupled Input Termination**

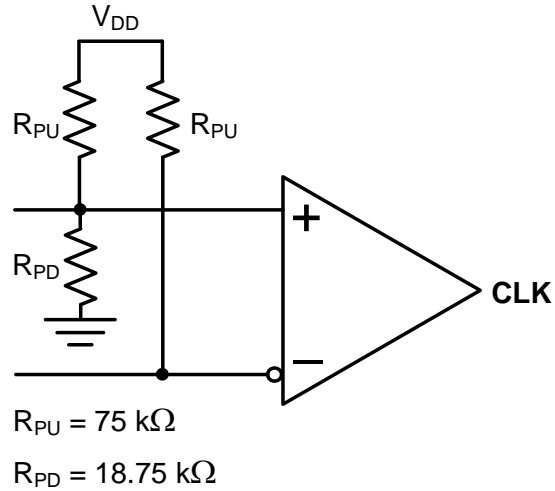


Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 4. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

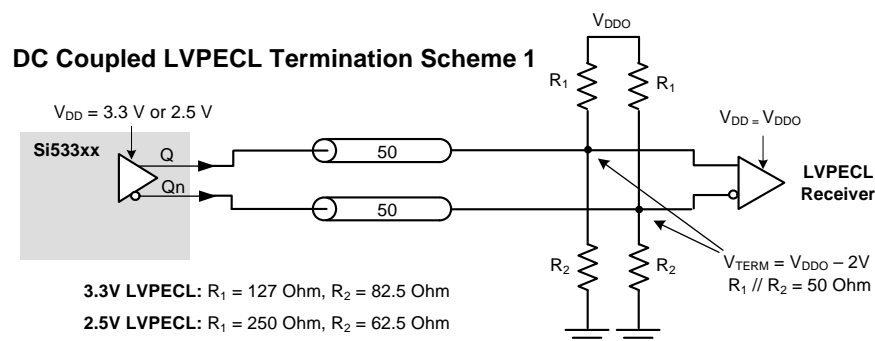
Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V<sub>DD</sub>. The inverting input is biased with a 75 kΩ pullup to V<sub>DD</sub>.



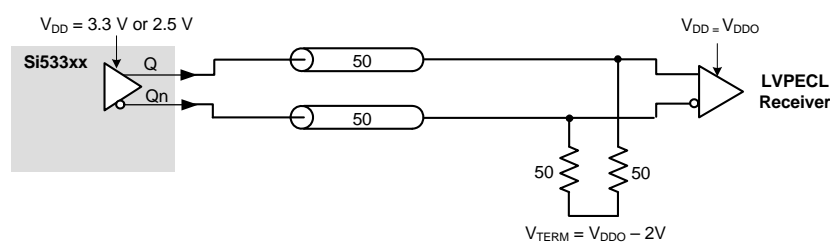
**Figure 5. Input Bias Resistors**

## 2.3. Output Clock Termination Options

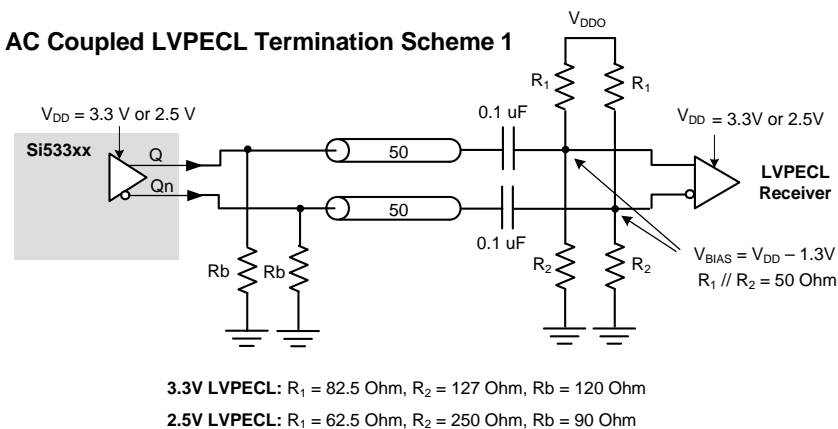
The recommended output clock termination options are shown below. Unused outputs can be left floating. Do not short unused outputs to ground.



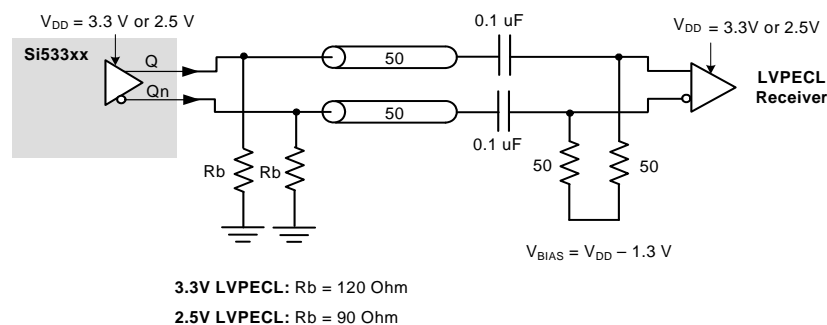
### DC Coupled LVPECL Termination Scheme 2



### AC Coupled LVPECL Termination Scheme 1

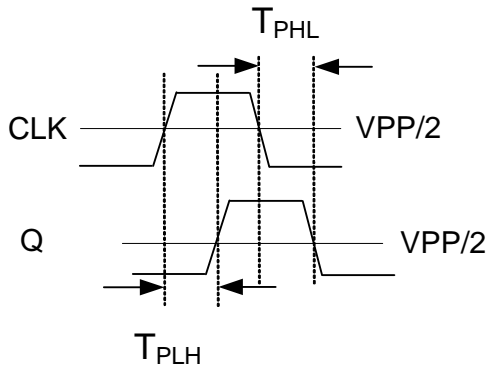


### AC Coupled LVPECL Termination Scheme 2

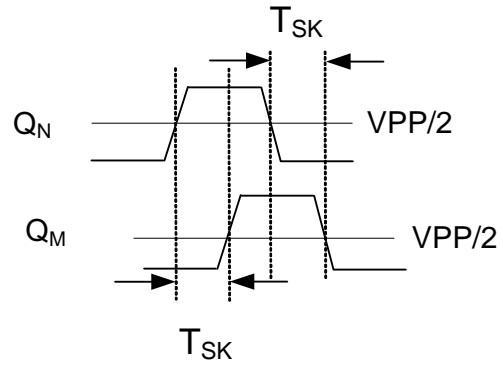


**Figure 6. LVPECL Output Termination**

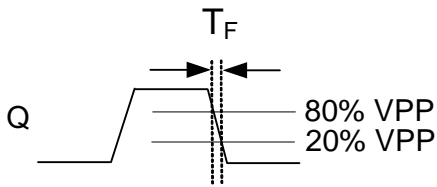
## 2.4. AC Timing Waveforms



Propagation Delay



Output-Output Skew



Rise/Fall Time

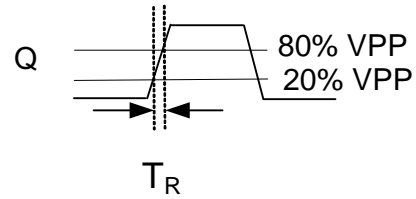


Figure 7. AC Waveforms

## 2.5. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

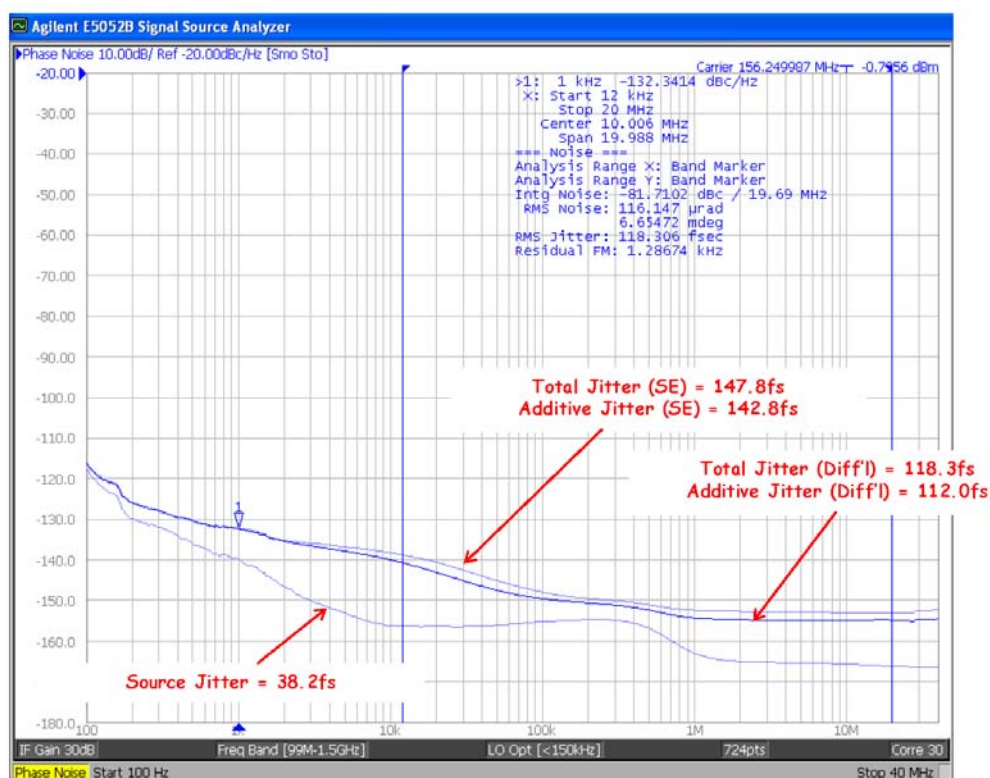
**Source Jitter:** Reference clock phase noise.

**Total Jitter (SE):** Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

**Total Jitter (Diff'l):** Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 8.

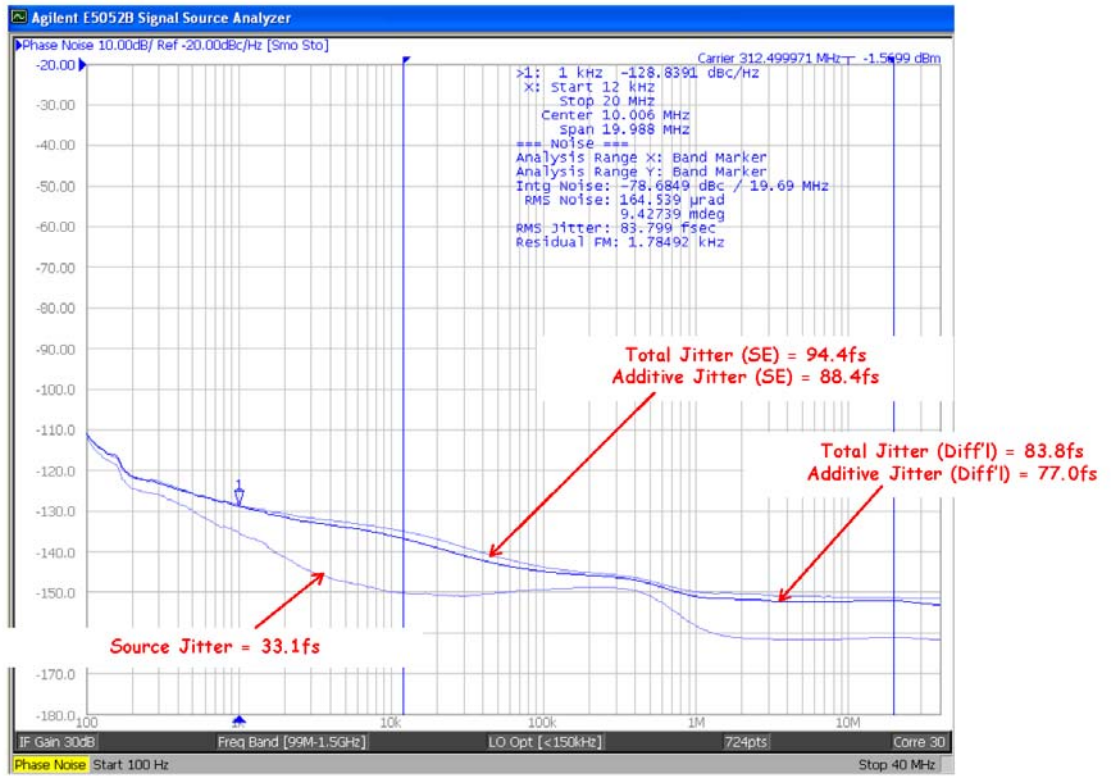
**Note:** To calculate the total RMS phase jitter when adding a buffer to your clock tree, use root-sum-square (RSS) addition.

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



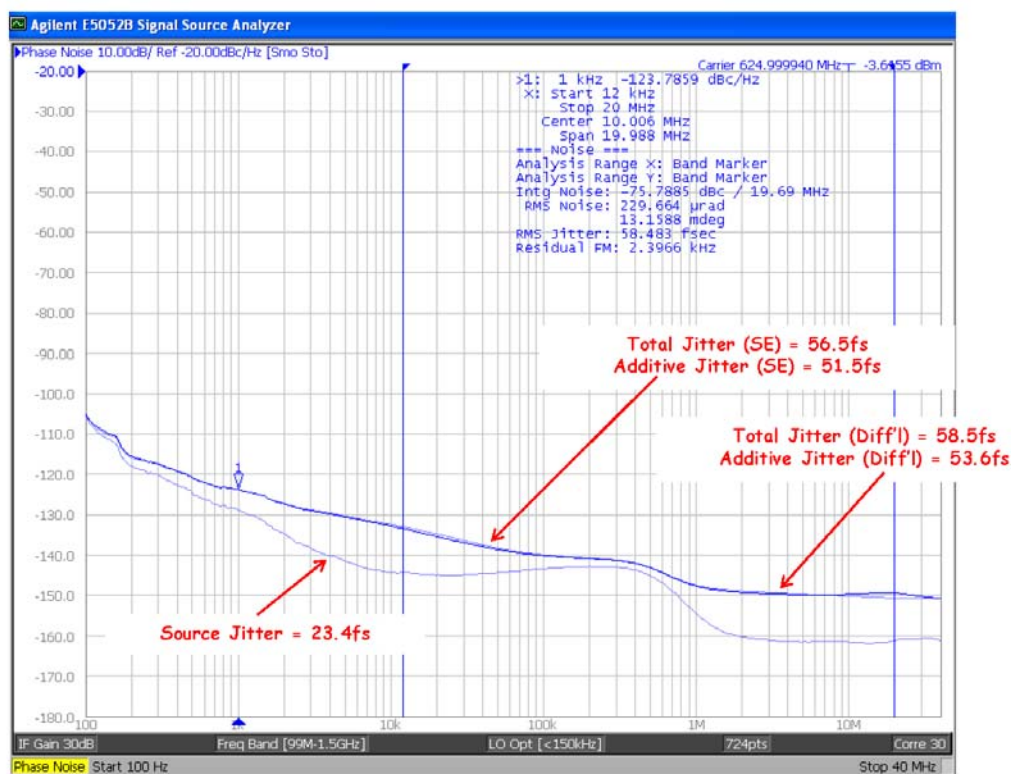
Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

Figure 8. Source, Additive, and Total Jitter (156.25 MHz)



Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.10	94.4	88.4	83.8	77.0

Figure 9. Source, Additive, and Total Jitter (312.5 MHz)



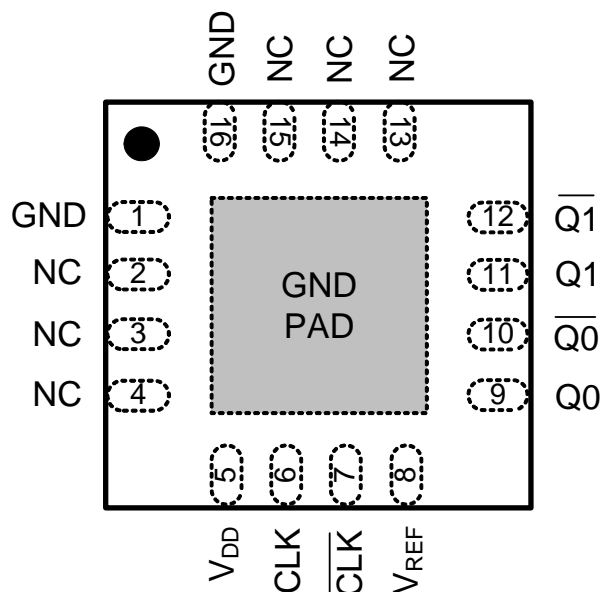
Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
625	1.0	23.4	56.5	51.5	58.5	53.6

Figure 10. Source, Additive, and Total Jitter (625 MHz)

## 2.6. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

## 3. Pin Description: 16-Pin QFN



**Table 12. Pin Descriptions**

Pin	Name	Description
1	GND	Ground.
2	NC	No connect.
3	NC	No connect.
4	NC	No connect.
5	VDD	<b>Core Voltage Supply.</b> Bypass with 1.0 $\mu$ F capacitor and place as close to the VDD pin as possible.
6	CLK	Input Clock
7	$\overline{\text{CLK}}$	<b>Input Clock (Complement).</b> When the CLK is driven by a single-ended LVPECL input, connect $\overline{\text{CLK}}$ to VREF. See Figure 1, “Differential Measurement Method Using a Balun,” on page 8.
8	VREF	<b>Input Clock Reference Voltage</b> When driven by a single-ended LVPECL clock input, connect the unused clock input to VREF and a 0.1 $\mu$ F cap to ground. When driven by a differential clock, do not connect the VREF pin.
9	Q0	Output Clock 0.
10	$\overline{\text{Q0}}$	Output Clock 0 (complement).
11	Q1	Output Clock 1.
12	$\overline{\text{Q1}}$	Output Clock 1 (complement).
13	NC	No connect.

**Table 12. Pin Descriptions (Continued)**

<b>Pin</b>	<b>Name</b>	<b>Description</b>
14	NC	No connect.
15	NC	No connect.
16	NC	No connect.
GND Pad	GND	Ground.

# Si53322

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## 4. Ordering Guide

Part Number	Package	Pb-Free, ROHS-6	Temperature
Si53322-B-GM	16-QFN	Yes	-40 to 85 °C
Si53301/4-EVB	NA	Yes	-40 to 85 °C

## 5. Package Outline

Figure 11 shows the package dimensions for the 3x3 mm 16-pin QFN package. Table 13 lists the values for the dimensions shown in the illustration.

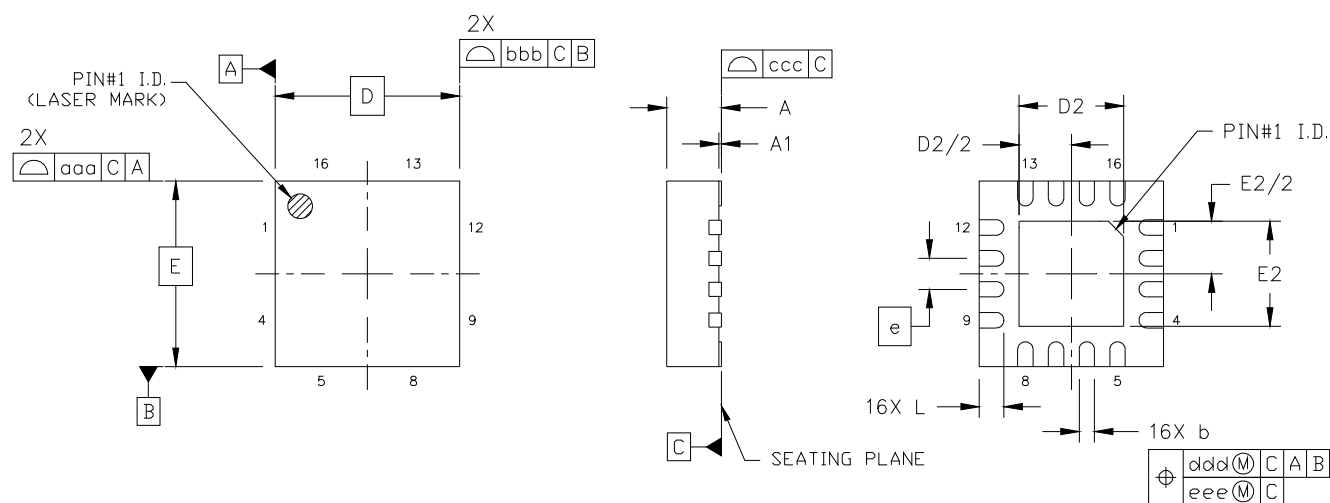


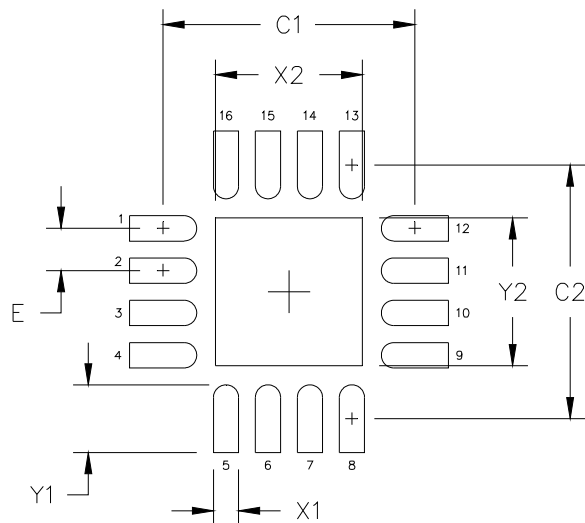
Figure 11. Si53322 3x3 mm 16-QFN Package Diagram

Table 13. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.00 BSC.		
D2	1.65	1.70	1.75
e	0.50 BSC.		
E	3.00 BSC.		
E2	1.65	1.70	1.75
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05
<b>Notes:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

## 6. PCB Land Pattern

Figure 12 shows the PCB land pattern dimensions for the 3x3 mm 16-pin QFN package. Table 14 lists the values for the dimensions shown in the illustration.



**Figure 12. Si53322 3x3 mm 16-QFN Package Land Pattern**

**Table 14. PCB Land Pattern Dimensions**

Dimension	mm
C1	3.00
C2	3.00
E	0.50
X1	0.30
Y1	0.80
X2	1.75
Y2	1.75

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

**Stencil Design**

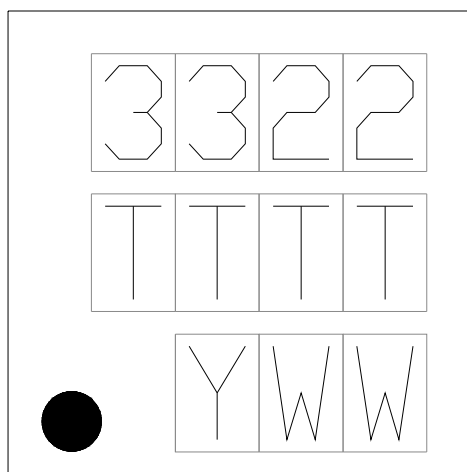
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2x2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Top Marking

### 7.1. Si53322 Top Marking



### 7.2. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	0.635 mm (25 mils) Right-Justified	
<b>Line 1 Marking:</b>	Product ID	<b>3322</b>
<b>Line 2 Marking:</b>	TTTT = Mfg Code	Manufacturing Code
<b>Line 3 Marking</b>	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YWW = Date Code	Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date.

## CONTACT INFORMATION

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Please visit the Silicon Labs Technical Support web page:  
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>  
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