

MC74VHC4066

Quad Analog Switch/ Multiplexer/Demultiplexer

High-Performance Silicon-Gate CMOS

The MC74VHC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

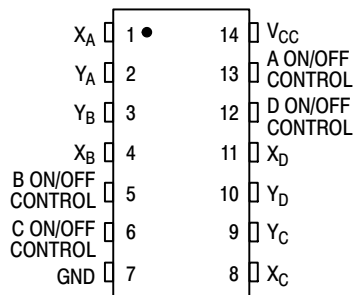
The VHC4066 is identical in pinout to the metal-gate CMOS MC14066 and the high-speed CMOS HC4066A. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the VHC4316.

Features

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

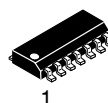
PIN ASSIGNMENT



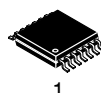
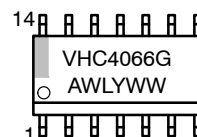
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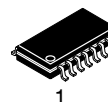
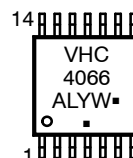
MARKING DIAGRAMS



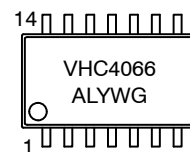
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOEIAJ-14
M SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC4066DR2G	SOIC-14	2500 / T&R
MC74VHC4066DTR2G	TSSOP-14	2500 / T&R
MC74VHC4066MG	SOEIAJ-14	50 / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

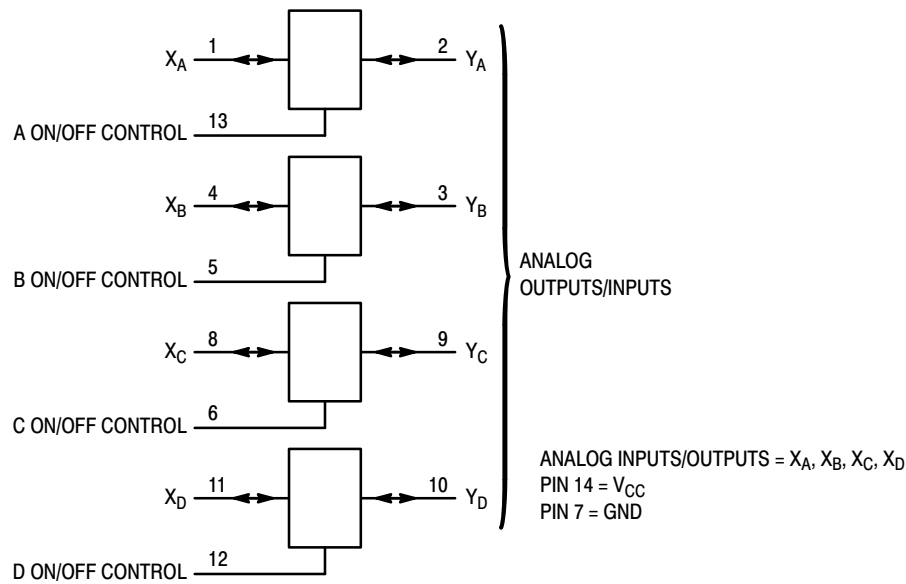


Figure 1. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	- 0.5 to + 14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{in}	Digital Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}^*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 14)			ns
	$V_{CC} = 2.0 \text{ V}$	0	1000	
	$V_{CC} = 3.0 \text{ V}$	0	600	
	$V_{CC} = 4.5 \text{ V}$	0	500	
	$V_{CC} = 9.0 \text{ V}$	0	400	
	$V_{CC} = 12.0 \text{ V}$	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

MC74VHC4066

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25 °C	≤ 85 °C	≤ 125 °C	
V _{IH}	Minimum High-Level Voltage ON/OFF Control Inputs	R _{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	V
V _{IL}	Maximum Low-Level Voltage ON/OFF Control Inputs	R _{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	V
I _{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V _{in} = V _{CC} or GND	12.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND V _{IO} = 0 V	6.0 12.0	2 4	20 40	40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25 °C	≤ 85 °C	≤ 125 °C	
R _{on}	Maximum “ON” Resistance	V _{in} = V _{IH} V _{IS} = V _{CC} to GND I _S ≤ 2.0 mA (Figures 2 through 7)	2.0† 3.0† 4.5 9.0 12.0	— — 120 70 70	— — 160 85 85	— — 200 100 100	Ω
		V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Endpoints) I _S ≤ 2.0 mA (Figures 2 through 7)	2.0 3.0 4.5 9.0 12.0	— — 70 50 30	— — 85 60 60	— — 100 80 80	
ΔR _{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V _{in} = V _{IH} V _{IS} = 1/2 (V _{CC} – GND) I _S ≤ 2.0 mA	2.0 4.5 9.0 12.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} V _{IO} = V _{CC} or GND Switch Off (Figure NO TAG)	12.0	0.1	0.5	1.0	μA
I _{on}	Maximum On-Channel Leakage Current, Any One Channel	V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Figure NO TAG)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 3 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

MC74VHC4066

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, ON/OFF Control Inputs: $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 18 and 13)	2.0 3.0 4.5 9.0 12.0	40 30 5 5 5	50 40 7 7 7	60 50 8 8 8	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 14 and 15)	2.0 3.0 4.5 9.0 12.0	80 60 20 20 20	90 70 25 25 25	110 80 35 35 35	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 14 and 15)	2.0 3.0 4.5 9.0 12.0	80 45 20 20 20	90 50 25 25 25	100 60 30 30 30	ns
C	Maximum Capacitance ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND	—	35	35	35	
	Analog I/O Feedthrough	—	1.0	1.0	1.0	
C _{PD}	Power Dissipation Capacitance (Per Switch) (Figure 17)*	Typical @ 25°C, V _{CC} = 5.0 V				pF
		15				

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74VHC4066

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V _{CC} V	Limit* 25°C 74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure NO TAG)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads - 3 dB R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure NO TAG)	f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	- 50 - 50 - 50 - 40 - 40 - 40	dB
—	Feedthrough Noise, Control to Switch (Figure NO TAG)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mV _{PP}
—	Crosstalk Between Any Two Switches (Figure 16)	f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	- 70 - 70 - 70 - 80 - 80 - 80	dB
THD	Total Harmonic Distortion (Figure 20)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 V _{PP} sine wave V _{IS} = 8.0 V _{PP} sine wave V _{IS} = 11.0 V _{PP} sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

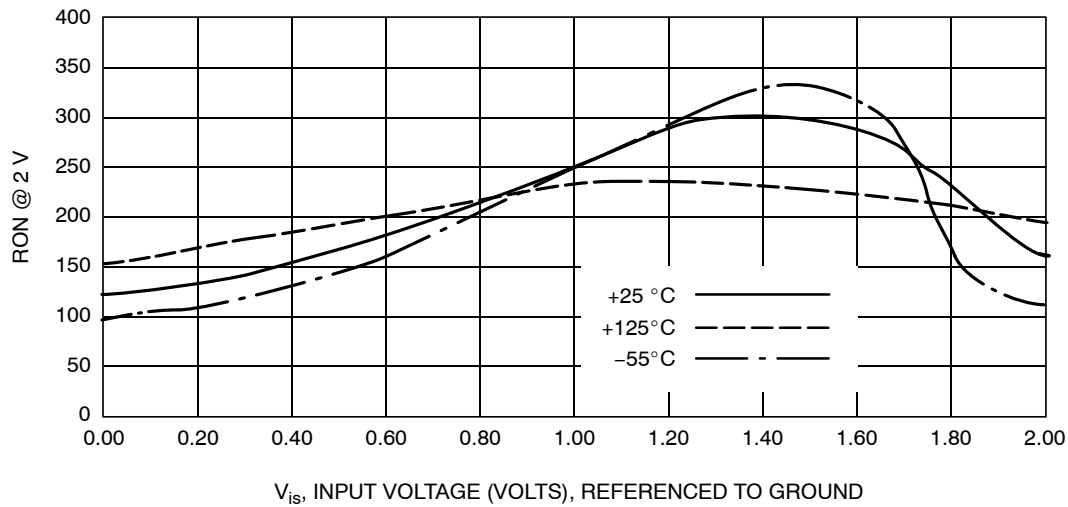


Figure 2. Typical On Resistance, V_{CC} = 2.0 V

MC74VHC4066

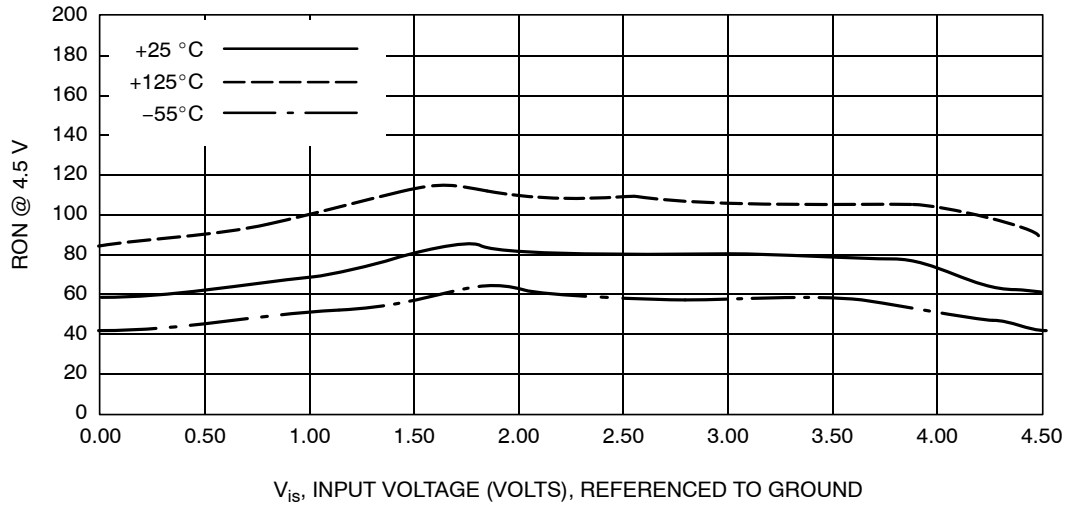


Figure 3. Typical On Resistance, $V_{CC} = 4.5$ V

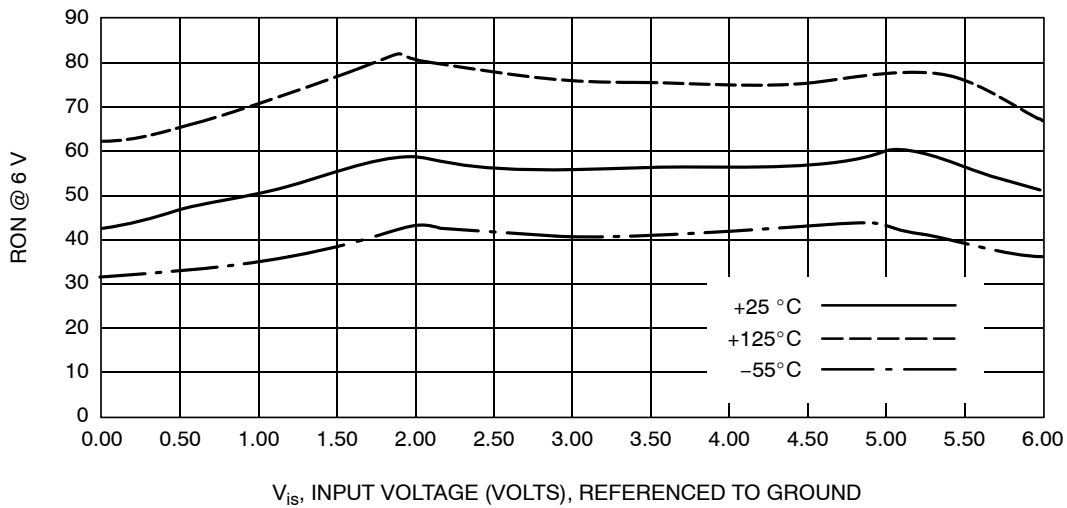


Figure 4. Typical On Resistance, $V_{CC} = 6.0$ V

MC74VHC4066

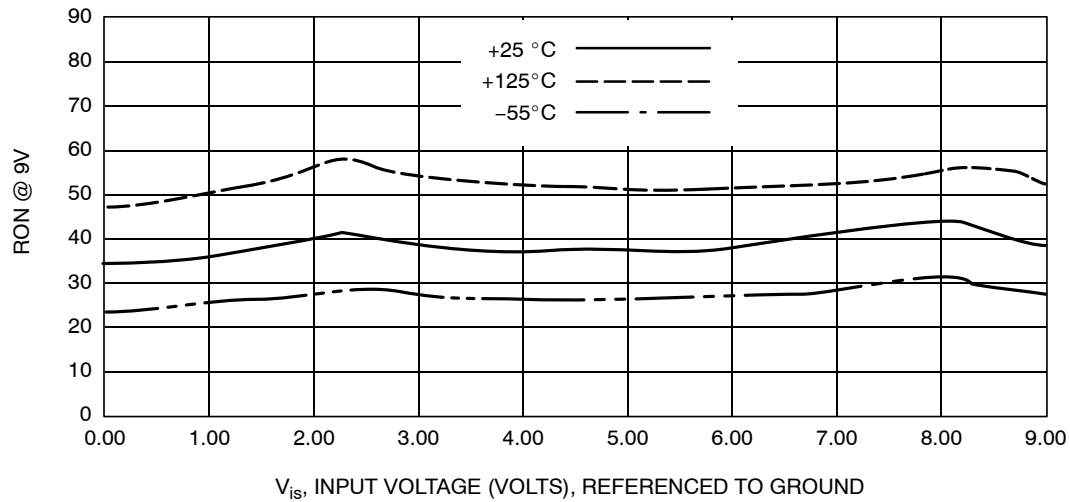


Figure 5. Typical On Resistance, $V_{CC} = 9.0\text{ V}$

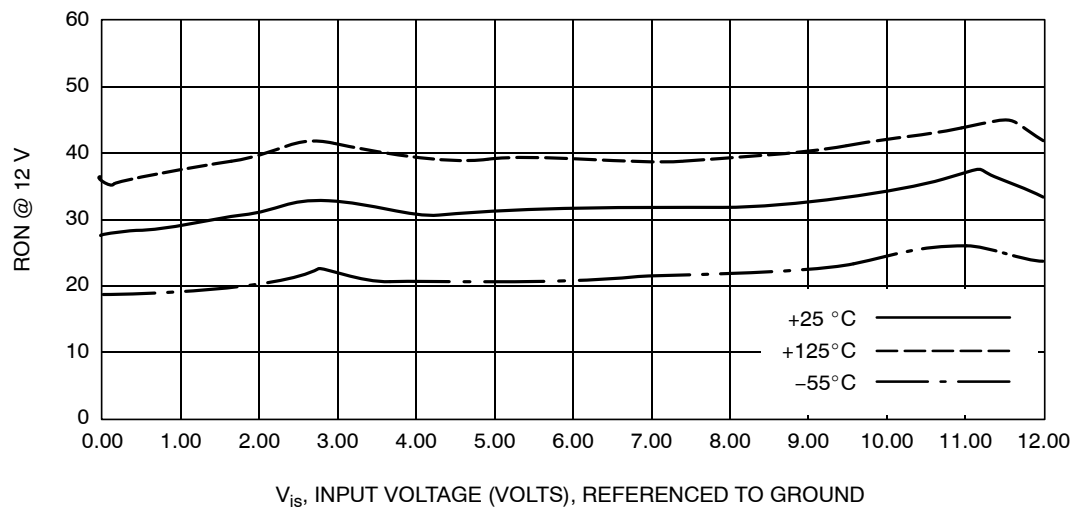


Figure 6. Typical On Resistance, $V_{CC} = 12\text{ V}$

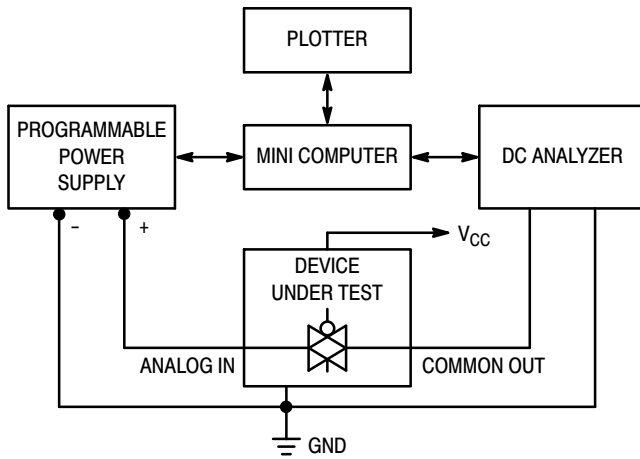


Figure 7. On Resistance Test Set-Up

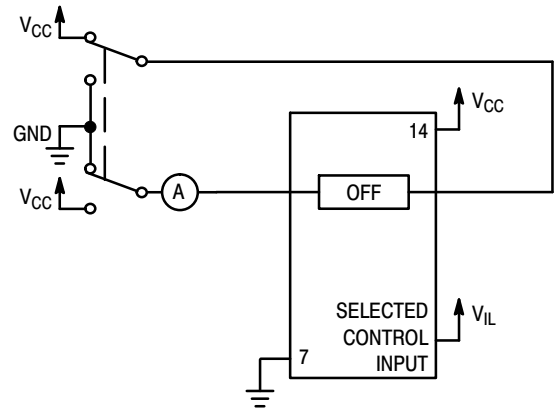


Figure 8. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

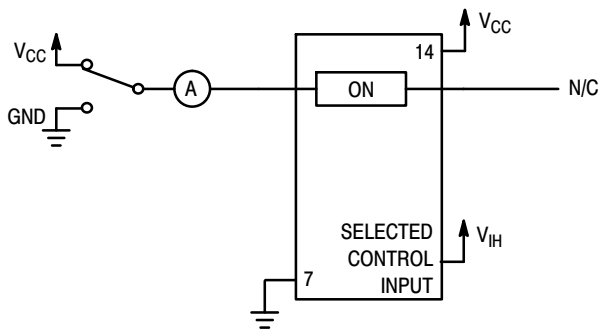
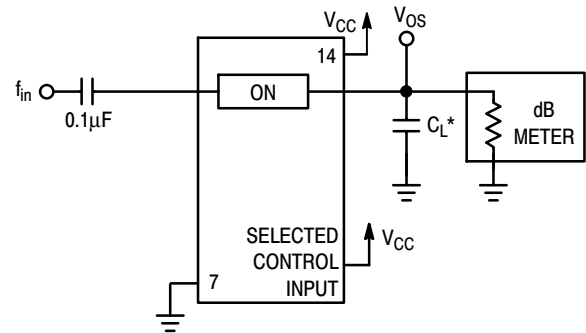
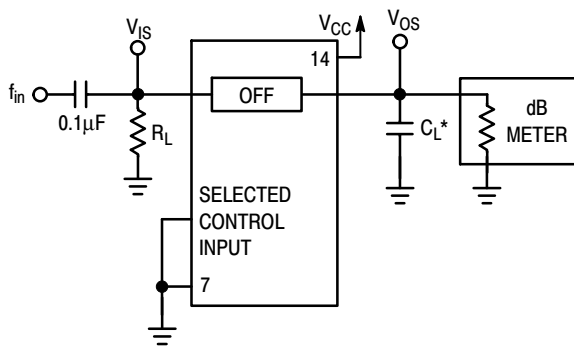


Figure 9. Maximum On Channel Leakage Current, Test Set-Up



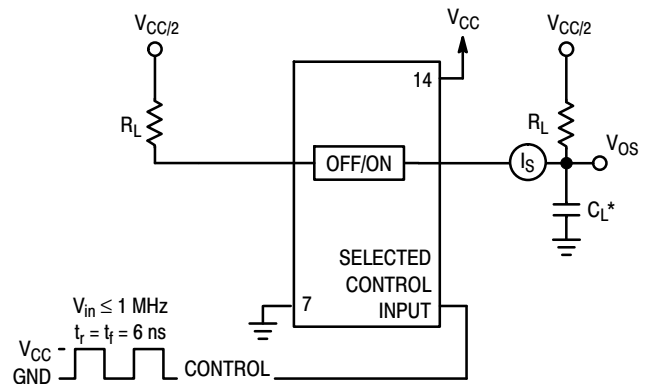
*Includes all probe and jig capacitance.

Figure 10. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 11. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

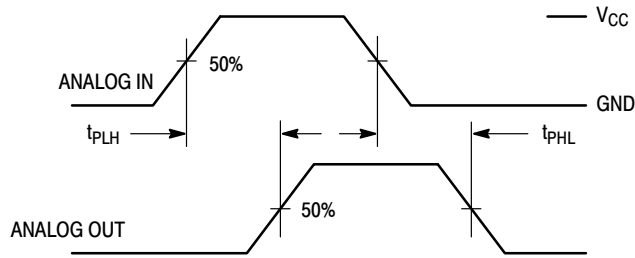
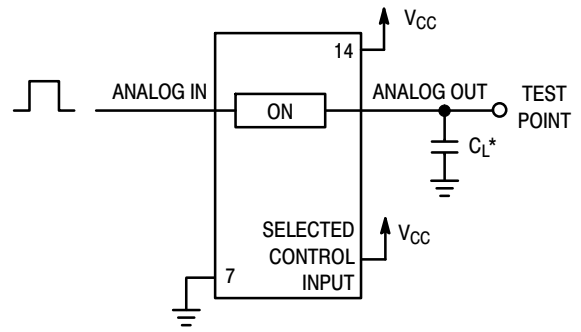


Figure 18. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 13. Propagation Delay Test Set-Up

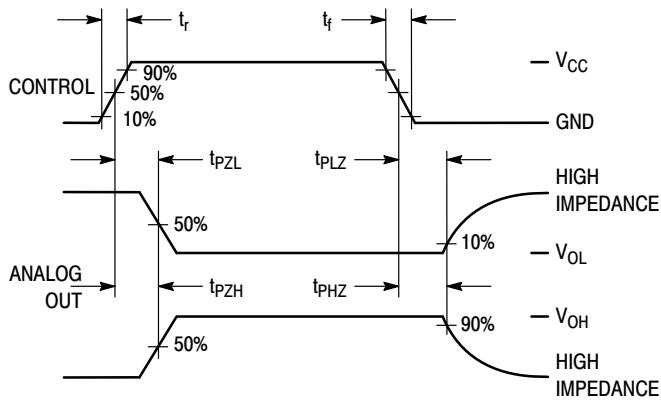
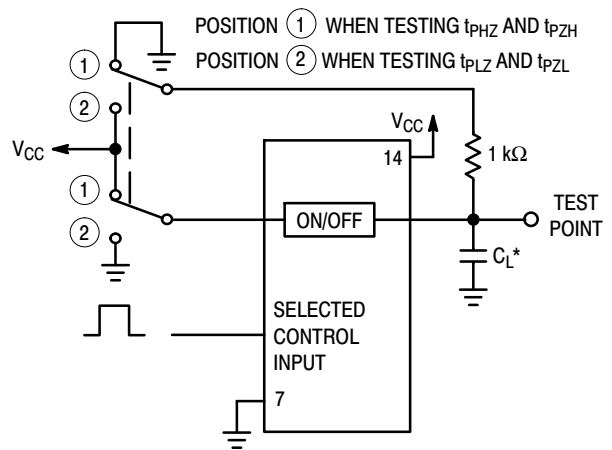
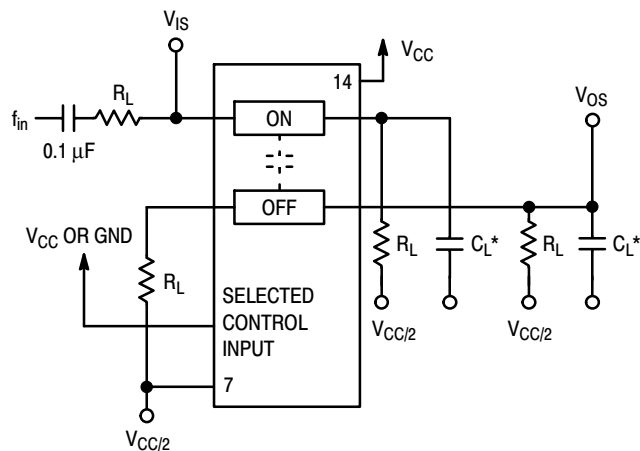


Figure 14. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 15. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 16. Crosstalk Between Any Two Switches, Test Set-Up

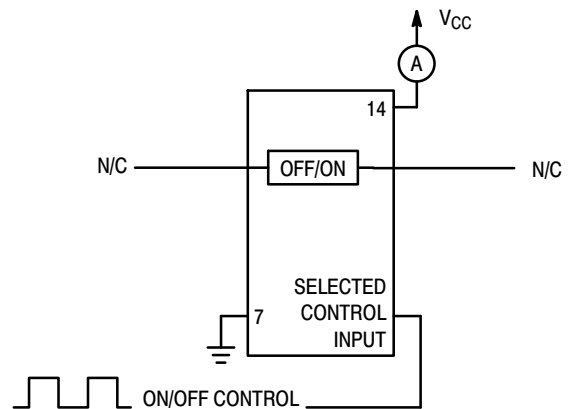
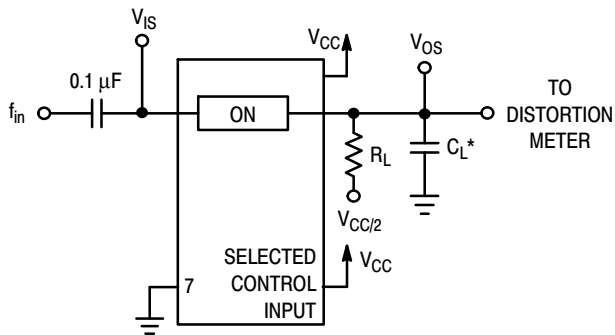


Figure 17. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 20. Total Harmonic Distortion, Test Set-Up

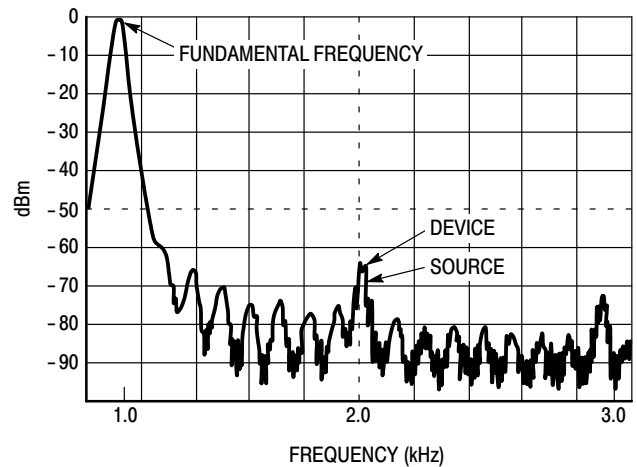


Figure 19. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below GND. In

the example below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 21, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure 22. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the D_x diodes with Mosorbs (high current surge protectors). Mosorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

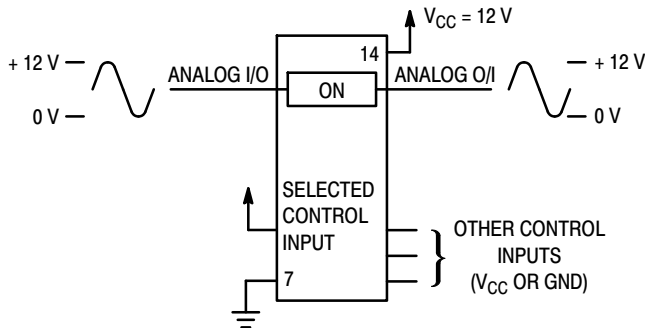


Figure 21. 12 V Application

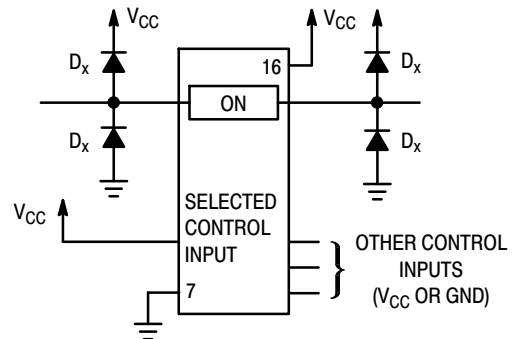


Figure 22. Transient Suppressor Application

MC74VHC4066

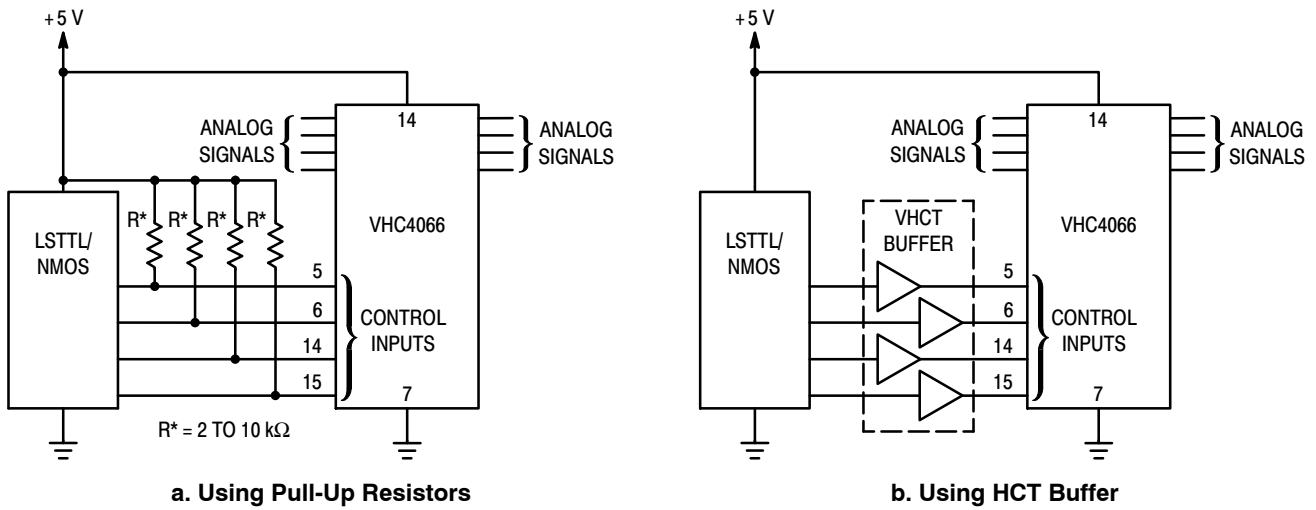


Figure 23. LSTTL/NMOS to HCMOS Interface

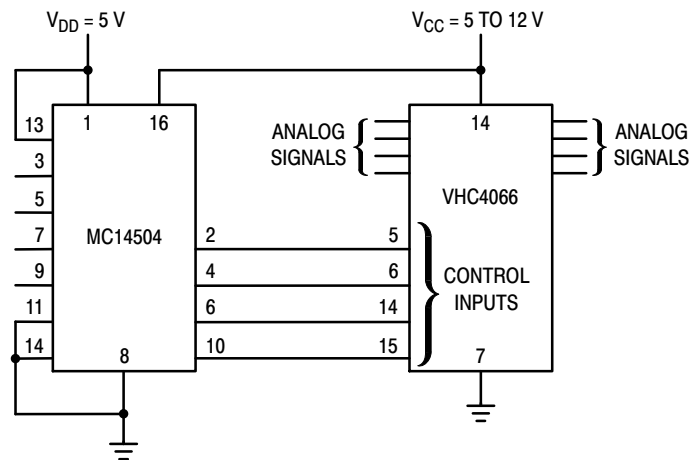


Figure 24. TTL/NMOS-to-CMOS Level Converter Analog Signal
Peak-to-Peak Greater than 5 V
(Also see VHC4316)

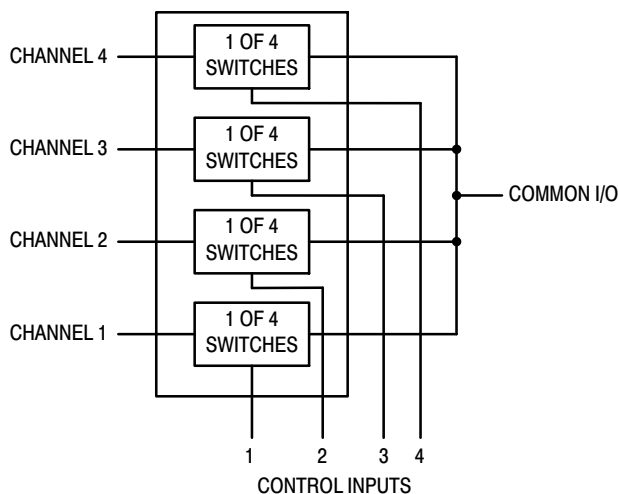


Figure 25. 4-Input Multiplexer

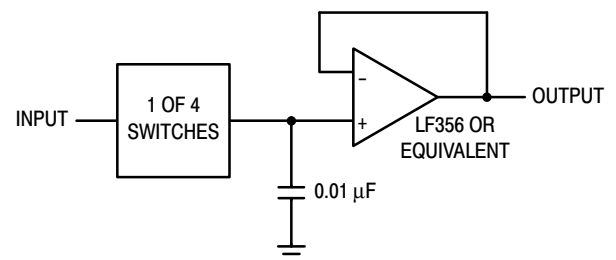


Figure 26. Sample/Hold Amplifier

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

Technical drawing of a 14-pin D-sub connector. The drawing includes three views: a top view, a side view, and a detail view of the contact area.

Top View Dimensions:

- Overall width: A
- Pin pitch (center-to-center): $0.25 (0.010) \text{ M}$
- Pin diameter: $B \text{ M}$
- Pin height: 14
- Pin spacing (between groups): 8
- Pin diameter (bottom): 1
- Pin spacing (bottom): 7
- Pin diameter (bottom): G

Side View Dimensions:

- Overall height: P
- Pin height: 7 PL
- Pin diameter: $0.25 (0.010) \text{ M}$
- Pin diameter: $B \text{ M}$

Detail View Dimensions:

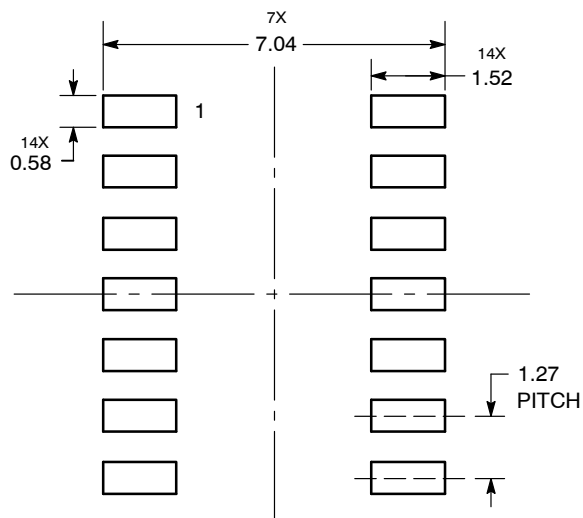
- Radius: $R \times 45^\circ$
- Pin diameter: F
- Pin diameter: J
- Pin diameter: M

Other Dimensions:

- Seating Plane: T
- Pin diameter: D
- Pin diameter: 14 PL
- Pin diameter: K
- Pin diameter: C

Feature Callouts:

- $-A-$
- $-B-$
- $-T-$ SEATING PLANE
- D
- 14 PL
- K
- C
- $R \times 45^\circ$
- F
- J
- M



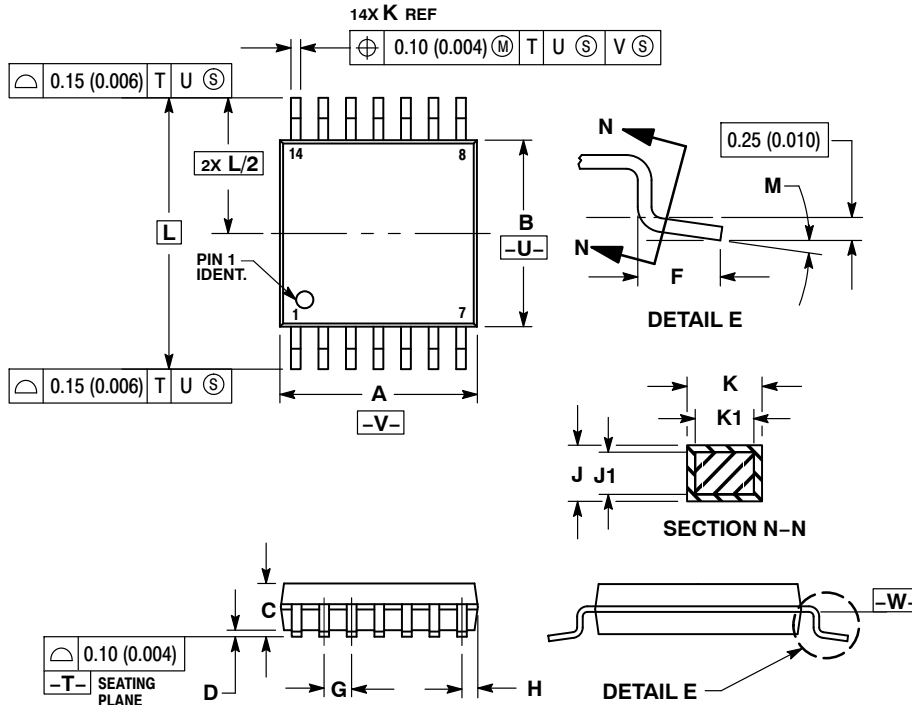
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC4066

PACKAGE DIMENSIONS

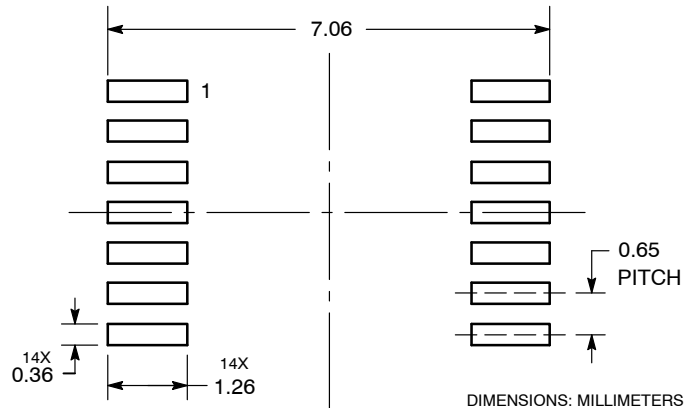
TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT*

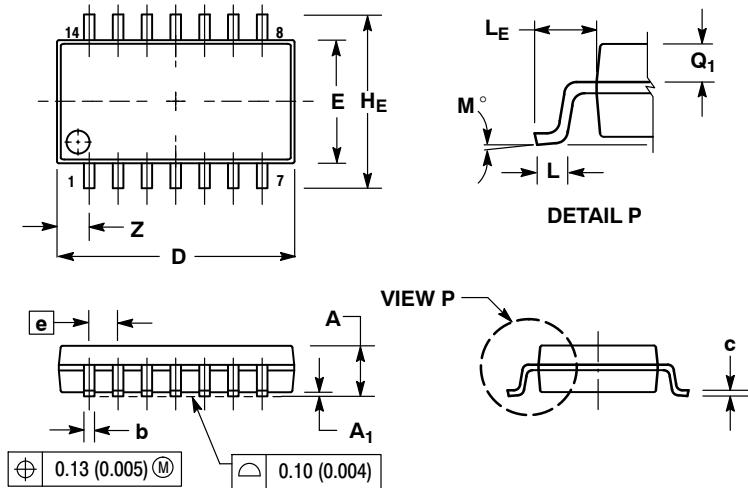


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC4066

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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