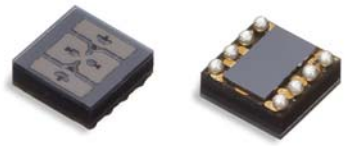
Data Sheet



CMA3000-D01 3-AXIS ULTRA LOW POWER ACCELEROMETER WITH DIGITAL SPI AND I²C INTERFACE

Features

- 1.7 V – 3.6 V supply voltage
- SPI and I²C digital interface
- User selectable
  - ±2 g and ±8 g measurement ranges
  - sample rate & frequency response
- Ultra low current consumption
  - ≤ 70 uA with 100/400 Hz sample rate
  - ≤ 11 uA with 40/10Hz sample rate
- Interrupt signal triggered by data ready, motion and free fall
- Size 2x2x0.95 mm3
- Proven capacitive 3D-MEMS technology
- High shock durability
- RoHS compliant / lead free soldering

Applications

CMA3000-D01 is targeted to battery operated devices. Typical applications are but not limited

- Gaming input devices
- Computer peripherals
- Free fall detection
- Activity monitoring

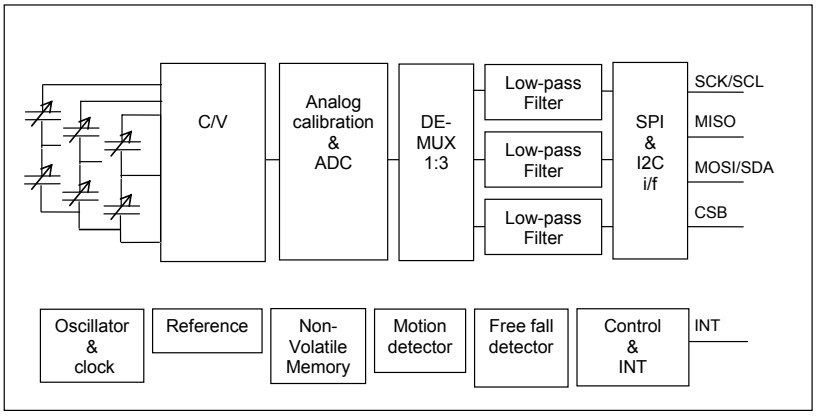


Figure 1 CMA3000-D01 Block Diagram

Performance Characteristics [1)]

Parameter	Condition	Typical supply range 1.7 – 2.7 V			Extended supply range 2.7 – 3.6 V			Units
		Min	Typ [2)]	Max	Min	Typ [2)]	Max	
Vdd		1.7	2.5	2.7	-	3.3	-	V
Digital I/O Vdd	Vdd ≥ Digital I/O Vdd	1.7	1.8 / 2.5	2.7	-	3.3	-	V
Operating temperature **		-40	-	85	-40	-	85	°C
Current consumption *	ODR=400 Hz ODR=100 Hz ODR=40 Hz ODR=10 Hz Power down	- - - - -	70 50 11 7 4	90 - - - 9	- - - - -	70 50 14 9 3	- - - - -	µA
Acceleration range *	G_RANGE bit 0 G_RANGE bit 1	-8 -2	- -	8 2	- -	±8 ±2	-	G
Offset calibration error * [3)]	G_RANGE bit 1	-100	±25	+100	-	±100	-	mg
Offset temperature error ** [4)]	-40 ... +85 °C X and Z axis Y axis		 ±1 ±2.5		 - -	 ±1 ±2.5	 - -	mg/°C
Sensitivity * [5)]	Full scale = 2 g Full scale = 8 g	- -	56 14	- -	- -	56 14	- -	Count/g
Sensitivity calibration error *		-10	-	+10	-	±10	-	%
Sensitivity temperature error ** [6)]	-40 ... +85 °C	-	±0.02		-	±0.02	-	%/°C
Non-Linearity ** [7)]		-	1.5	3	-	1.5	-	% FS
Cross-Axis sensitivity ** [8)]	G_RANGE bit 1	-	1	-	-	1	-	%
Output Data Rate, ODR **	MODE bits x10 MODE bits x01 MODE bits 011 MODE bits 100		400 100 40 10		-	400 100 40 10	-	Hz
Bandwidth** [9)]			ODR/5			ODR/5	-	Hz
Noise ** [10)]	Full scale=2 g, ODR=100 Hz Full scale=8 g, ODR=400 Hz	- -	13 25		- -	13 25	- -	mg RMS
Turn on time ** [11)]	ODR=400 Hz ODR≤100 Hz	- -	0.01 2.5/ODR		- -	0.01 2.5/ODR	- -	s
I^2C clock rate **		-	-	400	-	-	400	kHz
SPI clock rate **				500			500	kHz

* 100% tested in production

** Qualified during product validation

1) The product is factory calibrated at 2.5 V in room temperature.

2) Typical values are not guaranteed.

3) Z-axis +1g position. Soldering process can cause offset shift which is typically less than 150 mg. Please see TN68_CMA3000_Assembly_Instructions for further details.

4) Offset temperature error = {Count(0g)-Offset} / Sensitivity [g]. Sensitivity = Calibrated sensitivity. Offset= Calibrated offset.

5) Sensitivity = {Count(+1g) - Count(-1g)}/2 [Count/g].

6) Sensitivity temperature error = {[Count(+1g)-Count(-1g)]/2 - Sensitivity} / Sensitivity x 100% [%]. Sensitivity = Calibrated sensitivity.

7) Best fit straight line.

8) The cross-axis sensitivity determines how much acceleration, perpendicular to the measuring axis, couples to the output. The total cross-axis sensitivity is the geometric sum of the sensitivities of the two axes which are perpendicular to the measuring axis. The angular alignment error between X, Y and Z axis is included into the cross axis sensitivity.

9) Frequency responses with 1st order roll off according to Figure 3.

10) Average noise/axis over the measurement bandwidth defined as $\sqrt{\frac{1}{3}(n_x{}^2+n_y{}^2+n_z{}^2)}$, where nx, ny and nz are the measured signal's standard deviation due to noise in x, y and z directions.

11) Settling error less than 1% of FS.

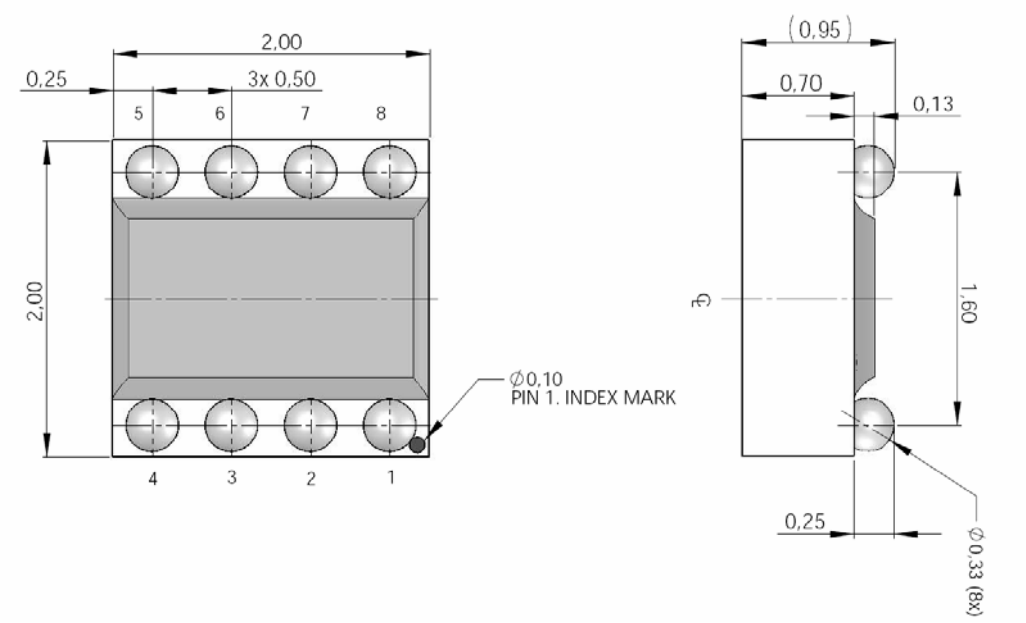


Figure 2 Package dimensions in mm with ±50 µm tolerance.

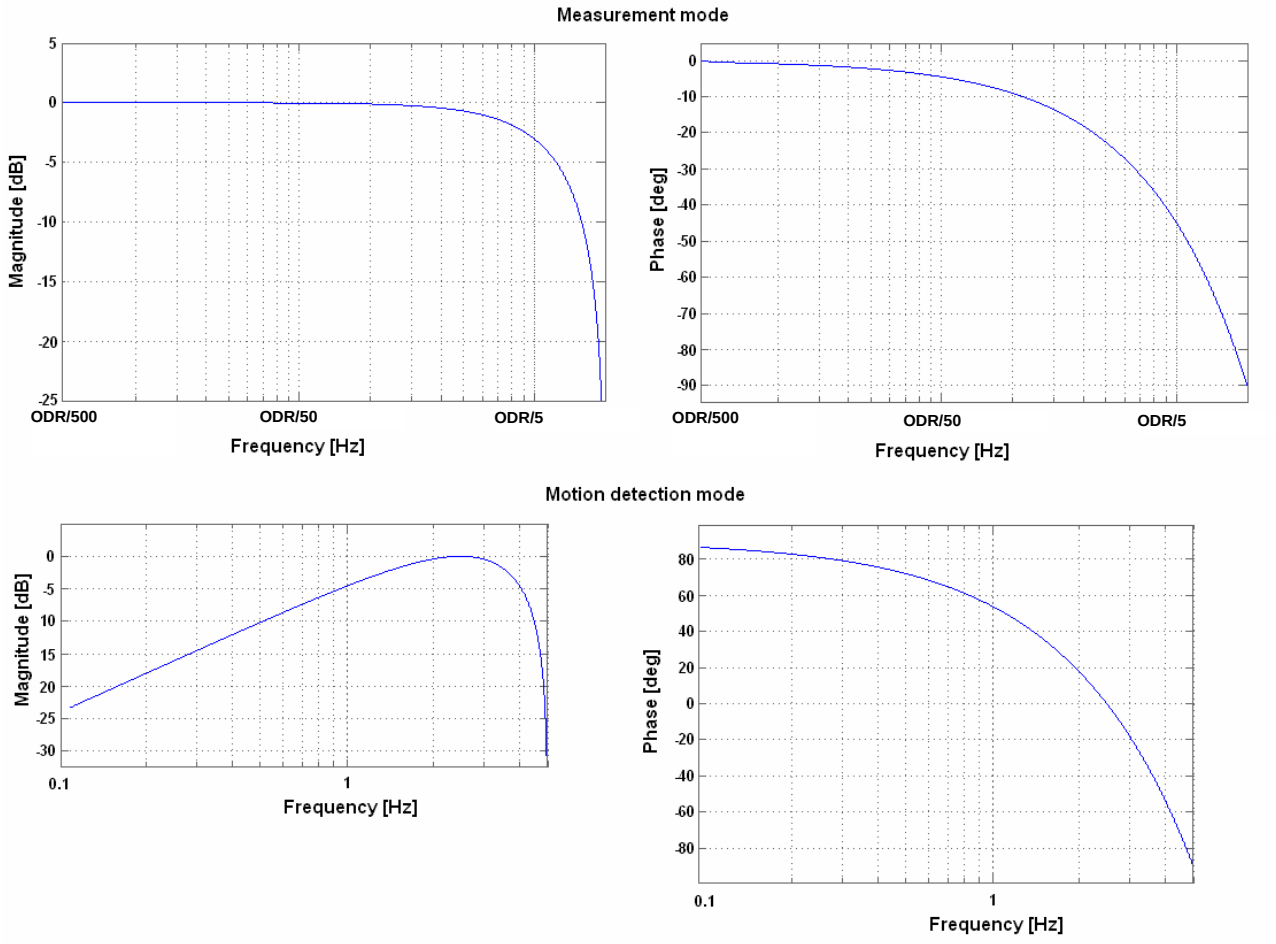


Figure 3 Typical Frequency responses of CMA3000-D01.

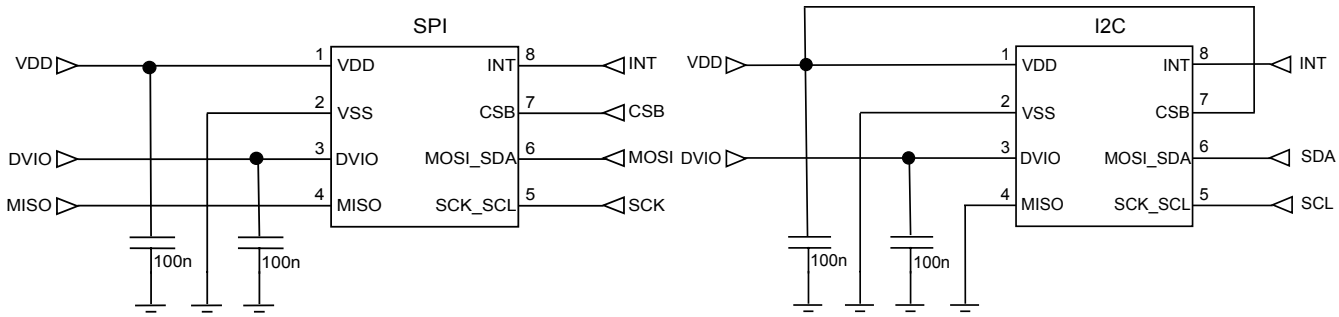


Figure 4 Application schematics for SPI and I²C bus

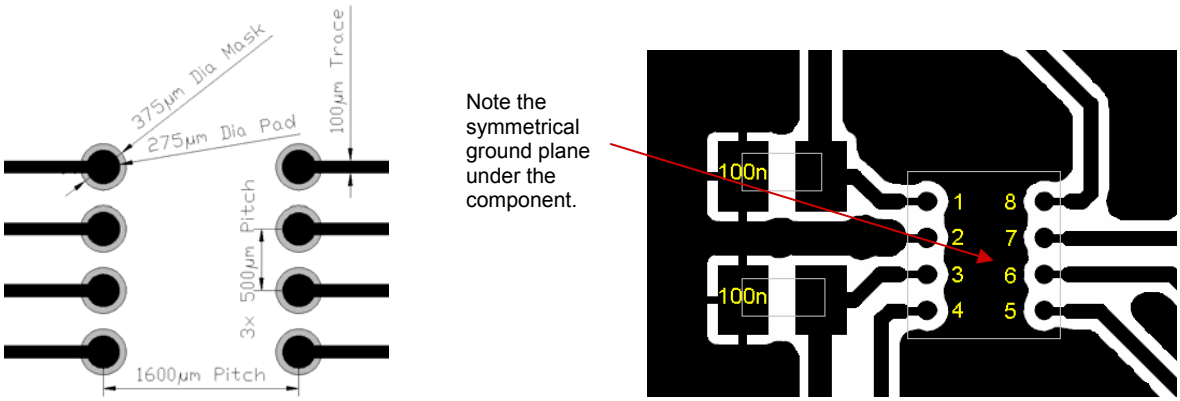


Figure 5 Recommended layout pattern (not actual size, for reference only)

Table 1 Pin descriptions

Pin #	Name	Function
1	VDD	Supply voltage
2	VSS	Ground
3	DVIO	I/O Supply
4	MISO	SPI Serial Data Output (MISO)
5	SCK_SCL	SPI Serial Clock (SCK) / I²C Serial Clock (SCL)
6	MOSI_SDA	SPI Serial Data Input (MOSI) / I²C Serial Data (SDA)
7	CSB	Chip select / I²C enable
8	INT	Interrupt

Document Change Control

Rev.	Date	Change Description
0.1	02-May-07	1st version
…	…	…
0.7	14-Feb-08	Performance characteristics update
0.8	21-Apr-08	Target values for offset and sensitivity, non-linearity and cross axis added.
0.9	01-Jul-08	Figure 1 & Table 1 pin names corrected, Figure 2,3 & 5 updated
0.10	28-Aug-08	Current consumption, sensitivity and sensitivity temperature error, non-linearity, cross axis sensitivity and noise updated.
0.11	01-Sep-08	8g range noise level corrected.
0.12	10-Dec-08	Performance characteristics and notes updated. Figure 2 updated.
0.13	29-Dec-08	Version for launch
0.14	12-Jun-09	Performance characteristics update
A.01	26-Oct-09	Release A