

Structure Silicon Monolithic Integrated Circuit

Product Name 6-Parallel white-LED Driver for mobile phone

Type **BD1606MVV**

Features Automatically transition to each mode (x1,x1.5,x2) charge pump type DC/DC converter
6 channels LED Driver (0.5mA-32mA, 64 steps)

○ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Condition
Power supply voltage	VMAX	7.0	V	
Power Dissipation	Pd	780 (*1)	mW	
Operating Temperature Range	Topr	-30 ~ +85	°C	
Storage Temperature Range	Tstg	-55 ~ +150	°C	

(*1) This value is the measurement value that was mounted on the PCB by ROHM.

(74.2mm × 74.2mm × 1.6mm glass epoxy Board)

Temperature delecting: 6.2mW/deg from Ta>25deg

○ Operating conditions (Ta=-30°C~+85°C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	2.7	3.6	5.5	V	

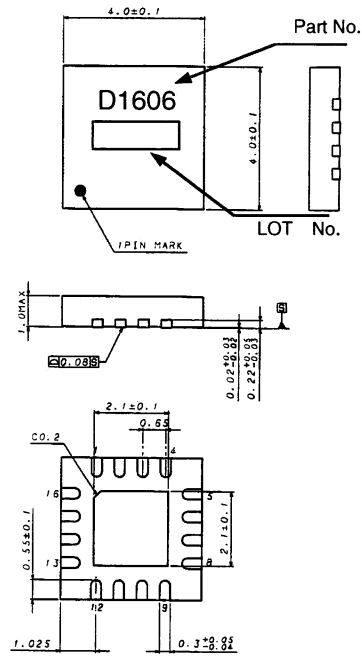
This product isn't designed to protect itself against radioactive rays.

○ Electrical Characteristics

(Unless otherwise noted, Ta = +25°C, Vin=3.6V)

Parameter	Symbol	Rating			Units	Condition
		Min.	Typ.	Max.		
Overall						
Input voltage range	V _{in}	2.7	3.6	5.5	V	
Quiescent Current	I _q	-	0	7	μA	EN=0V
Current Consumption 1	I _{DD1}	-	1.0	2.6	mA	x1.0 mode, Except LED current
Current Consumption 2	I _{DD2}	-	2.0	4.0	mA	x2.0 mode, Except LED current
Charge Pump						
Oscillator frequency	f _{OSC}	0.8	1.0	1.2	MHz	Add=0x03, D6='0'
Current Source						
LED current accuracy	I _{LED-ERR}	-	-	±6.5	%	When LED current 16.5mA setting and LED pin voltage 1.0V
LED current matching	I _{LED10-LED}	-	-	±3.75	%	When LED current 16.5mA setting and LED pin voltage 1.0V
LED control voltage	V _{LED}	-	0.20	0.25	V	Minimum voltage at ILEDA1~ILEDC2 pins
Logic Block (DC Characteristics)						
Low threshold voltage	V _{IL1}	-	-	0.4	V	EN pin
	V _{IL2}	-	-	0.3	V	SCL, SDA pins when EN=1.8V
High threshold voltage	V _{IH1}	1.6	-	V _{in}	V	EN pin
	V _{IH2}	1.5	-	V _{IH1}	V	SCL, SDA pins when EN=1.8V
High Input current	I _{IH}	-	-	10	μA	EN, SCL, SDA = V _{in}
Low Input current	I _{IL}	-10	-	-	μA	EN, SCL, SDA = GND
SDA Output Low Level	V _{OL}	-	-	0.4	V	Load current 3mA

External dimensions

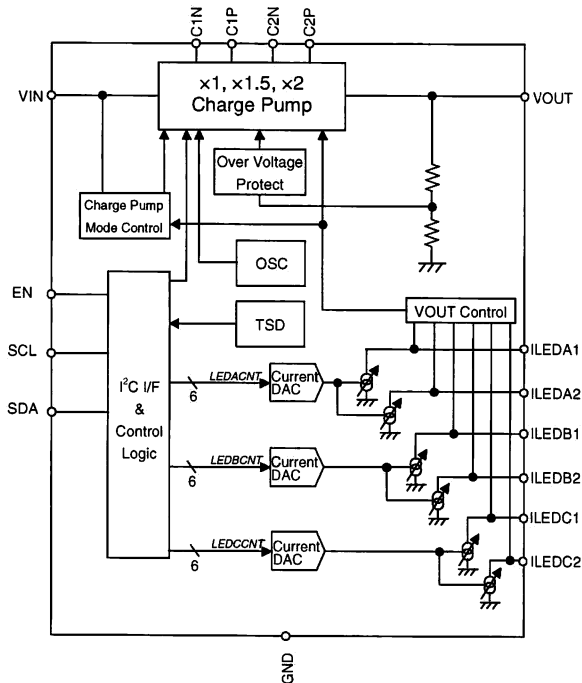


SQFN016V4040 (16PIN) (Unit: mm)

Terminals

PIN	Pin Name	PIN	Pin Name
1	ILEDA1	9	C2N
2	SDA	10	C2P
3	SCL	11	GND
4	EN	12	ILEDC2
5	VOUT	13	ILEDC1
6	VIN	14	ILEDB2
7	C1N	15	ILEDB1
8	C1P	16	ILEDA2

Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) Other cautions on use

Please consult supplementary documents such as technical notebook, function manual and application design guide of this LSI

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