



## Quad 2-input NAND gate

74LVC00

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

## DESCRIPTION

The 74LVC00 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC00 provides the 2-input NAND function.

## FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level

L = LOW voltage level

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 50 \text{ pF}$ $V_{CC} = 3.3 \text{ V}$	3.3	ns
$C_i$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	50	pF

## Notes to the quick reference data

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_i = \text{GND to } V_{CC}$

## ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC00D	14	SO	plastic	SO14/SOT108A
74LVC00DB	14	SSOP	plastic	SSOP14/SOT337
74LVC00PW	14	TSSOP	plastic	TSSOP14/SOT402

## PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	$V_{CC}$	positive supply voltage

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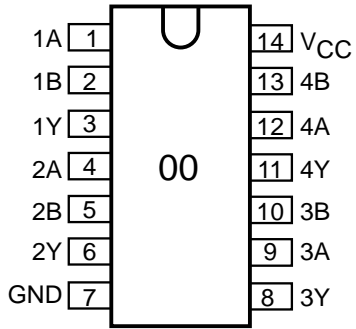


Fig.1 Pin configuration.

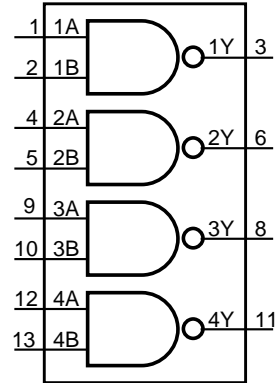


Fig.2 Logic symbol.

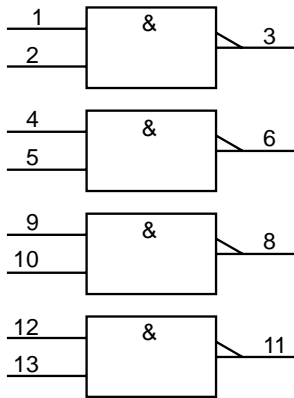


Fig.3 IEC Logic symbol.

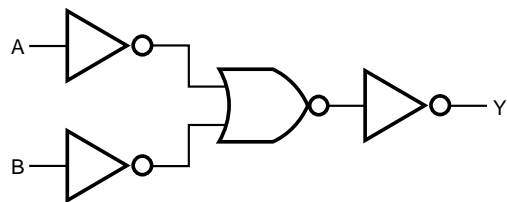


Fig.4 Logic diagram (one gate).

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## FAMILY DESCRIPTION

The LVC family comprises very fast low-power logic ICs fabricated in a sub-micron CMOS process. LVC ICs with 3.3 V  $\pm$ 0.3 V supply operate at the same speed as FAST bipolar logic and consumes only

a fraction of the power. The LVC family functions with supply voltages down to 2.7 V. The reduction from the conventional 5.0 V to 3.3 V reduces the output swing leading to a much lower

dynamic power dissipation. Pin and function compatibility with FAST ensures an easy transfer of existing systems into new 3.3 V systems.

## RECOMMENDED OPERATING CONDITIONS FOR THE LVC FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage (for max. speed performance)	2.7	3.6	V	
$V_{CC}$	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
$V_I$	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	$V_{CC}$	V	
$V_O$	DC output voltage range	0	$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range in free air	-40	+85	°C	see DC and AC characteristics per device
$t_r, t_f$	input rise and fall times	0	20 10	ns/V	$V_{CC} = 1.2$ to $2.7$ V $V_{CC} = 2.7$ to $3.6$ V

## LIMITING VALUES FOR THE LVC FAMILY (Note 1)

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+4.6	V	
$I_{IK}$	DC input diode current	-	-50	mA	$V_I < 0$
$V_I$	DC input voltage	-0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	-0.5	$V_{CC} + 0.5$	V	
$I_{OK}$	DC output diode current	-	$\pm 50$	mA	$V_O > V_{CC}$ or $V_O < 0$
$V_O$	DC output voltage	-0.5	$V_{CC} + 0.5$	V	note 2
$I_O$	DC output source or sink current	-	$\pm 50$	mA	$V_O = 0$ to $V_{CC}$
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current	-	$\pm 100$	mA	
$T_{stg}$	storage temperature range	-60	+150	°C	
$P_{tot}$	power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	-	500 500	mW mW	above + 70°C derate linearly with 8 mW/K above + 60°C derate linearly with 5.5 mW/K

## Notes to the limiting values

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**DC CHARACTERISTICS FOR THE LVC FAMILY**

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)			UNIT	TEST CONDITIONS		
		-40 to +85				$V_{CC}$ (V)	$V_I$	OTHER
		MIN.	TYP.	MAX.				
$V_{IH}$	HIGH level input voltage	$V_{CC}$ 2.0	–	–	V	1.2 2.7 to 3.6		
$V_{IL}$	LOW level input voltage	–	–	GND 0.8	V	1.2 2.7 to 3.6		
$V_{OH}$	HIGH level output voltage	$V_{CC} - 0.5$ $V_{CC} - 0.2$ $V_{CC} - 0.6$ $V_{CC} - 1.0$	– $V_{CC}$ –	– –	V	2.7 3.0 3.0 3.0	$V_{IH}$ or $V_{IL}$	$I_O = -12$ mA $I_O = -100$ $\mu$ A $I_O = -12$ mA $I_O = -24$ mA
$V_{OL}$	LOW level output voltage	–	–	0.40 0.20 0.55	V	2.7 3.0 3.0	$V_{IH}$ or $V_{IL}$	$I_O = 12$ mA $I_O = 100$ $\mu$ A $I_O = 24$ mA
$I_I$	input leakage current	–	$\pm 0.1$	$\pm 5$	$\mu$ A	3.6	5.5 V or GND	not for I/O pins
$I_{IHZ}/I_{ILZ}$	input current for common I/O pins	–	$\pm 0.1$	$\pm 15$	$\mu$ A	3.6	$V_{CC}$ or GND	
$I_{OZ}$	3-state output OFF-state current	–	0.1	$\pm 10$	$\mu$ A	3.6	$V_{IH}$ or $V_{IL}$	$V_O = V_{CC}$ or GND
$I_{CC}$	quiescent supply current	–	0.1	20	$\mu$ A	3.6	$V_{CC}$ or GND	$I_O = 0$
$\Delta I_{CC}$	additional quiescent supply current given per input pin	–	5	500	$\mu$ A	2.7 to 3.6	$V_{CC} - 0.6$ V	$I_O = 0$

**Note:** All typical values are measured at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.

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**DC CHARACTERISTICS FOR 74LVC00**

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

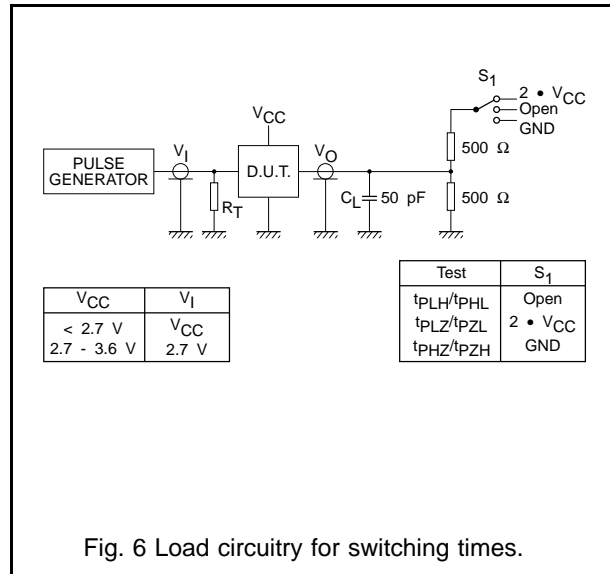
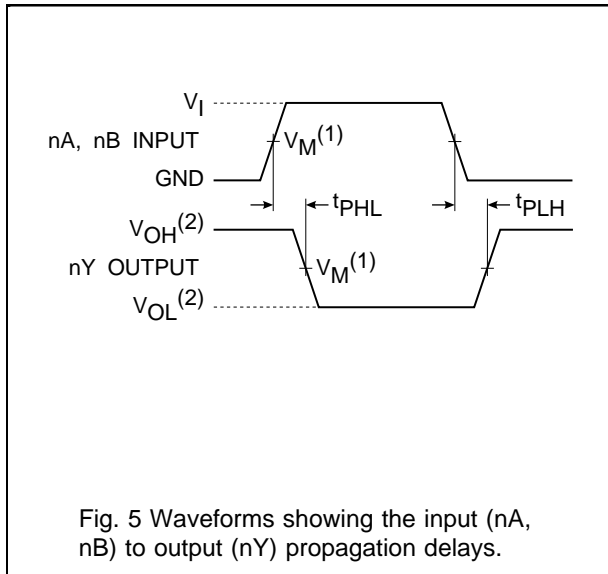
**AC CHARACTERISTICS FOR 74LVC00**

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V <sub>CC</sub> (V)	WAVEFORMS
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	-	20	-	ns	1.2 2.7 3.0 to 3.6	Figs 5, 6
		1.5	4.0	6.5			
		1.5	3.5*	6.0			

**Notes:** All typical values are measured at T<sub>amb</sub> = 25 °C.  
\* Typical values are measured at V<sub>CC</sub> = 3.3 V.

**AC WAVEFORMS**



**Notes:** (1) V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V  
V<sub>M</sub> = 0.5 · V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V  
(2) V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.



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**SOLDERING**

**Plastic mini-packs**

**BY WAVE**

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

**BY SOLDER PASTE REFLOW**

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

**REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING OR PULSE-HEATED SOLDER TOOL)**

Fix the component by first soldering two diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operating of the device at these or any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.