FAIRCHILD SEMICONDUCTOR®

March 2008

NC7WZ00
TinyLogic® UHS Dual 2-Input NAND Gate

Features

- Space saving US8 surface mount package
- MicroPak™ leadless package
- Ultra High Speed; t_{PD} 2.4ns typ. into 50pF at 5V V_{CC}
- High Output Drive; ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V–5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Proprietary noise/EMI reduction circuitry implemented

General Description

The NC7WZ00 is a dual 2-Input NAND Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

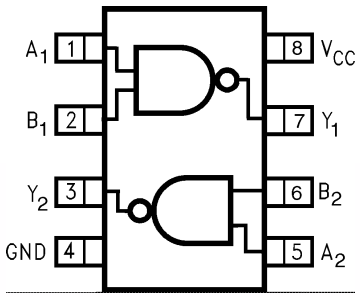
Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ00K8X	MAB08A	WZ00	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ00L8X	MAC08A	N6	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

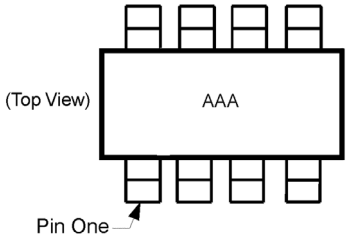
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



(Top View)

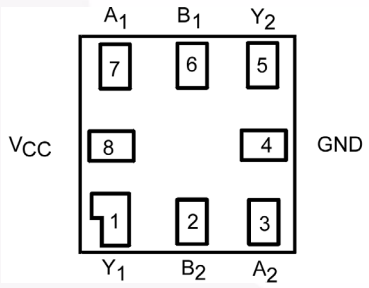
Pin One Orientation Diagram



AAA represents Product Code Top Mark – see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

Logic Symbol

IEEE/IEC

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Pin Description

Pin Names	Description
A_n, B_n	Inputs
Y_n	Output

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7V
V_{IN}	DC Input Voltage	–0.5V to +7V
V_{OUT}	DC Output Voltage	–0.5V to +7V
I_{IK}	DC Input Diode Current @ V_{IN} < –0.5V	–50mA
I_{OK}	DC Output Diode Current @ V_{OUT} < –0.5V	–50mA
I_{OUT}	DC Output Current	±50mA
I_{CC}/I_{GND}	DC V_{CC}/GND Current	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature Under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation @ +85°C	250mW

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage Operating	1.65V to 5.5V
	Supply Voltage Data Retention	1.5V to 5.5V
V_{IN}	Input Voltage	0V to 5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 1.65V ± 0.15V, 2.5V ± 0.2V	0ns/V to 20ns/V
	V_{CC} = 3.3V ±0.3V	0ns/V to 10ns/V
	V_{CC} = 5.0V ±0.5V	0ns/V to 5ns/V
θ_{JA}	Thermal Resistance	250°C/W

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65–1.95			0.75 x V_{CC}			0.75 x V_{CC}		V
		2.3–5.5			0.70 x V_{CC}			0.70 x V_{CC}		
V_{IL}	LOW Level Input Voltage	1.65–1.95					0.25 x V_{CC}		0.25 x V_{CC}	V
		2.3–5.5					0.30 x V_{CC}		0.30 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN} = V_{IL}$	$I_{OH} = -100\mu A$	1.55	1.65		1.55		V
		2.3			2.2	2.3		2.2		
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		1.65		$I_{OH} = -4mA$	1.29	1.52		1.69		
		2.3		$I_{OH} = -8mA$	1.9	2.15		1.9		
		3.0		$I_{OH} = -16mA$	2.4	2.80		2.4		
		3.0		$I_{OH} = -24mA$	2.3	2.68		2.3		
		4.5		$I_{OH} = -32mA$	3.8	4.20		3.8		
V_{OL}	LOW Level Output Voltage	1.65	$V_{IN} = V_{IH}$	$I_{OL} = 100\mu A$		0.0	0.1		0.1	V
		2.3				0.0	0.1		0.1	
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		1.65		$I_{OL} = 4mA$		0.08	0.24		0.24	
		2.3		$I_{OL} = 8mA$		0.10	0.3		0.3	
		3.0		$I_{OL} = 16mA$		0.15	0.4		0.4	
		3.0		$I_{OL} = 24mA$		0.22	0.55		0.55	
		4.5		$I_{OL} = 32mA$		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0–5.5	$V_{IN} = 5.5V$, GND				±0.1		±1	μA
I_{OFF}	Power Off Leakage Current	0.0	V_{IN} or $V_{OUT} = 5.5V$				1		10	μA
I_{CC}	Quiescent Supply Current	1.65–5.5	$V_{IN} = 5.5V$, GND				1		10	μA

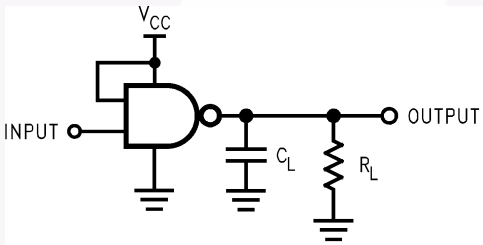
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.8 ± 0.15	C_L = 15pF, R_L = 1MΩ	2.0	5.3	9.6	2.0	9.8	ns	Figure 1 Figure 3
		2.5 ± 0.2		1.2	3.2	5.3	1.2	5.7		
		3.3 ± 0.3		0.8	2.4	3.7	0.8	4.0		
		5.0 ± 0.5		0.5	1.9	2.9	0.5	3.2		
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	C_L = 50pF, R_L = 500Ω	1.2	3.0	4.6	1.2	4.9	ns	Figure 1 Figure 3
		5.0 ± 0.5		0.8	2.4	3.6	0.8	3.9		
C_{IN}	Input Capacitance	0			2.5				pF	
C_{PD}	Power Dissipation Capacitance	3.3	(2)		13				pF	Figure 2
		5.0			17					

Note:

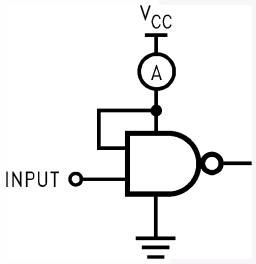
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_w = 500ns

Figure 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f$ = 1.8ns;
PRR = 10 MHz; Duty Cycle = 50%

Figure 2. I_{CCD} Test Circuit

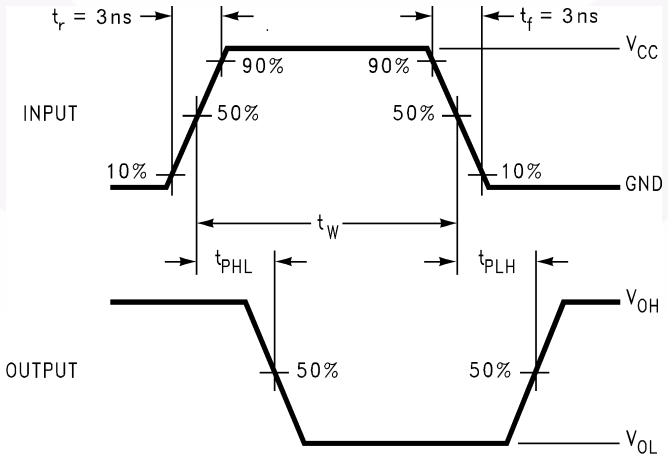


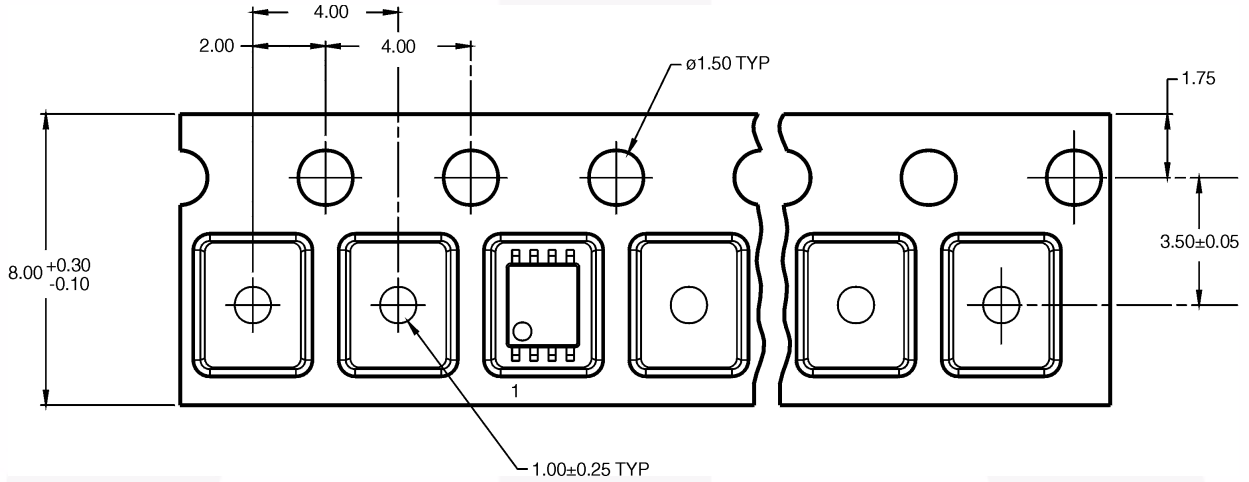
Figure 3. AC Waveforms

Tape and Reel Specifications

Tape Format for US8

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

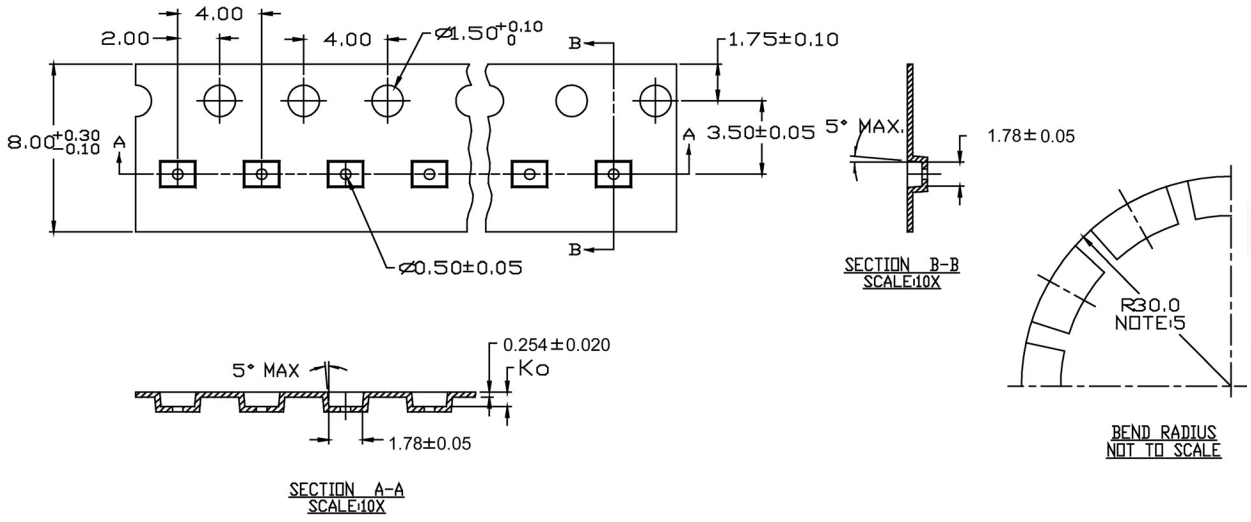
Tape Dimensions inches (millimeters)



Tape Format for MicroPak

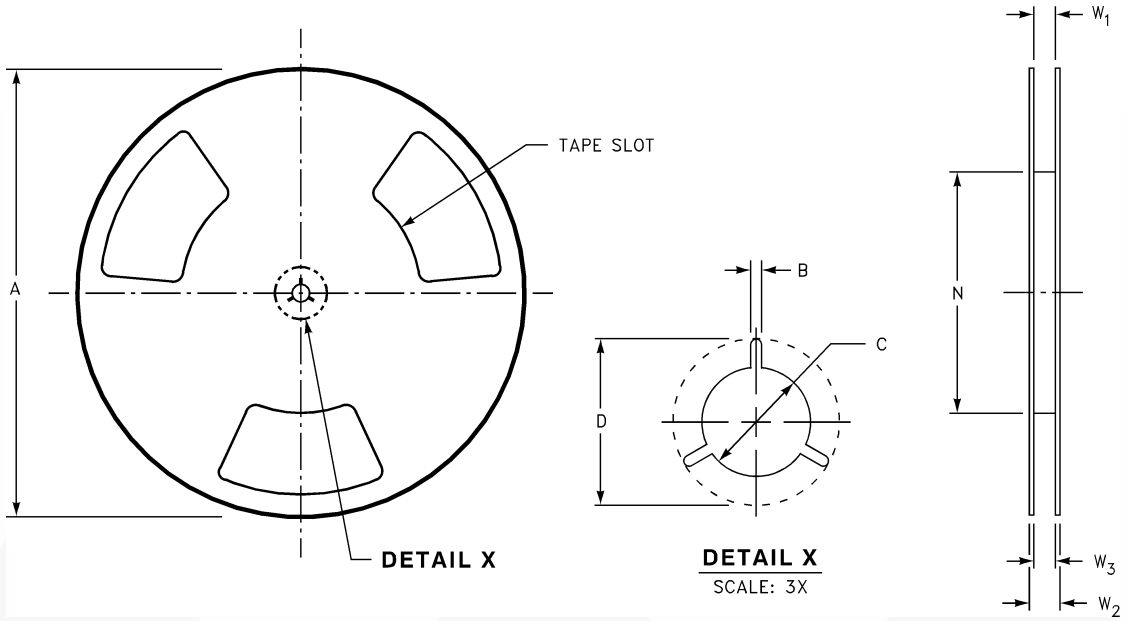
Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions inches (millimeters)



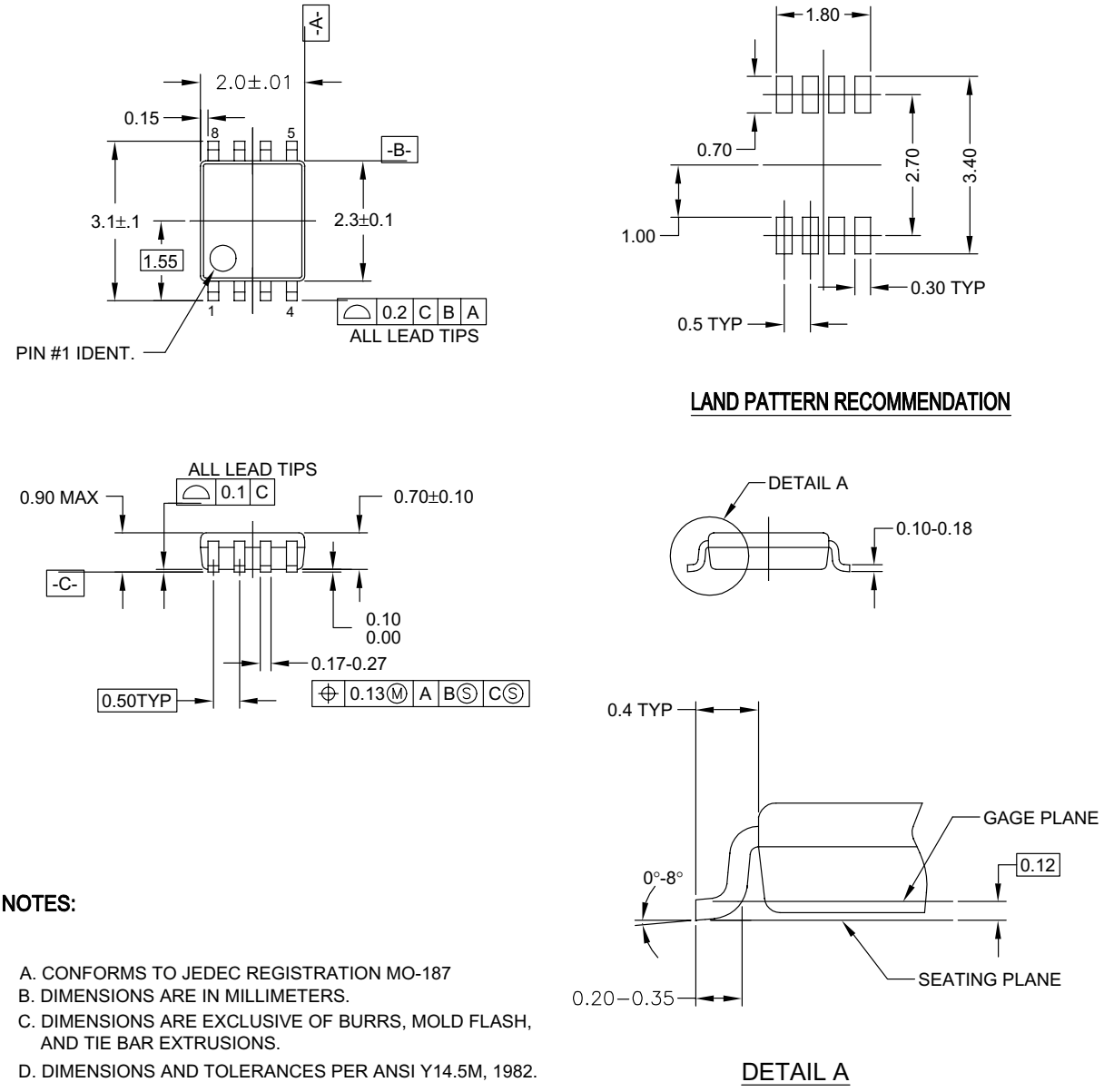
Tape and Reel Specifications (Continued)

Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/–0.000 (8.40 +1.50/–0.00)	0.567 (14.40)	W1 +0.078/–0.039 (W1 +2.00/–1.00)

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

Figure 4. 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide

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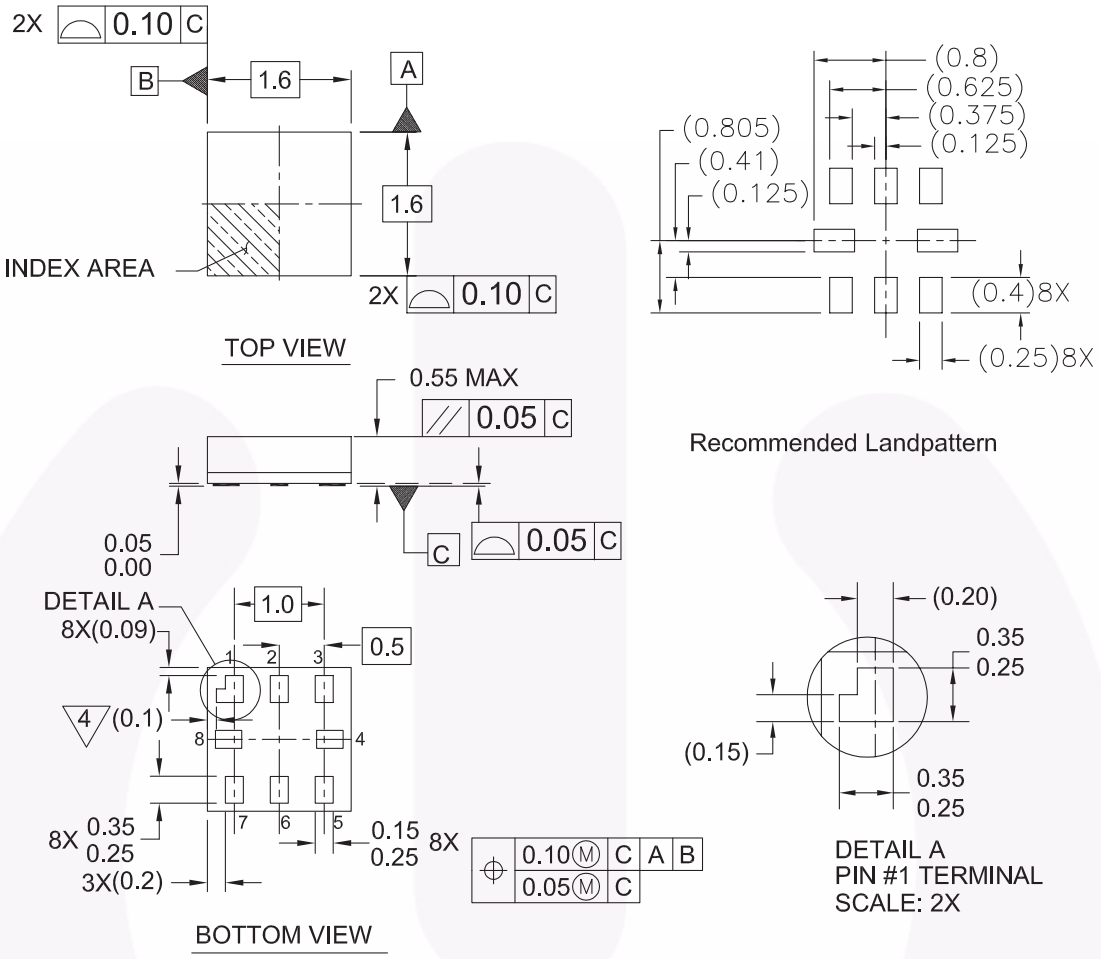
Physical Dimensions (Continued)



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 5. 8-Lead MicroPak, 1.6 mm Wide

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