HARRIS SEMICONDUCTOR

MLE Series

Multilayer Surface Mount ESD Suppressor/Filter

January 1998

Features

- **Rated for ESD (IEC-1000-4-2)**
- **Characterized for Impedance and Capacitance**
- **-55^{o}C to 125^{o}C Operating Temperature Range**
- **Leadless 0603, 0805, and 1206 Chip Sizes**
- **Operating Voltage up to 18$V_{M(DC)}$**
- **Multilayer Ceramic Construction Technology**
- **Available with Nickel/Tin End Terminations**

Applications

- **Protection of Components and Circuits Sensitive to ESD Transients Occurring on Power Supply, Control and Signal Lines**
- **Suppression of ESD Events Such as Specified in IEC-1000-4-2 or MIL-STD-883C Method-3015.7, for Electromagnetic Compliance (EMC)**
- **Used in Mobile Communications, Computer/EDP Products, Medical Products, Hand Held/Portable Devices, Industrial Equipment, Including Diagnostic Port Protection and I/O Interfaces**

Description

The MLE Series is a family of Transient Voltage Suppression devices based on the Harris Multilayer fabrication technology. These components are designed to suppress ESD events, including those specified in IEC1000-4-2 or other standards used for Electromagnetic Compliance testing. The MLE Series is typically applied to protect integrated circuits and other components at the circuit board level operating at 18VDC, or less.

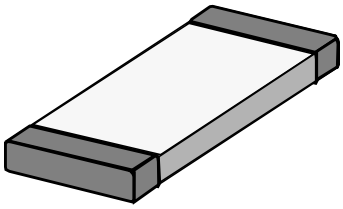
Additionally, the fabrication method and materials of these devices result in capacitance characteristics suitable for high frequency attenuation/low-pass filter circuit functions, thereby, providing suppression and filtering in a single device.

The MLE Series is manufactured from semiconducting ceramics, providing bidirectional voltage clamping and is supplied in leadless, surface mount form compatible with modern reflow and wave soldering procedures.

Harris manufactures other Multilayer Series products. See the ML Series data sheet (Harris AnswerFAX, 407-724-7800, doc. #2461) for higher energy/peak current transient applications. See the AUML Series for automotive applications (AnswerFAX doc. #3387).

Packaging

MLE SERIES (LEADLESS CHIP)



File Number **4263.2**

Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

	MLE SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	≤18	V
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC

Device Ratings and Specifications

PART NUMBER	MAX CONTINUOUS WORKING VOLTAGE -55°C TO 125°C (NOTE 1) $V_{M(DC)}$ (V)	PERFORMANCE SPECIFICATIONS (25°C) NOMINAL VOLTAGE V_{NOM} AT 1mA DC MIN (V)	MAX (V)	(NOTE 2) TYPICAL ESD CLAMP VOLTAGE (8kV CONTACT NOTE 3) PEAK (V)	(15kV AIR NOTE 4) PEAK (V)	(NOTE 5) TYPICAL CAPACITANCE AT 1MHz (pF)	MAXIMUM LEAKAGE $I_{L\ MAX}$ (μA)	AT APPLIED VOLTAGE V_{DC}
V18MLE0603	18	22	28	<140	<85	<100	0.1	3.5
							0.3	5.5
							5.0	15
							25	18
V18MLE0805	18	22	28	<95	<75	<500	0.2	3.5
							0.5	5.5
							5.0	15
							25	18
V18MLE1206	18	22	28	<75	<65	<1700	0.5	3.5
							1.0	5.5
							5.0	15
							25	18

NOTES:

1. For applications of $18V_{DC}$ or less. Higher voltages available, contact Sales.
2. Tested with IEC-1000-4-2 Human Body Model (HBM) discharge test circuit.
3. Direct discharge to device terminals (IEC preferred test method).
4. Corona discharge through air (represents actual ESD event).
5. Capacitance may be customized, contact Sales.

Typical Performance Curves

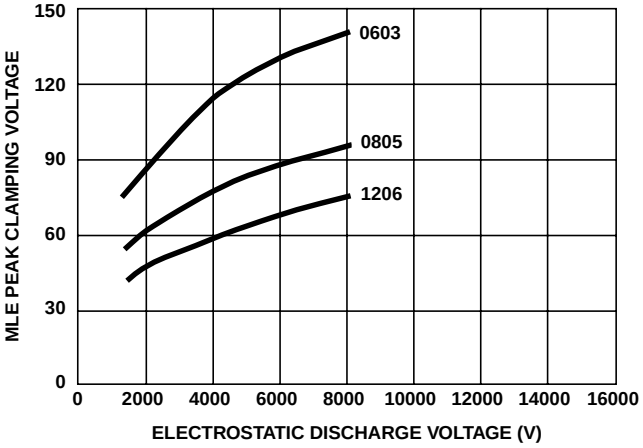


FIGURE 1. CLAMPING CHARACTERISTIC FOR CONTACT METHOD ESD PER IEC-1000-4-2, RANGE 0.5kV TO 8.0kV

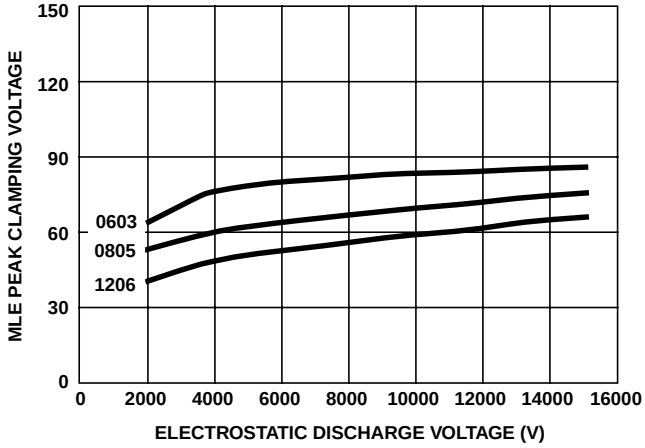


FIGURE 2. CLAMPING CHARACTERISTIC FOR AIR DISCHARGE METHOD ESD PER IEC1000-4-2, RANGE 2kV TO 15kV

Typical Performance Curves (Continued)

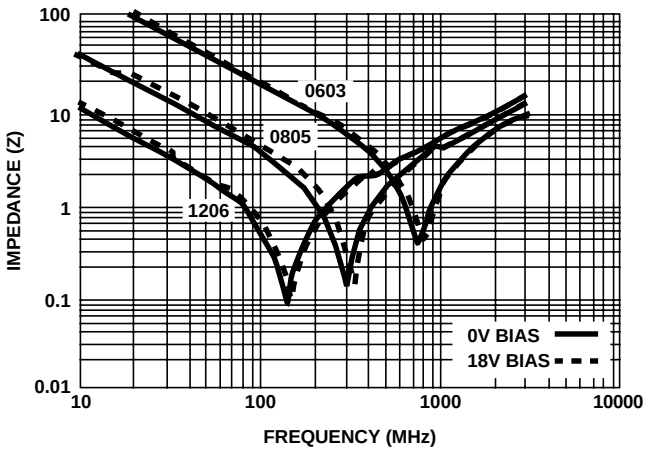


FIGURE 3. IMPEDANCE (Z) vs FREQUENCY TYPICAL CHARACTERISTIC WITH 0V AND 18V_{DC} BIAS

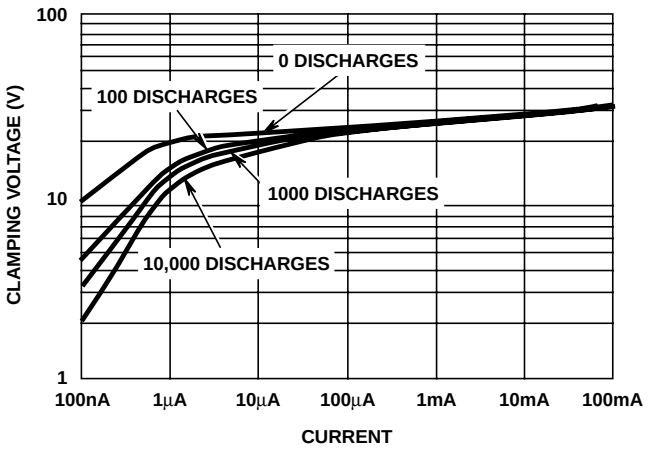


FIGURE 4. V18MLE0805 LEAKAGE CHARACTERISTIC STABILITY AFTER 10,000 x 8kV CONTACT ESD IMPULSES

NOTE: Figure 4 is an example of device clamping characteristics in the Standby (or "Leakage") current region of operation. It is intended to illustrate the stability of the device after the application of multiple, 8kV ESD CONTACT discharges per IEC 1000-4-2. Note that the discharges were applied in one polarity only and the measurements were made in that same polarity.

Multilayer Internal Construction

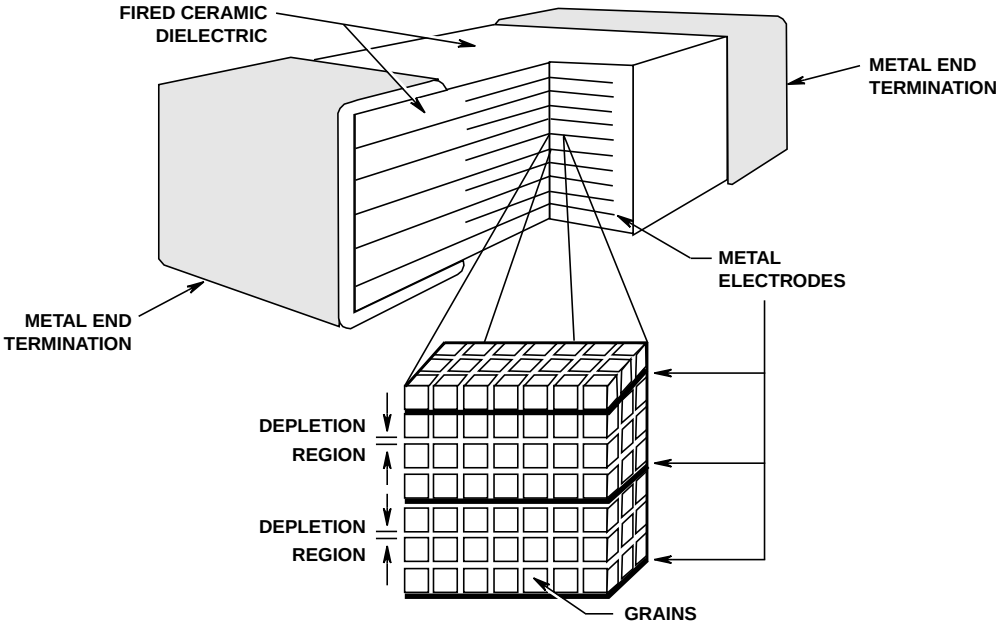


FIGURE 5. DIAGRAM OF INTERDIGITATED METAL ELECTRODES WITHIN THE CERAMIC DIELECTRIC MATERIAL AND REPRESENTATION OF GRAIN STRUCTURE WITHIN EACH LAYER

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapour Phase Reflow, and Wave Soldering. When wave soldering, the MLE suppressor is attached to the circuit board by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process to contact the wave. With IR and Vapour Phase Reflow, the device is placed in a solder paste on the substrate. As the solder paste is heated, it reflows and solders the unit to the board.

With the MLE suppressor, the recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the MLE chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the MLE series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to gradually cool to less than 50^{O}C before cleaning.

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

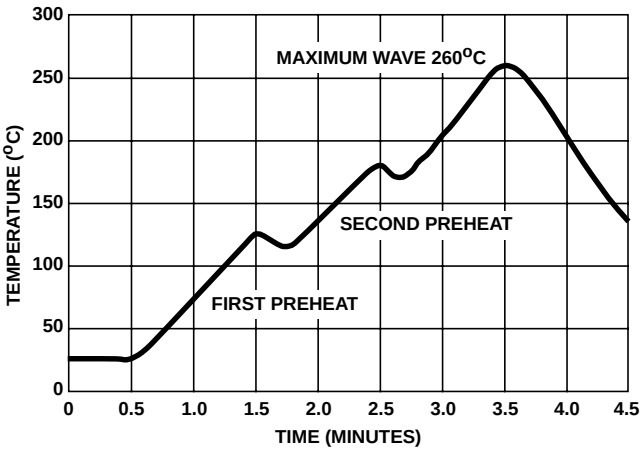


FIGURE 6. WAVE SOLDER PROFILE

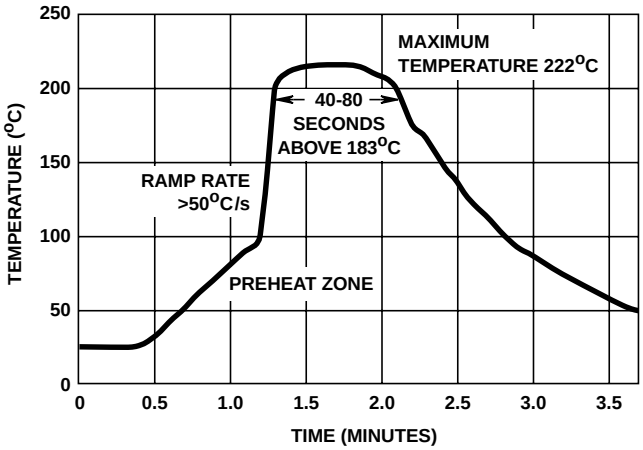


FIGURE 7. VAPOR PHASE SOLDER PROFILE

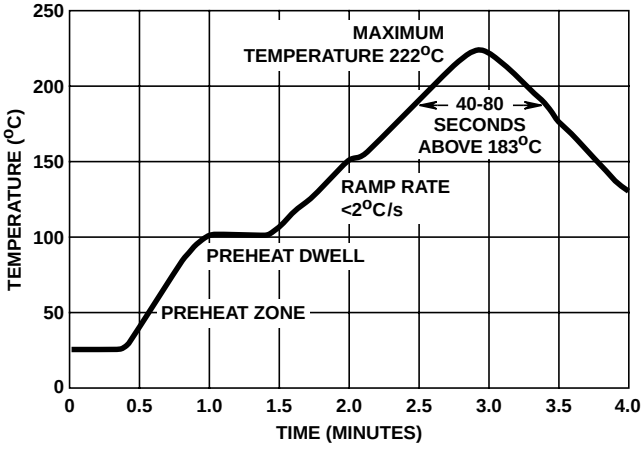


FIGURE 8. REFLOW SOLDER PROFILE

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}} \times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220°C and the next process is at 260°C, then the maximum time allowed at 260°C is:

For Nickel/Tin Termination:

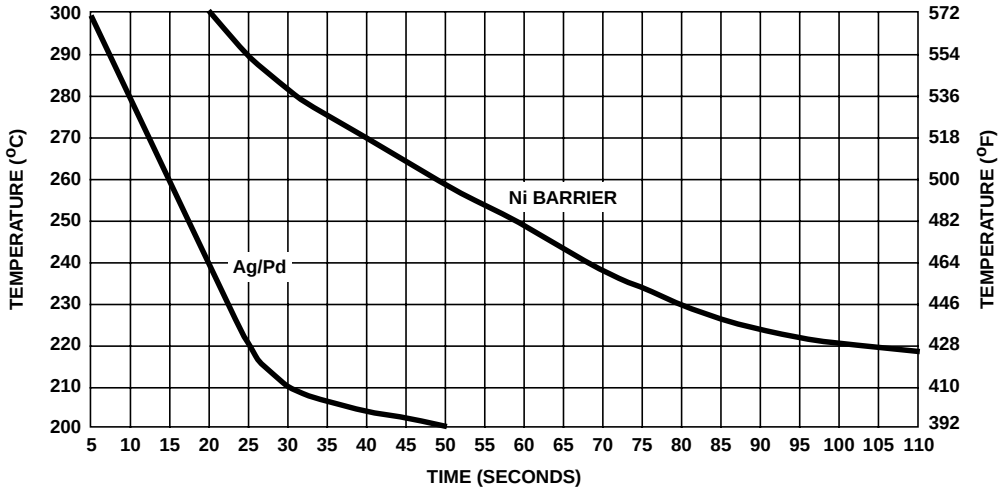
$$\frac{100 - 20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25 - 20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280°C, the Nickel/Tin termination can withstand a further 20 seconds at 280°C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230°C, the total time allowed at this temperature is:

$$\frac{30 - 10}{30} \times 80 = 53 \text{ seconds}$$

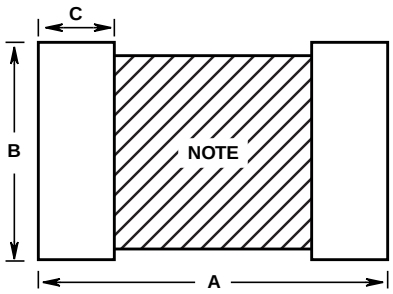


NOTES:

6. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
7. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
8. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 9. SOLDER TEMPERATURE-TIME CURVE

Recommended Pad Outline



NOTE: Avoid metal runs in this area.

SYMBOL	RECOMMENDED PAD SIZE DIMENSIONS					
	FOR 1206 SIZE DEVICE		FOR 0805 SIZE DEVICE		FOR 0603 SIZE DEVICE	
	IN	MM	IN	MM	IN	MM
A	0.203	5.15	0.144	3.66	0.11	2.8
B	0.103	2.62	0.084	2.13	0.064	1.62
C	0.065	1.65	0.058	1.48	0.044	1.12

Explanation of Terms

Rated DC Voltage ($V_{M(DC)}$)

This is the maximum continuous DC voltage which may be applied up to the maximum operating temperature of the device. The rated DC operating voltage (working voltage) is also used as the reference point for leakage current. This voltage is always less than the breakdown voltage of the device.

Leakage (I_L) at Rated DC Voltage

In the nonconducting mode, the device is at a very high impedance ($10^6\Omega$) and appears essentially as an open circuit in the system. The leakage current drawn at this level is very low. See Device Ratings.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off state to the on state and enters its conduction mode of operation. The voltage is usually characterized at the 1mA point and has a specified minimum and maximum voltage listed.

Clamping Voltage (V_C)

This is the peak voltage appearing across the suppressor when measured at conditions of specified pulse current and specified waveform. See Device Ratings.

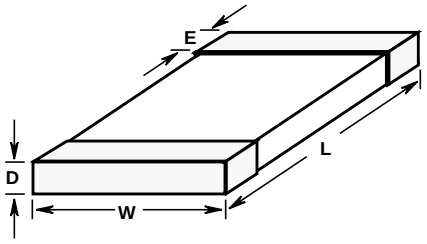
Capacitance (C)

This is the capacitance of the device at a specified frequency (1MHz) and bias ($1V_{P-P}$). See Device Ratings.

IEC 1000-4-2

The electrostatic discharge requirements portion of the electromagnetic compatibility standard written by the International Electrotechnical Commission. The specification describes a specific human body model test conditions and methods.

Mechanical Dimensions

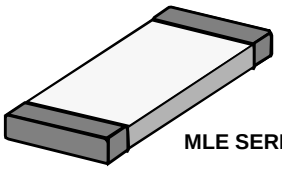


SYMBOL	DEVICE DIMENSIONS					
	1206 SIZE		0805 SIZE		0603 SIZE	
	INCH	MM	INCH	MM	INCH	MM
D Max.	0.071	1.80	0.043	1.1	0.035	0.9
E	0.02 ±0.01	0.50 ±0.25	0.02 to ±0.01	0.50 to ±0.25	0.015 ±0.008	0.4 ±0.2
L	0.125 ±0.012	3.20 ±0.03	0.079 ±0.008	2.01 ±0.2	0.063 ±0.006	1.6 ±0.15
W	0.06 ±0.011	1.60 ±0.28	0.049 ±0.008	1.25 ±0.2	0.032 ±0.006	0.8 ±0.15

Ordering Information

VXXMLE TYPES

V 18 ML X 1206 X X X



MLE SERIES

DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER DESIGNATOR

PERFORMANCE DESIGNATOR
A: Standard
E: ESD (See ML Data Sheet)

DEVICE SIZE:
i.e., 120 mil x 60 mil

CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version (Where available - see device ratings for standard versions)

END TERMINATION OPTION
No Letter: Ag/P_t (Standard)
W: Ag/P_d
N: Ni/Sn

PACKING OPTIONS
A: <100 pc Bulk Pak
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: See quantity table.

Standard Shipping Quantities

DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H" OPTION)	BULK PACK ("A" OPTION)
1206	10,000	2,500	100
0805	10,000	2,500	100
0603	10,000	2,500	100

Tape and Reel Specifications

- **Conforms to EIA - 481, Revision A**
- **Can be Supplied to IEC Publication 286 - 3**

SYMBOL	DESCRIPTION	MILLIMETERS
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.
W	Width of Tape	8 ± 0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ± 0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ± 0.1
P_1	Distance Between Cavity Center	4 ± 0.1
P_2	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ± 0.1
P_0	Axial Distance Between Drive Hole Centers	4 ± 0.1
D_0	Drive Hole Diameter	1.55 ± 0.05
D_1	Diameter of Cavity Piercing	1.05 ± 0.05
t_1	Embossed Tape Thickness	0.3 max
t_2	Top Tape Thickness	0.1 max

NOTE: Dimensions in millimeters.