

FEATURES

- Physical layer CAN transceiver
- 5 V operation on V_{CC}
- Complies with ISO 11898 standard
- High speed data rates up to 1 Mbps
- Short-circuit protection on CANH and CANL against shorts to power/ground in 24 V systems
- Unpowered nodes do not disturb the bus
- Connect 110 or more nodes on the bus
- Slope control for reduced EMI
- Thermal shutdown protection
- Low current standby mode
- Industrial operating temperature range (-40°C to $+125^{\circ}\text{C}$)
- Available in 8-lead SOIC package

APPLICATIONS

- CAN data buses
- Industrial field networks
- DeviceNet applications
- CanOpen, CanKingdom

GENERAL DESCRIPTION

The [ADM3051](#) is a controller area network (CAN) physical layer transceiver allowing a protocol layer CAN controller to access the physical layer bus. The [ADM3051](#) complies with the ISO 11898 standard. It is capable of running at data rates up to 1 Mbps.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where the bus may be shorted to ground or power terminals in 24 V bus power systems. The part is fully specified over the industrial temperature range of -40°C to $+125^{\circ}\text{C}$ and is available in an 8-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM

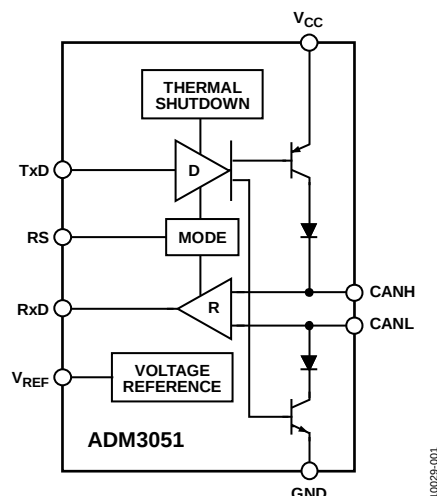


Figure 1.

Three operating modes are available: high speed, slope control, and standby. Pin 8 (RS) is used to select the operating mode. The low current standby mode can be selected by applying a logic high to RS.

The device can be set to operate with slope control to limit EMI by connecting RS with a resistor to ground to modify the rise and fall of slopes. This mode facilitates the use of unshielded cables. Alternatively, disabling slope control by connecting RS to ground allows high speed operation. Shielded cables or other measures to control EMI are necessary in this mode.

Rev. 0

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REVISION HISTORY

9/11—Revision 0: Initial Revision

SPECIFICATIONS

All voltages relative to ground (Pin 2); $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 60\ \Omega$, $I_{RS} > -10\ \mu\text{A}$, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT	I_{CC}					
Dominant State				78	mA	$V_{TXD} = 1\text{ V}$
Recessive State				10	mA	$V_{TXD} = 4\text{ V}$; $R_{SLOPE} = 47\text{ k}\Omega$
Standby State			275		μA	$V_{RS} = V_{CC}$, $I_{TXD} = I_{RXD} = I_{VREF} = 0\text{ mA}$, $T_A < 90^\circ\text{C}$
DRIVER						
Logic Inputs						
Input Voltage High	V_{IH}	$0.7 V_{CC}$		$V_{CC} + 0.3$	V	Output recessive
Input Voltage Low	V_{IL}	-0.3		$+0.3 V_{CC}$	V	Output dominant
CMOS Logic Input Current High	I_{IH}	-200		$+30$	μA	$V_{TXD} = 4\text{ V}$
CMOS Logic Input Current Low	I_{IL}	-100		-600	μA	$V_{TXD} = 1\text{ V}$
Differential Outputs						
Recessive Bus Voltage	V_{CANH}, V_{CANL}	2.0		3.0	V	$V_{TXD} = 4\text{ V}$, $R_L = \infty$, see Figure 23
Off-State Output Leakage Current	I_{LO}	-2		$+2$	mA	$-2\text{ V} < (V_{CANL}, V_{CANH}) < 7\text{ V}$
	I_{LO}	-10		$+10$	mA	$-5\text{ V} < (V_{CANL}, V_{CANH}) < 36\text{ V}$
CANH Output Voltage	V_{CANH}	3.0		4.5	V	$V_{TXD} = 1\text{ V}$, see Figure 23
CANL Output Voltage	V_{CANL}	0.5		2.0	V	$V_{TXD} = 1\text{ V}$, see Figure 23
Differential Output Voltage	V_{OD}	1.5		3.0	V	$V_{TXD} = 1\text{ V}$, see Figure 23
	V_{OD}	1.5			V	$V_{TXD} = 1\text{ V}$, $R_L = 45\ \Omega$, see Figure 23
	V_{OD}	-500		$+50$	mV	$V_{TXD} = 4\text{ V}$, $R_L = \infty$, see Figure 23
Short-Circuit Current, CANH	I_{SCCANH}			-200	mA	$V_{CANH} = -5\text{ V}$
	I_{SCCANH}		-100		mA	$V_{CANH} = -36\text{ V}$
Short-Circuit Current, CANL	I_{SCCANL}			200	mA	$V_{CANL} = 36\text{ V}$
RECEIVER						
Differential Inputs						
Voltage Recessive	V_{IDR}	-1.0		$+0.5$	V	$-2\text{ V} < V_{CANL}, V_{CANH} < 7\text{ V}$, see Figure 25, $V_{CC} = 4.75\text{ V}$ to 5.25 V , $C_L = 30\text{ pF}$
		-1.0		$+0.4$	V	$-7\text{ V} < V_{CANL}, V_{CANH} < 12\text{ V}$, see Figure 25, $C_L = 30\text{ pF}$
Voltage Dominant	V_{IDD}	0.9		5.0	V	$-2\text{ V} < V_{CANL}, V_{CANH} < 7\text{ V}$, see Figure 25, $V_{CC} = 4.75\text{ V}$ to 5.25 V , $C_L = 30\text{ pF}$
		1.0		5.0	V	$-7\text{ V} < V_{CANL}, V_{CANH} < 12\text{ V}$, see Figure 25, $C_L = 30\text{ pF}$ ¹
Input Voltage Hysteresis	V_{HYS}		150		mV	See Figure 26
CANH, CANL Input Resistance	R_{IN}	5		25	k Ω	
Differential Input Resistance	R_{DIFF}	20		100	k Ω	
Logic Outputs						
Output Voltage High	V_{OH}	$0.8 V_{CC}$		V_{CC}	V	$I_{OUT} = -100\ \mu\text{A}$
Output Voltage Low	V_{OL}	0		$0.2 V_{CC}$	V	$I_{OUT} = 1\text{ mA}$
	V_{OL}	0		1.5	V	$I_{OUT} = 10\text{ mA}$
Short-Circuit Current	$ I_{OS} $			120	mA	$V_{OUT} = \text{GND or } V_{CC}$
VOLTAGE REFERENCE						
Reference Output Voltage	V_{REF}	2.025		3.025	V	$V_{RS} = 1\text{ V}$, $ I_{REF} = 50\ \mu\text{A}$
	V_{REF}	$0.4 V_{CC}$		$0.6 V_{CC}$	V	$V_{RS} = 4\text{ V}$, $ I_{REF} = 5\ \mu\text{A}$
STANDBY/SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	$0.75 V_{CC}$			V	
Current for Slope Control Mode	I_{SLOPE}	-10		-200	μA	
Slope Control Mode Voltage	V_{SLOPE}	$0.4 V_{CC}$		$0.6 V_{CC}$	V	

¹ In standby, $V_{CC} = 4.75\text{ V}$ to 5.25 V .

TIMING SPECIFICATIONS

All voltages are relative to ground (Pin 2); $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		1			Mbps	$V_{RS} = 1\text{ V}$
Propagation Delay from TxD On to Bus Active	t_{onTxD}			50	ns	$V_{RS} = 1\text{ V}$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
Propagation Delay from TxD Off to Bus Inactive	t_{offTxD}		40	80	ns	$V_{RS} = 1\text{ V}$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
RECEIVER						
Propagation Delay from TxD On to Receiver Active	t_{onRxD}		55	120	ns	$V_{RS} = 1\text{ V}$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
			440	600	ns	$R_{SLOPE} = 47\text{ k}\Omega$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
Propagation Delay from TxD Off to Receiver Inactive	t_{offRxD}		90	190	ns	$R_{SLOPE} = 0\ \Omega$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
			290	400	ns	$R_{SLOPE} = 47\text{ k}\Omega$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
Bus Dominant to RxD Low	t_{dRxDL}			3	μs	$V_{RS} = 4\text{ V}$, $V_{TxD} = 4\text{ V}$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 29
CANH, CANL Slew Rate	$ SR $		7		$\text{V}/\mu\text{s}$	$R_{SLOPE} = 47\text{ k}\Omega$, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, see Figure 24, Figure 27
TIME TO WAKE-UP FROM STANDBY	t_{WAKE}			20	μs	$V_{TxD} = 1\text{ V}$, see Figure 28

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +7 V
Digital Input Voltage TxD	−0.3 V to $V_{CC} + 0.3$ V
Digital Output Voltage RxD	−0.3 V to $V_{CC} + 0.3$ V
CANH, CANL	−36 V to +36 V
V_{REF}	−0.3 V to $V_{CC} + 0.3$ V
RS	−0.3 V to $V_{CC} + 0.3$ V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−55°C to +150°C
ESD (Human Body Model) on All Pins	4 kV
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
θ_{JA} Thermal Impedance	110°C/W
T_J Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

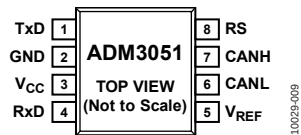


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TxD	Driver Input Data.
2	GND	Ground.
3	V _{CC}	Power Supply. This pin requires a decoupling capacitor to GND of 100 nF.
4	RxD	Receiver Output Data.
5	V _{REF}	Reference Voltage Output.
6	CANL	Low Level CAN Voltage Input/Output.
7	CANH	High Level CAN Voltage Input/Output.
8	RS	Slope Resistor Input.

TYPICAL PERFORMANCE CHARACTERISTICS

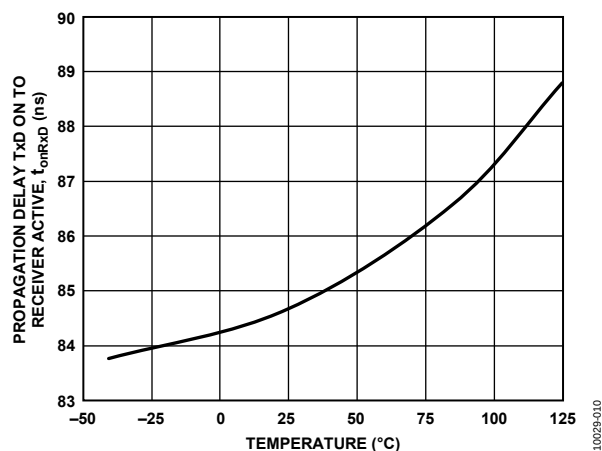


Figure 3. Propagation Delay from TxD On to Receiver Active vs. Temperature

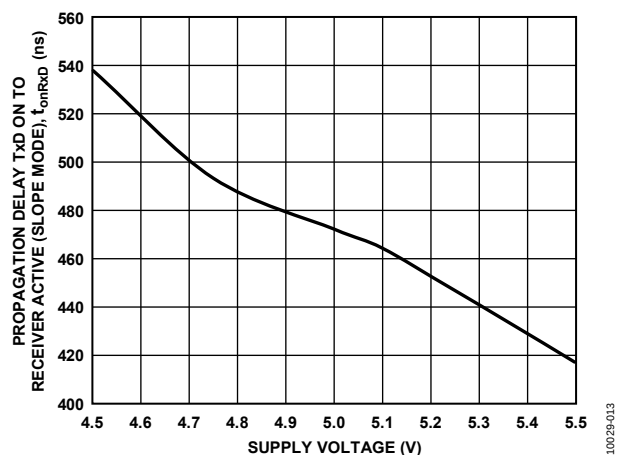
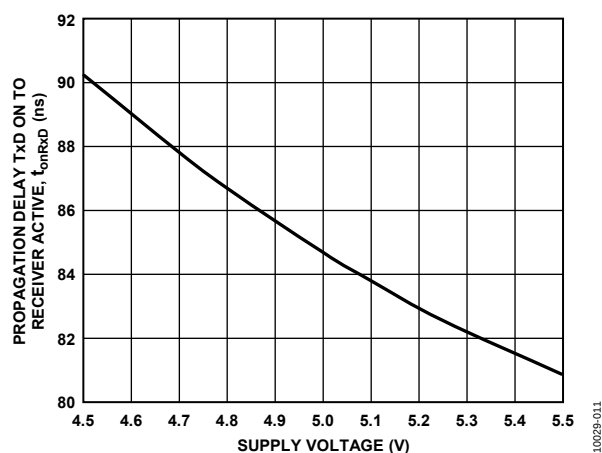
Figure 6. Propagation Delay (Slope Control Mode, $R_{SLOPE} = 47\text{ k}\Omega$) from TxD On to Receiver Active vs. Supply Voltage

Figure 4. Propagation Delay from TxD On to Receiver Active vs. Supply Voltage

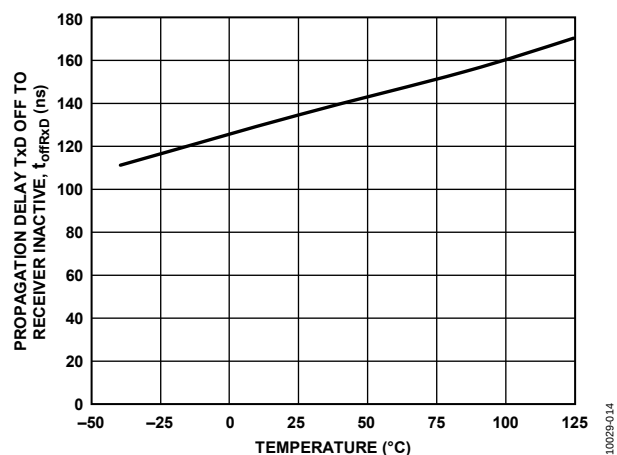


Figure 7. Propagation Delay from TxD Off to Receiver Inactive vs. Temperature

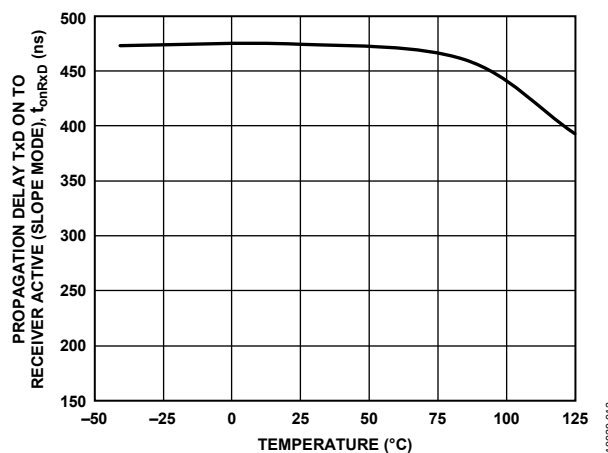
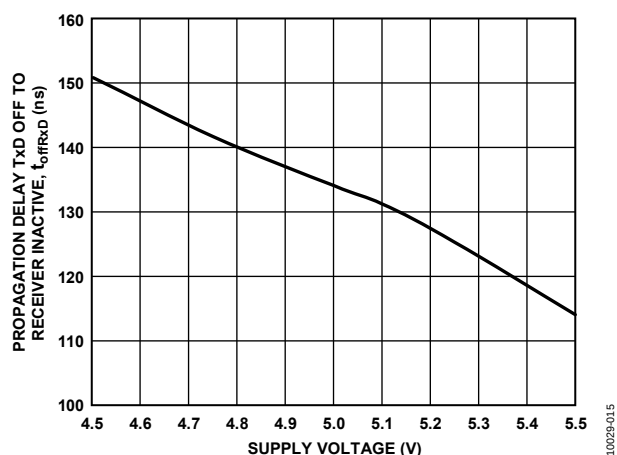
Figure 5. Propagation Delay (Slope Control Mode, $R_{SLOPE} = 47\text{ k}\Omega$) from TxD On to Receiver Active vs. Temperature

Figure 8. Propagation Delay from TxD Off to Receiver Inactive vs. Supply Voltage

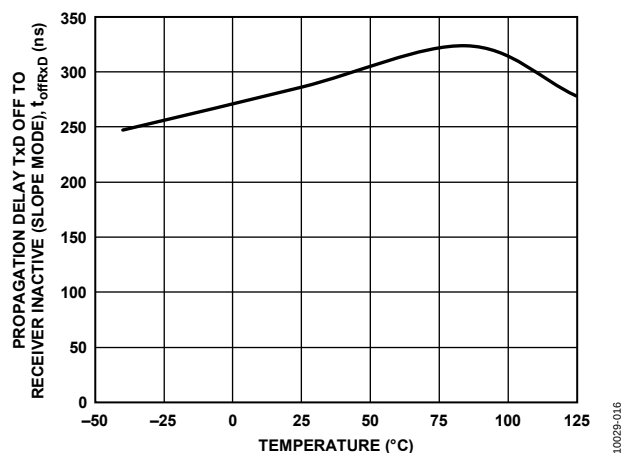


Figure 9. Propagation Delay (Slope Control Mode, $R_{SLOPE} = 47\text{ k}\Omega$) from TxD Off to Receiver Inactive vs. Temperature

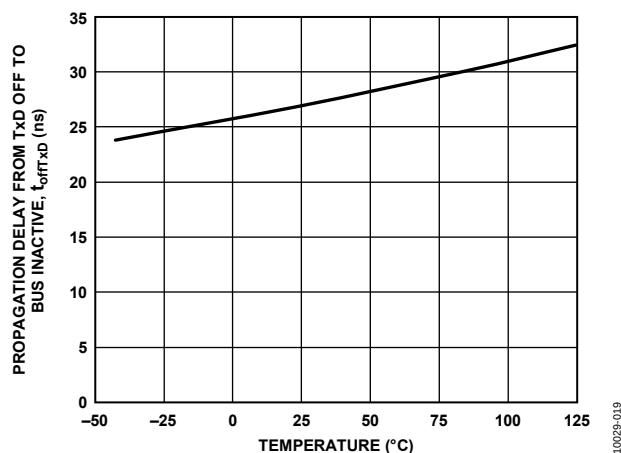


Figure 12. Propagation Delay from TxD Off to Bus Inactive vs. Temperature

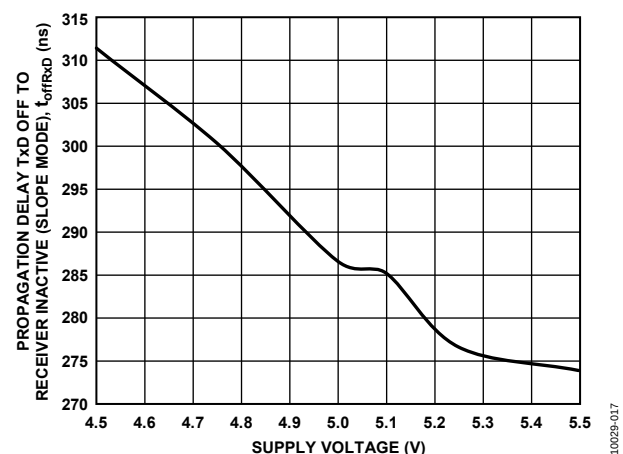


Figure 10. Propagation Delay (Slope Control Mode, $R_{SLOPE} = 47\text{ k}\Omega$) from TxD Off to Receiver Inactive vs. Supply Voltage

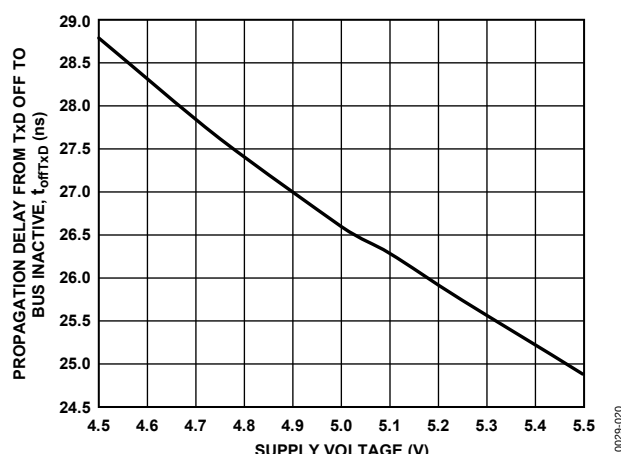


Figure 13. Propagation Delay from TxD Off to Bus Inactive vs. Supply Voltage

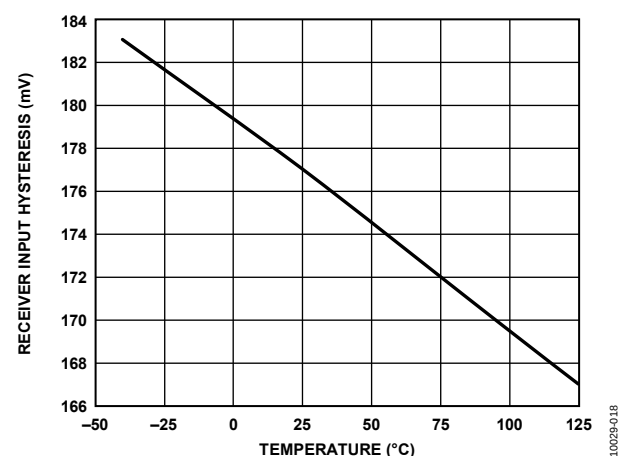


Figure 11. Receiver Input Hysteresis vs. Temperature

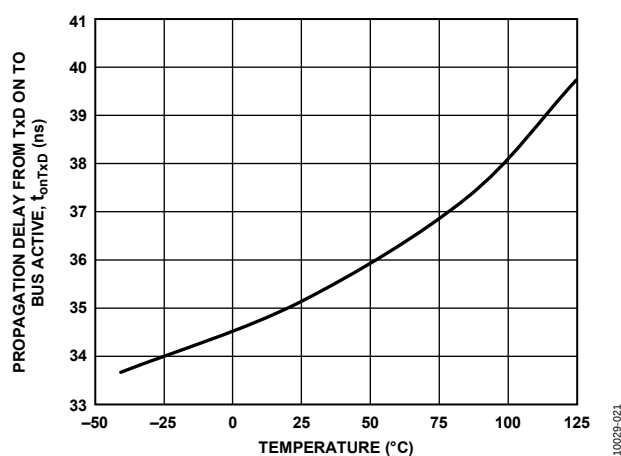


Figure 14. Propagation Delay from TxD On to Bus Active vs. Temperature

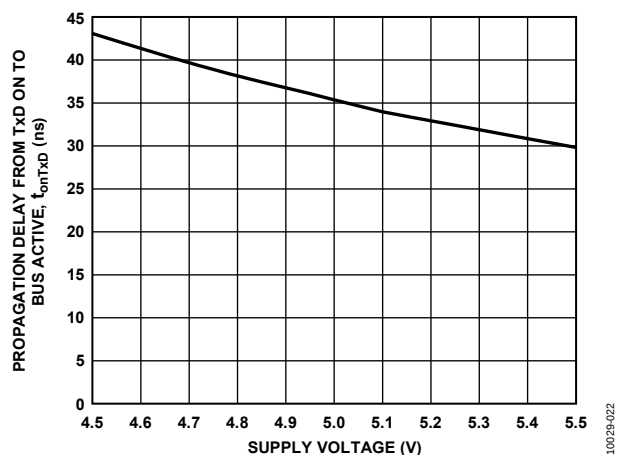


Figure 15. Propagation Delay from TxD On to Bus Active vs. Supply Voltage

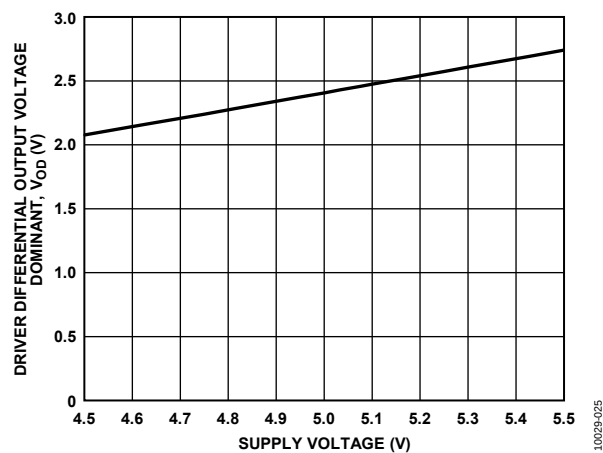


Figure 18. Driver Differential Output Voltage Dominant vs. Supply Voltage

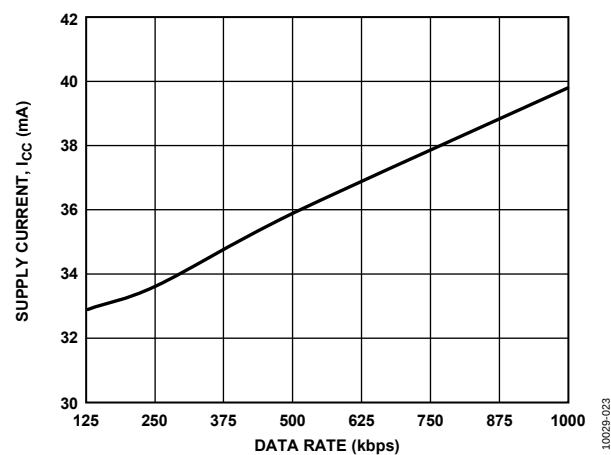
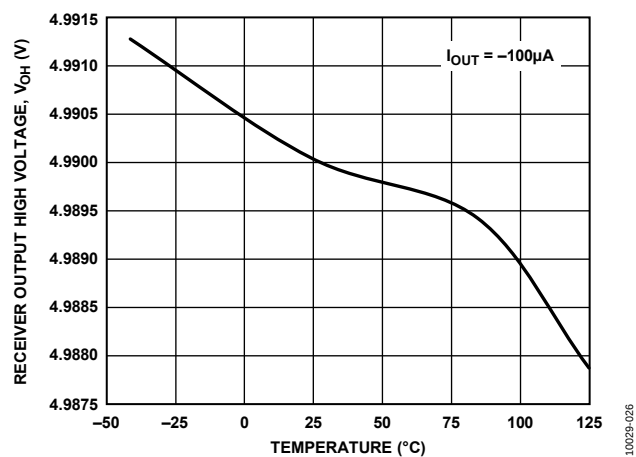
Figure 16. Supply Current (I_{CC}) vs. Data Rate

Figure 19. Receiver Output High Voltage vs. Temperature

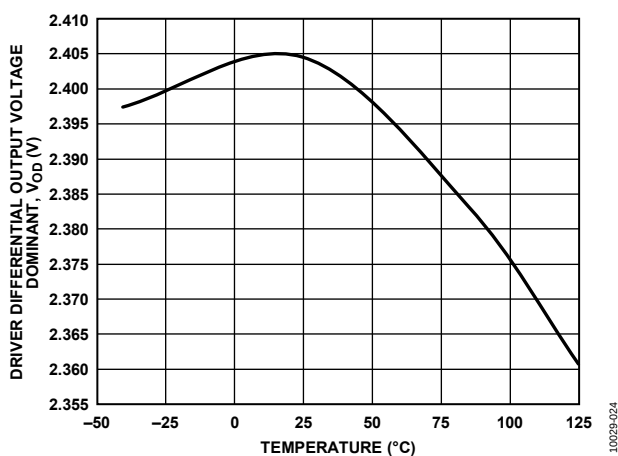


Figure 17. Driver Differential Output Voltage Dominant vs. Temperature

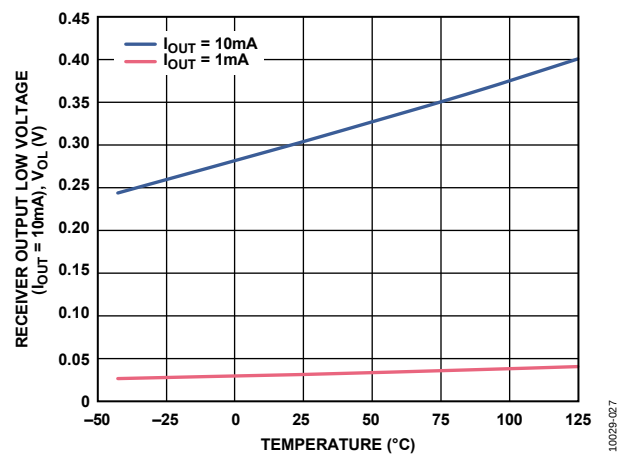


Figure 20. Receiver Output Low Voltage vs. Temperature

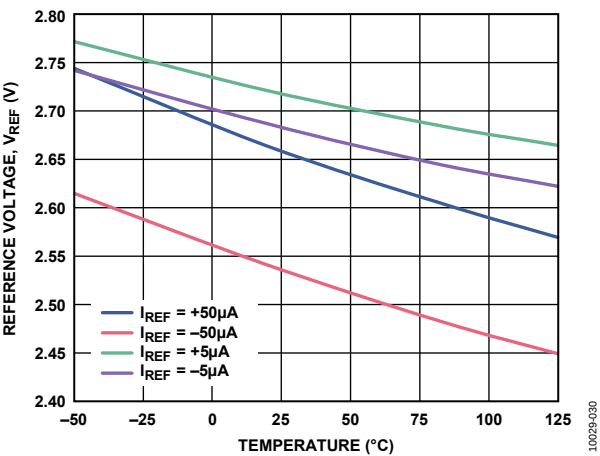


Figure 21. V_{REF} vs. Temperature

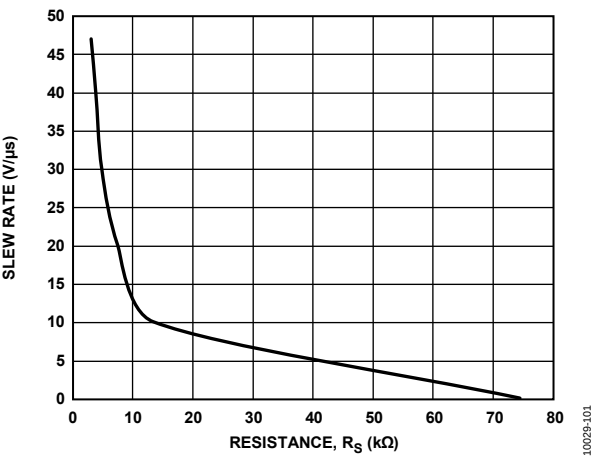


Figure 22. Driver Slew Rate vs. Resistance, R_{SLOPE}

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

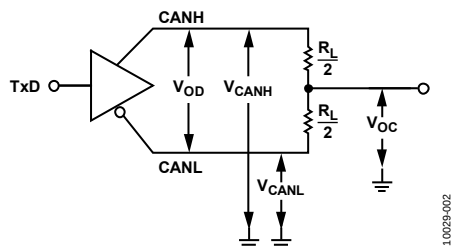


Figure 23. Driver Voltage Measurements

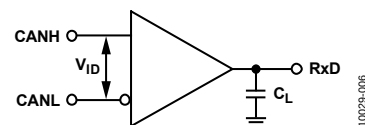


Figure 25. Receiver Voltage Measurements

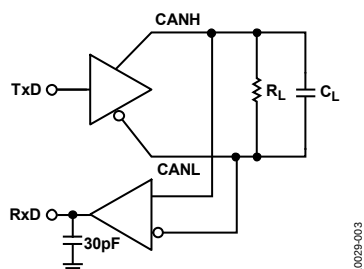


Figure 24. Switching Characteristics Measurements

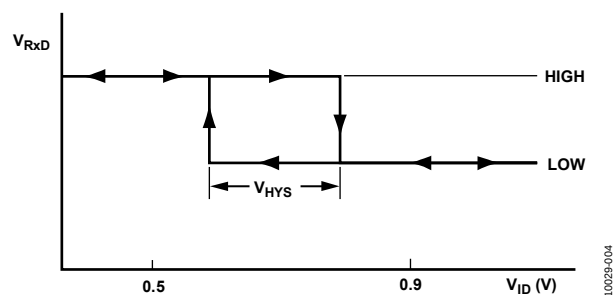


Figure 26. Receiver Input Hysteresis

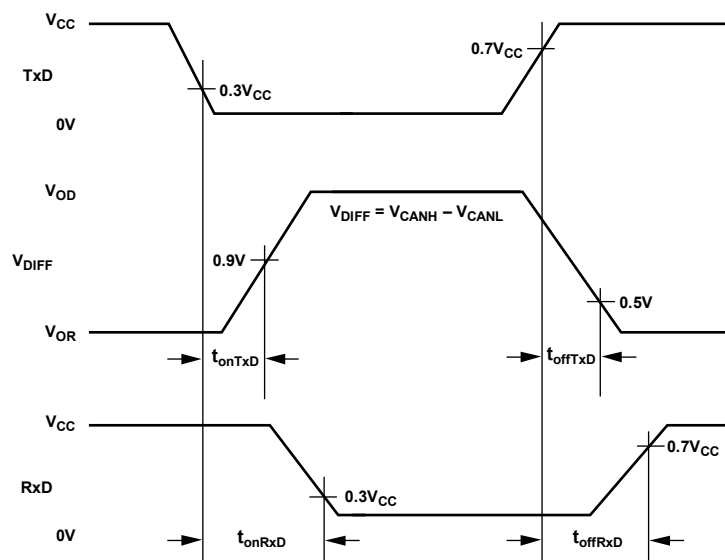


Figure 27. Driver and Receiver Propagation Delay

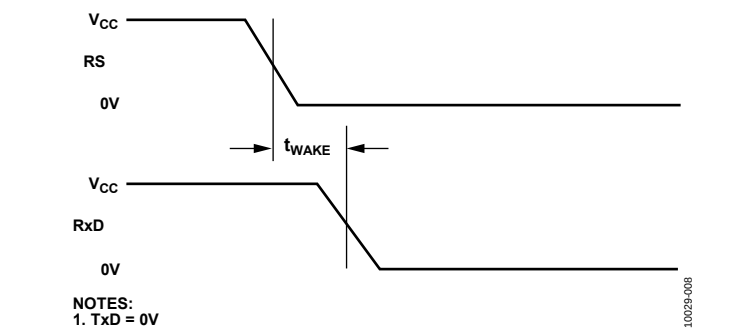


Figure 28. Wake-Up Delay Returning from Standby Mode

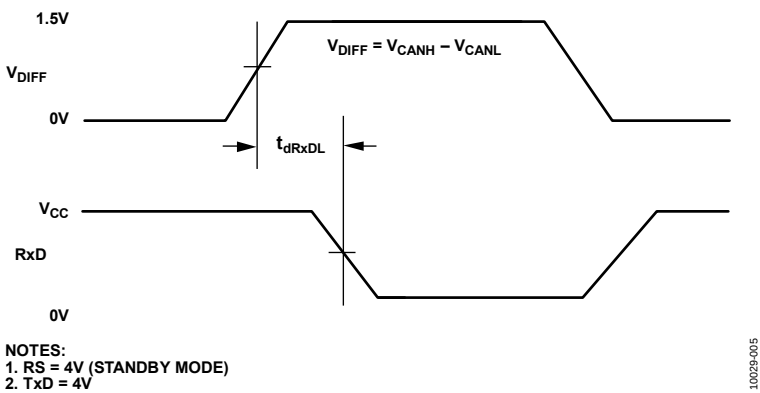


Figure 29. Bus Dominant to RxD Low (Standby Mode)

CIRCUIT DESCRIPTION

CAN TRANSCEIVER OPERATION

A CAN bus has two states: dominant and recessive. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 0.9 V. A recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. During a dominant bus state, the CANH pin is high and the CANL pin is low. During a recessive bus state, both the CANH and CANL pins are in the high impedance state.

The driver drives CANH high and CANL low (dominant state) if a logic low is present on TxD. If a logic high is present on TxD, the driver output is placed in a high impedance state (recessive state). The driver output states are shown in Table 7.

The receiver output is low if the bus is in the dominant state and high if the bus is in the recessive state. If the differential voltage between CANH and CANL is between 0.5 V and 0.9 V, the bus state is indeterminate and the receiver output may be high or low. The receiver output states for given inputs are listed in Table 8.

OPERATIONAL MODES

Three modes of operation are available: high speed, slope control, and standby. RS (Pin 8) allows modification of the operational mode by connecting the RS input through a resistor to ground, or directly to ground, or to a CAN controller, as shown in Figure 30.

With RS connected to ground, the output transistors switch on and off at the maximum rate possible in high speed mode, with no modification to the rise and fall slopes. EMI in this mode can be alleviated using shielded cables.

Alternatively, connecting RS to a resistor, R_{SLOPE} , allows slope control mode, with the value of the resistor modifying the rise and fall slopes. The reduced EMI allows the use of unshielded cables.

Applying a logic high to RS initiates a low current standby mode. The transmitter is disabled, and the receiver is connected to a low current. RxD goes low upon receiving dominant bits, allowing an attached microcontroller that detects this to wake the transceiver via Pin 8, which returns it to standard operation. The receiver is slower in standby mode and loses the first message at higher bit rates.

Table 5. Mode Selection Using RS Pin (Pin 8)

Mode	Condition to Force	Resulting Voltage/Current
Standby	$V_{RS} > 0.75 V_{CC}$	$-I_{RS} < 10 \mu A$
Slope Control	$10 \mu A < -I_{RS} < 200 \mu A$	$0.4 V_{CC} < V_{RS} < 0.6 V_{CC}$
High Speed	$V_{RS} < 0.3 V_{CC}$	$-I_{RS} < -500 \mu A$

TRUTH TABLES

The truth tables in this section use the abbreviations found in Table 6.

Table 6. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
X	Don't care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected

Table 7. Transmitting

Supply	Input	Outputs		
V_{CC}	TxD	State	CANH	CANL
On	L	Dominant	H	L
On	H	Recessive	Z	Z
On	Z	Recessive	Z	Z
Off	X	Z	Z	Z

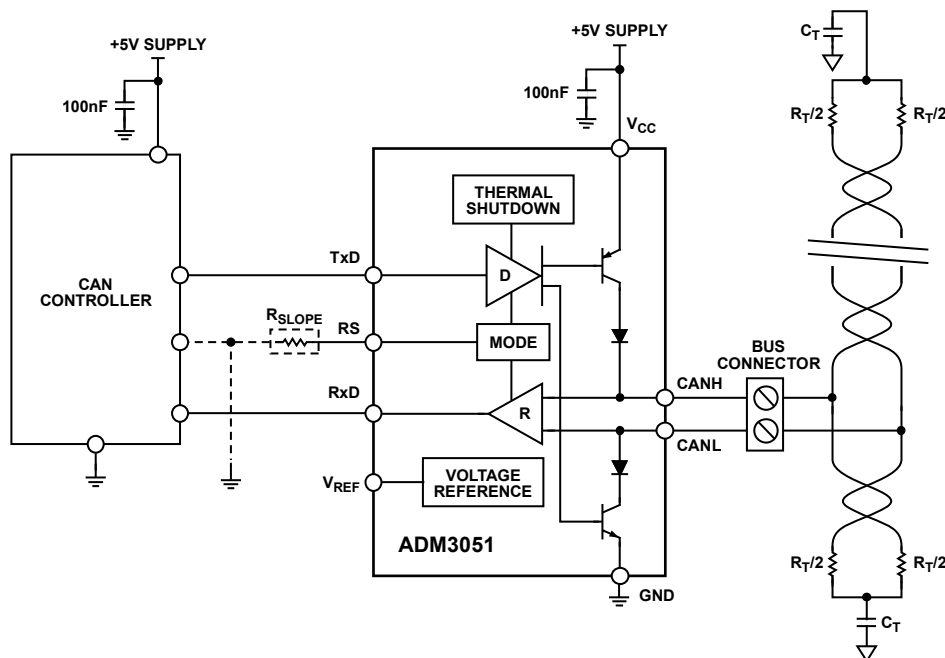
Table 8. Receiving

Supply	Inputs		Output
V_{CC}	$V_{ID} = \text{CANH} - \text{CANL}$	Bus State	RxD
On	$\geq 0.9 V$	Dominant	L
On	$\leq 0.5 V$	Recessive	H
On	$0.5 V < V_{ID} < 0.9 V$	I	I
On	Inputs open	Recessive	H
Off	X	X	I

THERMAL SHUTDOWN

The ADM3051 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The design of this circuitry ensures the disabling of driver outputs upon reaching a die temperature of 150°C. As the device cools, reenabling of the drivers occurs at a temperature of 140°C.

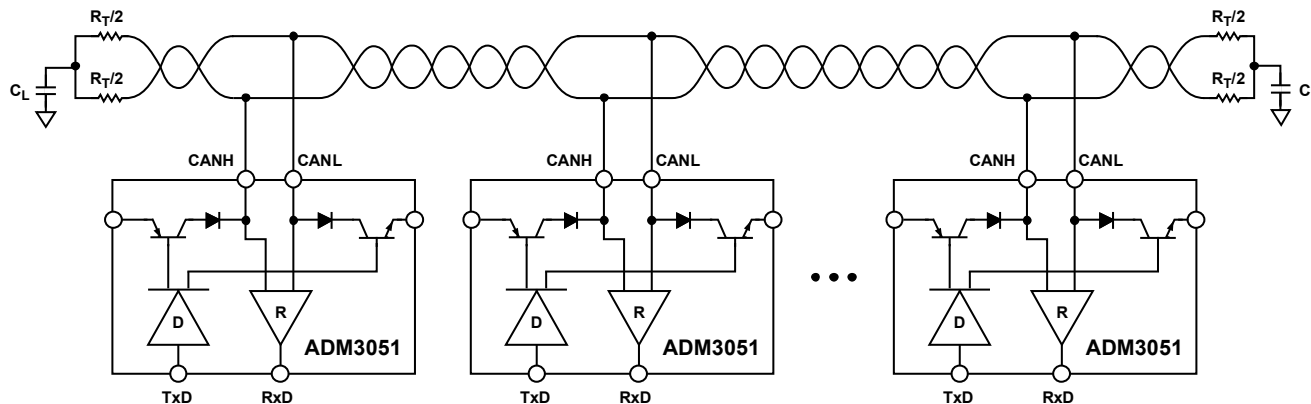
APPLICATIONS INFORMATION



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 30. Typical CAN Node Using the ADM3051

10029-028

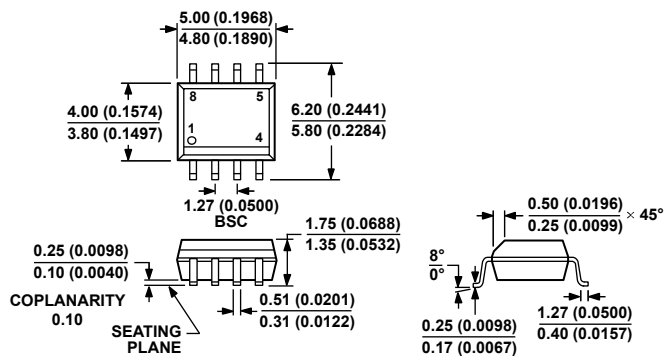


NOTES
1. MAXIMUM NUMBER OF NODES: 110.
2. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 31. Typical CAN Network

10029-029

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 32. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

012A07-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADM3051CRZ	−40°C to +125°C	8-Lead SOIC_N	R-8
ADM3051CRZ-RL7	−40°C to +125°C	8-Lead SOIC_N	R-8
EVAL-ADM3051EBZ		Evaluation Board	

¹ Z = RoHS Compliant Part.

NOTES