Input and Output Filters for Z-One™ POL Converters

Application Note

TABLE OF CONTENTS

Introduction

The Z-One™ Point Of Load (POL) converters are intelligent, fully programmable step-down point-of-load DC-DC modules integrating digital power conversion and intelligent power management. This application note focuses on just the input and output filtering considerations.

The POL converters have some on-board filtering, and some additional filtering components are typically placed on the customer's board as shown in Figure 1.

The Intermediate Bus Architecture (IBA) uses an isolated front-end converter to develop an Intermediate Bus Voltage (IBV) and non-isolated Point-Of-Load converters (POL's). With a non-isolated converter such as a POL, the internal switching waveforms are not in close proximity to chassis or isolated grounds, so common-mode noise issues typically do not arise with respect to the POLs. Therefore, this application note focuses on differential filtering. When used, common-mode filtering is typically placed at the front-end converter where noise coupling between grounds is possible.

The input and output filters affect the ripple, transient response, and stability of the POL converters. Possible reasons to deviate from the data sheet's recommended filter values are:

- Enhance the input/output ripple performance
- Enhance the transient performance
- Enhance stability
- Reduce cost
- Use preferred components

1. Gather Information

Before embarking on an input or output filter design, it is a good idea to gather the following information:

- Baseline data sheet ripple performance
- Load ripple requirements
- Inductance in the system (can cause stability issues)
- Noise sensitivity of the system
- Number of POL converters in the system

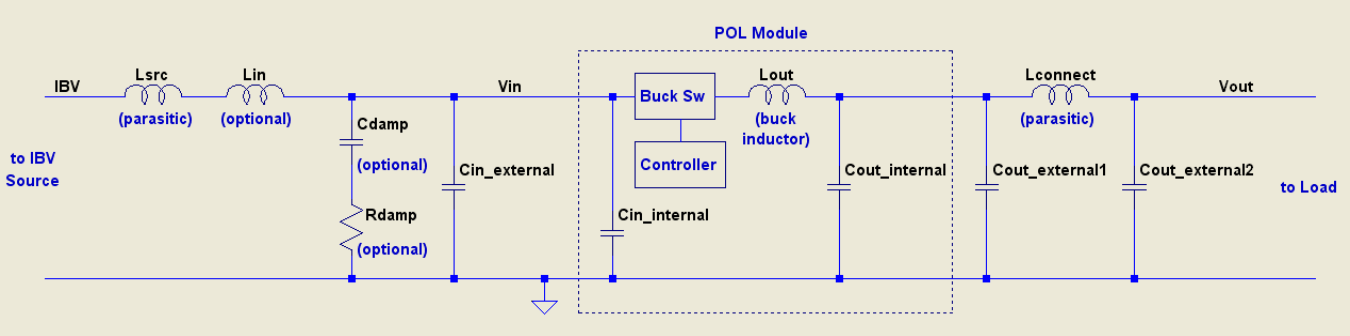


Figure 1. POL module and external filter components.

2. Input Filter Considerations

2.1 Input Filter Design Procedure

The input filter is there to control the input ripple and assure stability. Unlike the output filter, it does not help the transient response. In fact, it may even adversely affect the transient response or system stability if it is not designed properly. A common pitfall is to neglect to properly damp the input filter and fail to meet the Middlebrook Criterion described below.

2.2 Middlebrook Criterion

An important yet often overlooked aspect of input filter design is meeting the Middlebrook Criterion. A professor at Caltech named R.D. Middlebrook and his students extensively studied the phenomenon of input filter / converter interactions. He showed that under certain conditions, an input filter can cause a converter to become unstable. This can happen if the output impedance of the filter is higher than the input impedance of the converter. And even before a converter becomes unstable, its performance degrades significantly due to improperly designed input filter.

Within its control loop's bandwidth, the POL converter is a constant-power load and thus it presents a negative incremental impedance to the input filter (see Figure 2). This can move the poles of the L-C input filter into the right-half plane and cause oscillation.

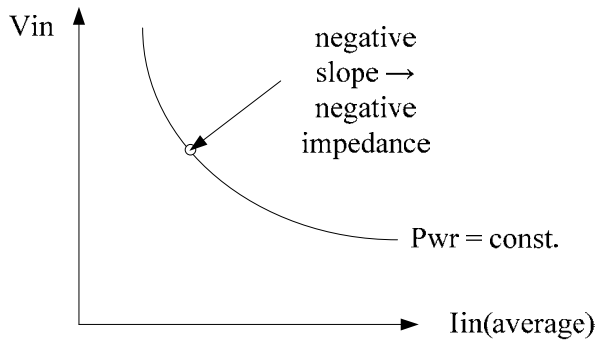


Figure 2. The input V-I characteristic of a converter.

To avoid this problem, there needs to be a separation between the impedance curves as shown in Figure 3. The recommended separation is at least 12 dB[1].

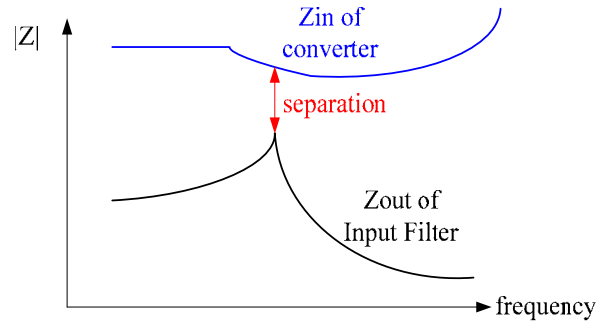


Figure 3. Separation of impedance curves.

Detailed calculation of the impedance curves is best done by SPICE simulation, but to get a rough idea of the separation in a proposed system, a few hand calculations can be performed.

[1] Where $dB(Z) = 20 \cdot \mathrm{Log}(Z)$

At low frequencies, the converter's input impedance is:

$$|Zin\_conv| = \frac{Vin\_DC^2}{Pout}[Ohms]$$
$$= \frac{Vin\_DC^2}{Vout\_DC \times Iout\_DC}[Ohms]$$

If critically damped, the peak output impedance of the input filter is:

$$|Zout\_filter| = \sqrt{\frac{Lin}{Cin}}[Ohms]$$

These values can quickly be checked to see if

$$|Zout\_filter| << |Zin\_conv|$$

The above expression is referred to as the Middlebrook Criterion. It can be seen that the larger Lin is, the larger Cin needs to be to meet this criterion. Also note that more Cin is required at lower input voltages and higher output powers. Input filter damping to avoid resonant peaking is also a key to reliably meeting the Middlebrook Criterion.

2.3 Determine Input Filter Topology

The minimum required filter uses only an input capacitor to control the ripple voltage at the POL converter. An optional input inductor may be used to further reduce IBV ripple by controlling the reflected ripple currents and thus preventing these currents from generating ripple across impedances in the distribution system. The damping capacitor and resistor damp the L-C ringing that occurs when the input inductor is used or when there is parasitic input inductance. Such ringing can degrade the performance of the POL converter or even make it oscillate. (See Middlebrook Criterion above.)

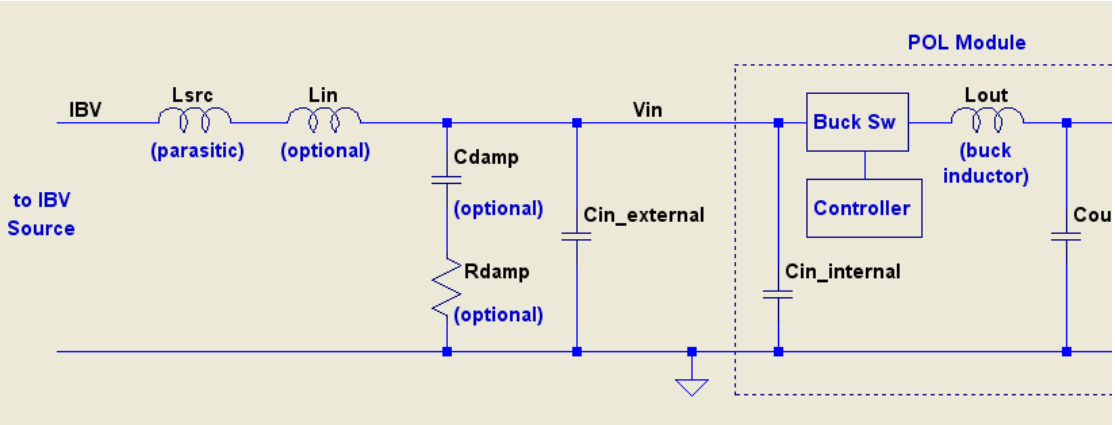


Figure 4. POL module and external input filter components

Use a capacitor-only input filter if:

- The system is cost sensitive
- POL converter is close to the IBV source

Use an L-C input filter if:

- Additional control of IBV voltage and current ripple are needed
- The IBV is distributed over a large distance
- The system is very noise sensitive

Use an input filter damper if:

- The filter includes an input inductor
- There is a need to tolerate parasitic input inductance
- The input source is off-board or far away
- The input voltage is relatively low and the output current is relatively high
- For more information, see the Middlebrook Criterion section

2.4 Interleaving

Z-One™ POL converters give system designers additional resources to reduce the input and output noise – switching frequency synchronization and interleaving. Interleaving means applying a phase shift between the switching actions of multiple POL converters. Calculation of ripple with interleaved POL converters is beyond the scope of this document, but the following scheme can be applied to optimize the interleaving. Interleaving should be applied so that the switching ripple tends to cancel. For paralleled POL converters, it is always optimal to have even spacing so their output ripple is minimized

e.g.,

$$\phi \text{ between parallel POLs} = \frac{360^\circ}{\text{number of POLs in parallel}}$$

To minimize the input ripple, the POL converters connected to each output bus should have a phase offset as a group so they don't switch current to the input bus at the same time. The optimality condition for minimizing input ripple is not as straight-forward, but a simple group offsetting scheme that greatly reduces input ripple is as follows:

$$\theta \text{ between output buses} = \frac{360^\circ}{\text{number of output buses}}$$

Also, a more complex scheme can be applied that takes into account the magnitudes of each load current. Input and output ripple are both minimized by applying the sum of the above two angles to each POL converter.

Tips on Interleaving:

- Use when there are multiple POL converters connected to the same input source
- The GUI's Design Wizard will automatically calculate values of phase shifts for each POL converter. See Figure 5.
- The input ripple improvements with interleaving depend on many factors, so the

filters designed in this document do not take interleaving into effect.

Figure 5. Design Wizard in the Graphical User Interface (GUI)

2.5 Input Filter Design Steps

(See Variables Defined)

1.) Calculate the duty cycle of the POL converter:

$$D = \frac{Vout\_DC}{Vin\_DC}$$

2.) Calculate the total input filter capacitance needed based on the required Vin_pk_pk ripple:

$$Cin = \frac{Iout\_DC \cdot D \cdot (1-D)}{Fsw \cdot Vin\_pk\_pk}$$

Use ~25% more capacitance than calculated to account for spikes and other noise.

3.) Calculate the filter inductance needed to meet Iin_pk_pk (if used):

$$Lin = \frac{Vin\_pk\_pk}{8 \cdot Fsw \cdot Iin\_pk\_pk}$$

4.) Find the maximum total inductance for which the Middlebrook Criterion must be met:

$$Lin\_total = Lin + Lsrc\_\max$$

5.) Calculate the Cin required based on meeting the Middlebrook Criterion:

5a.) Minimum input impedance of POL:

$$Zin\_\min = \frac{Vin\_DC^2}{Vout\_DC \times Iout\_DC\_\max}$$

5b.) Maximum output impedance of filter:

With damper, use 12dB separation

$$Zout\_\max = \frac{Zin\_\min}{4}$$

Without damper, use 26 dB separation or more

$$Zout\_\max = \frac{Zin\_\min}{20}$$

$$Cin = \frac{Lin\_total}{Zout\_\max^2}$$

6.) Choose the **larger** Cin from steps 2 and 5.

Deduct the input capacitance already in the POL converter.

$$Cin\_external = Cin - Cin\_internal$$

(See Onboard Capacitor and Inductor Table in Appendix)

Use 4.7µF as a minimum for Cin_external.

7.) Calculate the input damper capacitance and resistance (if used).

$$Cdamp \geq 4 \cdot Cin$$

$$Rdamp = \sqrt{\frac{Lin\_total}{Cin}}$$

2.6 Practical Considerations

- Place Cin_external as close to the POL as possible and minimize stray inductance by using wide traces or shapes and parallel planes
- Multi Layer Ceramic Chip (MLCC) capacitors are recommended for ripple filtering because of high ripple current rating and excellent high frequency performance

- X7R is the preferred dielectric because of good temperature and voltage coefficients
- X5R offers high capacitance, but capacitance decreases significantly above 50% of rated voltage, so carefully check the manufacturer's data.
- Derate tantalum capacitor voltages to 50% (max applied voltage = 50% of rated voltage)
- Other types of capacitors are typically derated to 75% of rated voltage (consult the manufacturer or in-house guidelines)
- Avoid MLCC capacitors larger than 1210 due to cracking issues
- Observe capacitor manufacturers' soldering and handling instructions
- For the damper, use a capacitor with an ESR = Rdamp and C >= Cdamp (tantalums are often used)
- Use damper resistor rated at 0.25W for non-pulsating load, 1 Watt for heavily pulsating load

2.7 Input Filter Design Example

Given, Vin_DC = 12 V, Vout_DC =3 V, Iout_DC = 15 A, and Fsw = 500 kHz, design an input filter for a ZY7115 POL to limit the peak-to-peak voltage and current ripple to 2% of their DC values. Design the filter to be stable with 0.1 µH of additional source inductance.

Vin_pk_pk = 2%·12 = 240 mV
$D = Vout\_DC/Vin\_DC$ = 3/12 = 0.25

Cin to meet Vin_pk_pk:
$Cin = Iout\_DC \cdot D \cdot (1-D)/(Fsw \cdot Vin\_pk\_pk)$
= 15·0.25·0.75/(500,000·0.24) = 23.4 µF

$Iin\_DC = Iout\_DC \cdot D$ = 15·0.25 = 3.75 Amps
Iin_pk_pk = 2%·3.75 = 75 mA
$Lin = Vin\_pk\_pk/(Iin\_pk\_pk \cdot 8 \cdot Fsw)$
Lin = 0.24/(0.075·8·500,000) = 0.8 µH

$Lin\_total = Lin + Lsrc\_max$
Lin_total = 0.8 µH + 0.1 µH = 0.9 µH

$$Zin\_\min = \frac{Vin\_DC^2}{Vout\_DC \times Iout\_DC\_\max}$$

$Zin\_min = 12^2/(3 \cdot 15)$ = 3.2 Ohms

$Zout\_max = Zin\_min/4$ = 0.8 Ohms

Cin to meet Middlebrook Criterion:

$$Cin = \frac{Lin\_total}{Zout\_\max^2}$$

Cin = 0.9 µH /((0.8 Ohms)^2) = 1.4 µF

Cin to meet Vin_pk_pk was 23.4 µF which is greater than the 1.4 µF to meet the Middlebrook Criterion, so use 23.4 µF.

$Cin\_external = Cin - Cin\_internal$
(See Onboard Capacitor and Inductor Table in Appendix)
$Cin\_external$ = 23.4 µF – 30 µF
$Cin\_external$ = (negative, so use minimum of 4.7 µF)

$Cdamp$ = 4· Cin = 93.8 µF

$$Rdamp = \sqrt{\frac{Lin\_total}{Cin}}$$

= 0.185 Ohms

In an actual implementation, the closest available component values would be chosen, but here we shall verify the ability of the formulas to achieve the desired results. Checking by SPICE simulation, Vin_pk_pk = 242 mV and Iin_pk_pk = 75.6 mA were obtained as shown in Figure 6 and Figure 7.

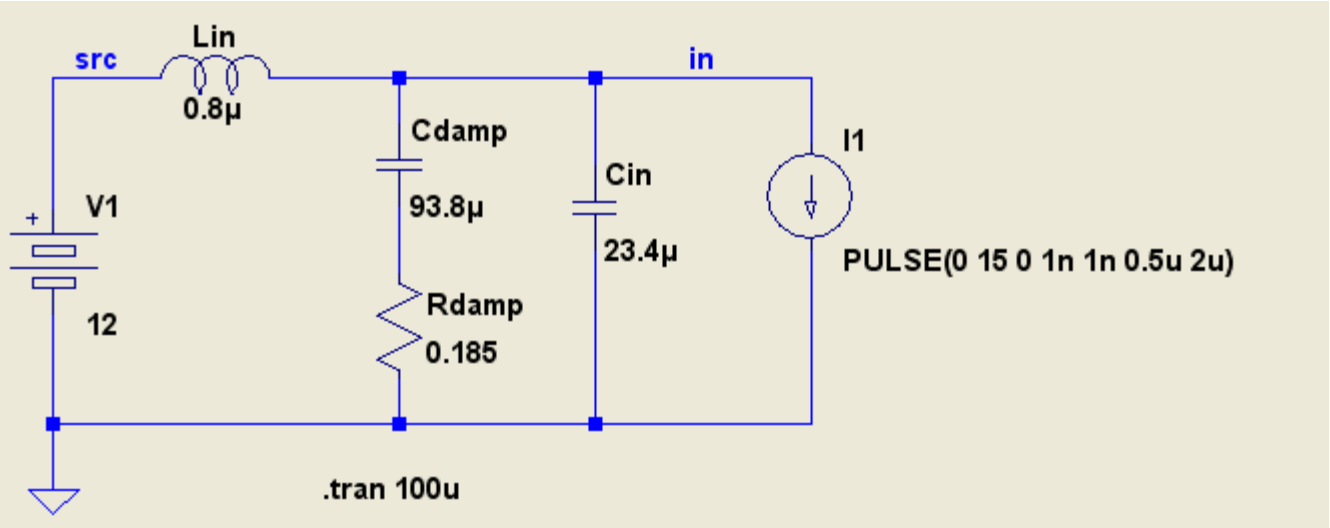


Figure 6. SPICE simulation schematic for input filter example

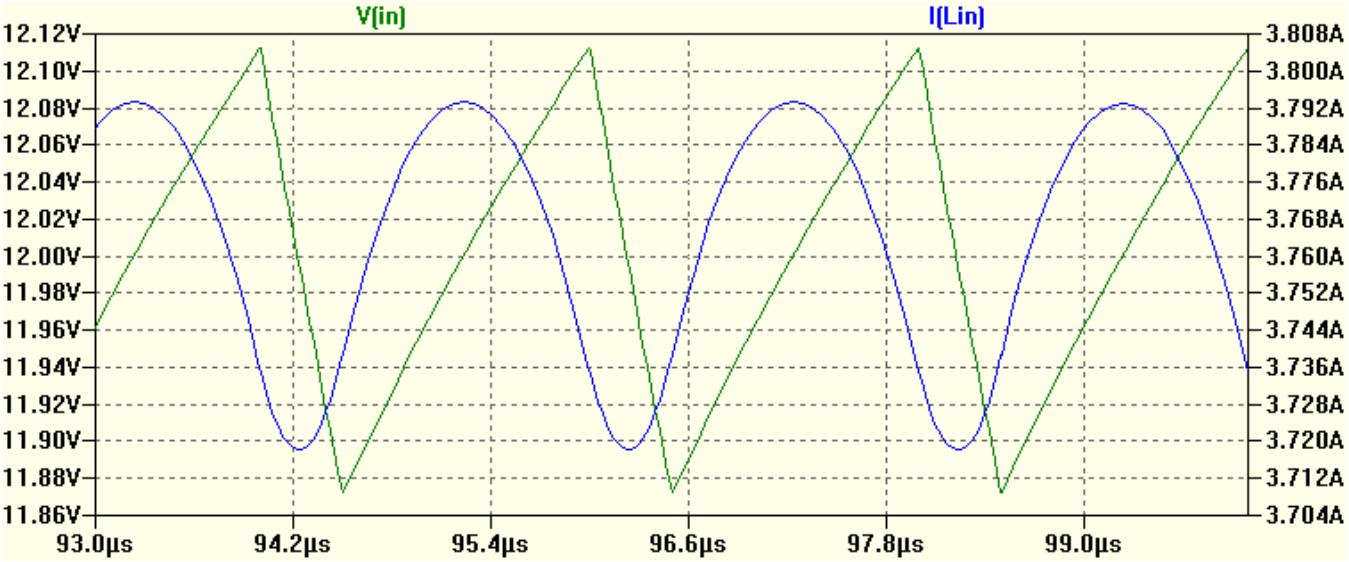


Figure 7. Simulation results for input filter example

3. Output Filter Considerations

3.1 Output Filter Design Procedure

The output filter determines the transient response of the POL converter as well as the output ripple and has a profound effect on control loop stability. Since the output filter in inside the feedback loop, the compensation poles and zeros of the PWM controller also play an important role in the stability of the POL converter.

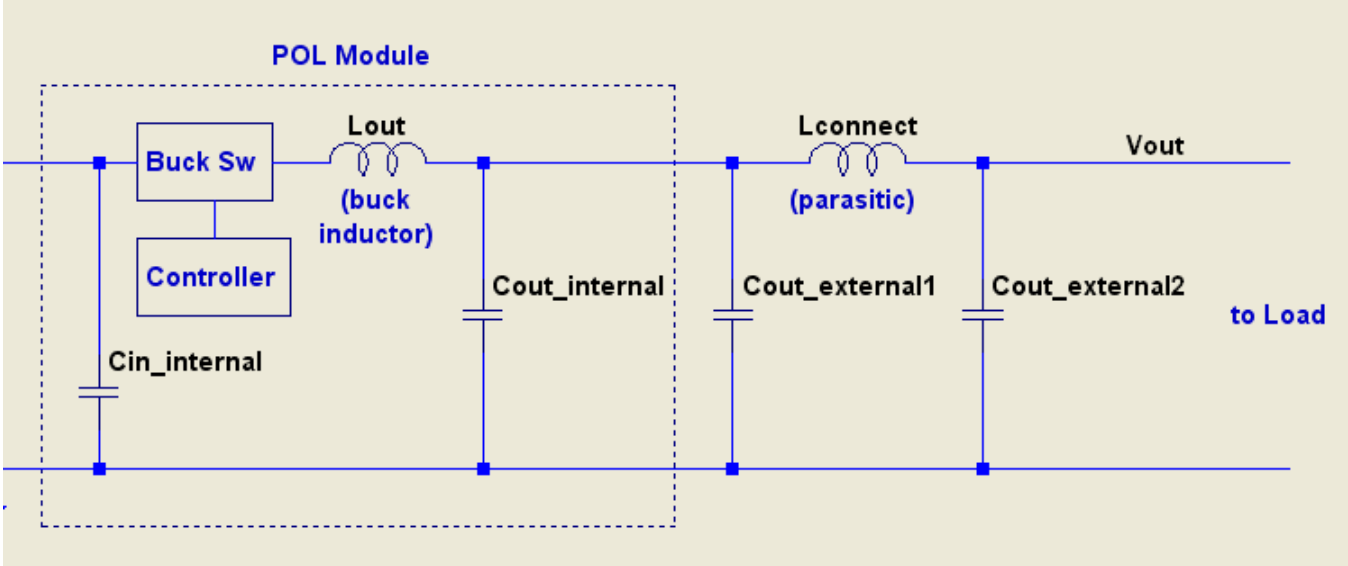


Figure 8. POL module and external output filter components.

3.2 Output Filter Topology

As shown in Figure 8, the output filter consists of a low-pass LC filter formed by the buck inductor and ceramic capacitors internal to the POL converter and some additional capacitors added externally. External capacitors are generally placed near the POL converter and near the load so Figure 8 shows some parasitic interconnect inductance between the two groups. A small inductance (~Lout/10) may be intentionally placed between the two groups of external capacitance to improve the output ripple.

The waveform coming out of the Buck Switch is a square wave with amplitude equal to the input voltage and an average value equal to the output voltage (see Synchronous Buck Waveforms). The output filter provides two distinct functions: 1.) it greatly reduces the switching ripple and 2.) it provides transient currents to the load.

To aid in design, both of these functions can be viewed in terms of impedance. The impedance at the loop crossover frequency determines the transient response while the impedance at the switching frequency determines the output ripple.

The equation below shows how the loop gain reduces the open loop output impedance of the converter, which is mainly due to the impedance of the output capacitors.

$$Zout\_closed\_loop = \frac{Zout\_open\_loop}{1 + loop\_gain}$$

The loop gain can be examined in the PWM controller window of the GUI as shown in Figure 9. The loop gain is large at low frequencies, gets smaller at higher frequencies, and eventually becomes less than 0 dB. The frequency where the loop gain crosses 0 dB is called the crossover frequency (or open loop bandwidth) and is a key parameter. Once the loop gain crosses over and becomes small, Zout_closed_loop ≅ Zout_open_loop and thus becomes just the impedance of the output capacitors. Conversely, Zout_closed_loop is reduced below crossover where the gain is large.

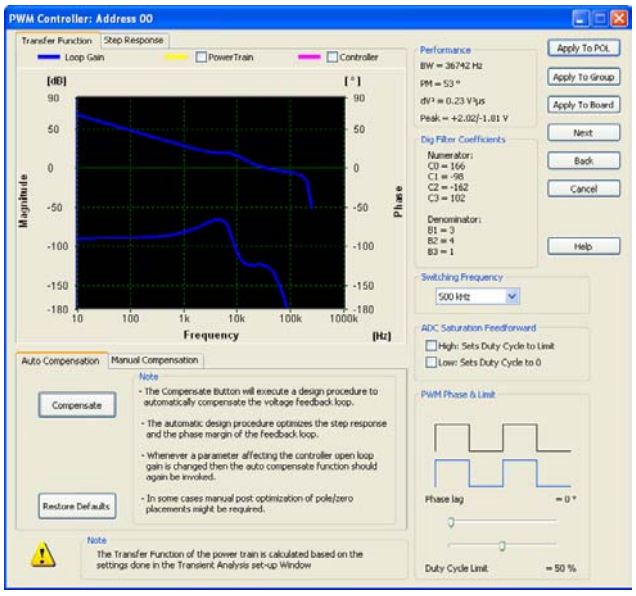


Figure 9. The PWM Controller window in the GUI. The top curve is Loop Gain and the bottom curve is Phase.

As shown in Figure 10, **Zout_max, occurs approximately at the loop crossover frequency.** Zout_max determines the transient response because for a step of current,

$$\Delta Vout \approx \Delta Iout \cdot Zout\_max$$

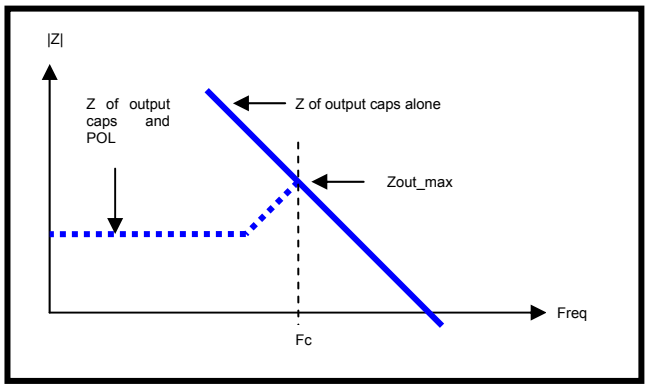


Figure 10. Output impedance with loop open and closed.

3.3 Filter Design for Output Ripple

1.) Calculate the duty cycle of the POL converter:

$$D = \frac{Vout\_DC}{Vin\_DC}$$

2.) Calculate the output ripple filter capacitance needed based on the required Vout_pk_pk ripple:

$$Cout\_ripple = \frac{Vin\_DC \cdot D \cdot (1-D)}{8 \cdot Lout \cdot Vout\_pk\_pk \cdot Fsw^2}$$

(See Onboard Capacitor and Inductor Table in Appendix)

Use ~25% more capacitance than calculated to account for spikes and other noise.

3.) Deduct the output capacitance already in the POL

$$Cout\_external1 = Cout\_ripple - Cout\_internal$$

(See Onboard Capacitor and Inductor Table in Appendix)

Use a 4.7 µF ceramic capacitor as a minimum. In general, Multilayer Ceramic Chip (MLCC) capacitors are recommended for ripple filtering because of high ripple current rating and excellent high frequency performance.

3.4 Filter Design for Transient Response

1.) Calculate Zout_max based on desired transient response.

$$Zout\_\max = \frac{\Delta Vout\_allowed}{\Delta Iout\_\max\_step}$$

2.) Choose Cout to have an impedance of less than Zout_max at the loop cross-over frequency, Fc. Assume an initial Fc of 20 kHz.

$$Cout\_\min = \frac{1}{Zout\_\max \cdot 2 \cdot \pi \cdot Fc}$$

$$ESR\_max = Zout\_max$$

3.) Determine the additional capacitance to meet the transient requirement:

$$Cout\_external2 = Cout\_min - Cout\_internal - Cout\_external1$$

Use 110 µF for Cout_external2 as a minimum. Cout should meet or exceed the above requirements including some room for tolerances.

Various types of capacitors (such as ceramic, tantalum, OSCON, SP etc.) can be combined to meet the transient requirement as shown in Figure 11.

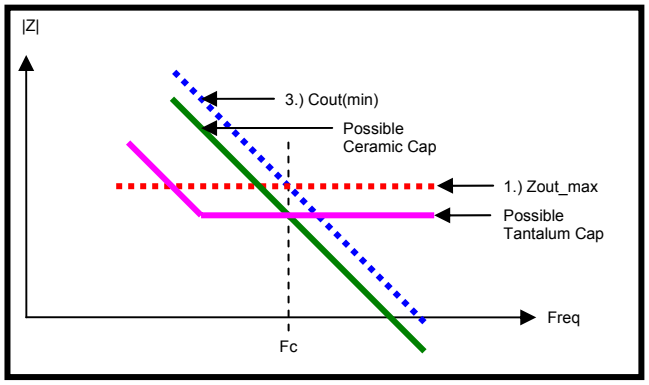


Figure 11. Impedance requirements for transient response

4.) Enter the chosen capacitor's parameters into the GUI's Transient Simulation window. See Figure 12.

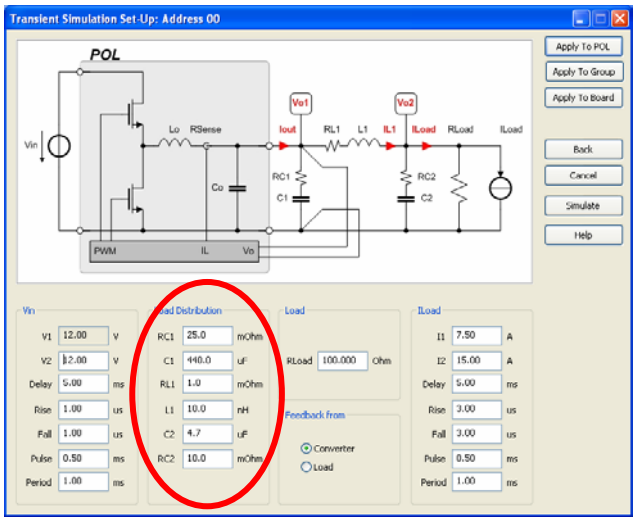


Figure 12. Capacitor parameter fields in the Transient Simulation window.

5.) Using the GUI's PWM Controller window, perform an auto-compensation or manually adjust compensation to get the desired crossover frequency (bandwidth) and a phase margin of at least 45 degrees. See Figure 13. If the desired bandwidth can not be obtained, iterate the design using the attained bandwidth.

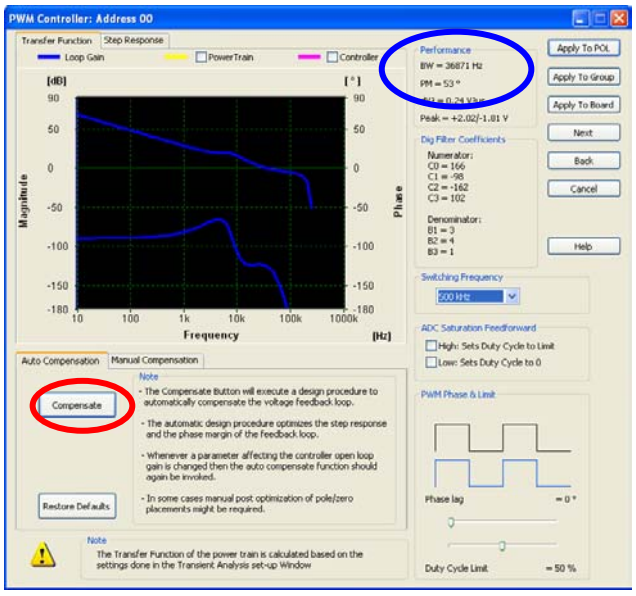


Figure 13. Red: Auto-Compensate button in the PWM Controller window. Blue: Bandwidth and Phase margin.

3.5 Practical Considerations

- Place Cout_external1 as close to the POL converter as possible and minimize stray inductance by using wide traces or shapes and parallel planes
- Multi Layer Ceramic Chip (MLCC) capacitors are recommended for ripple filtering because of high ripple current rating and excellent high frequency performance
- X7R is the preferred MLCC dielectric because of good temperature and voltage coefficients
- X5R offers high capacitance, but capacitance decreases significantly above 50% of rated voltage, so carefully check the manufacture's data.
- Derate tantalum capacitor voltages to 50% (max applied voltage = 50% of rated voltage)
- Other types of capacitors are typically derated to 75% of rated voltage (consult the manufacturer or in-house guidelines)
- Avoid MLCC capacitors larger than 1210 due to cracking issues
- Observe capacitor manufacturers' soldering and handling instructions

3.6 Output Filter Design Example

Given, Vin_DC = 12 V, Vout_DC =3 V, and Fsw = 500 kHz, design an output filter for a ZY7115 POL to limit the peak-to-peak output voltage ripple to 2% of

its DC value and limit the transient ΔVout to 5% of its DC value for a 50% load step.

Ripple: $Vout\_pk\_pk = 2\% \cdot 3\ V = 60\ mV$
Transient: $\Delta Vout\_allowed = 5\% \cdot 3\ V = 150\ mV$

$D = Vout\_DC/Vin\_DC = 3/12 = 0.25$

$$Cout\_ripple = \frac{Vin\_DC \cdot D \cdot (1-D)}{8 \cdot Lout \cdot Vout\_pk\_pk \cdot Fsw^2}$$
$$= \frac{12 \cdot 0.25 \cdot 0.75}{8 \cdot 0.75 \cdot 10^{-6} \cdot 0.06 \cdot 500000^2}$$
$= 25\ \mu F$

$Cout\_external1 = Cout\_ripple - Cout\_internal$
$= 25\ \mu F - 30\ \mu F$
(See Onboard Capacitor and Inductor Table in Appendix)
= negative, so use 4.7 µF X7R ceramic at POL

$$Zout\_max = \frac{\Delta Vout\_allowed}{\Delta Iout\_max\_step}$$
$= 150\ mV / 7.5\ A = 20$ milliohms

$Cout\_min = 1 / (Zout\_max \cdot 2 \cdot \pi \cdot Fc)$
$= 1 / (0.02 \cdot 2 \cdot \pi \cdot 20\ kHz)$
$= 398\ \mu F$

$ESR\_max = Zout\_max$
$= 20$ milliohms

$Cout\_external2 = Cout\_min - Cout\_internal - Cout\_external1$
$= 398\ \mu F - 4.7\ \mu F - 30\ \mu F$
$= 363\ \mu F$

Use 5x 100 µF 6.3 V X5R ceramic capacitors at the load. Vendor data shows these loose 17% of rated capacitance at 3 V bias, so this gives 415 µF.

Upon entering these values into the GUI and performing auto-compensation, Fc (called BW or Bandwidth in the GUI) was 23 kHz and the Phase Margin was 46 degrees. Since the actual Fc was higher than the target value of 20 kHz, the performance should be better. As shown in Figure 14, transient simulation in the GUI resulted in a Vout_pk_pk ripple of 50 mV and a ΔVout of 101 mV for a 7.5 Amp current step. The ripple and transient response are slightly better than required.

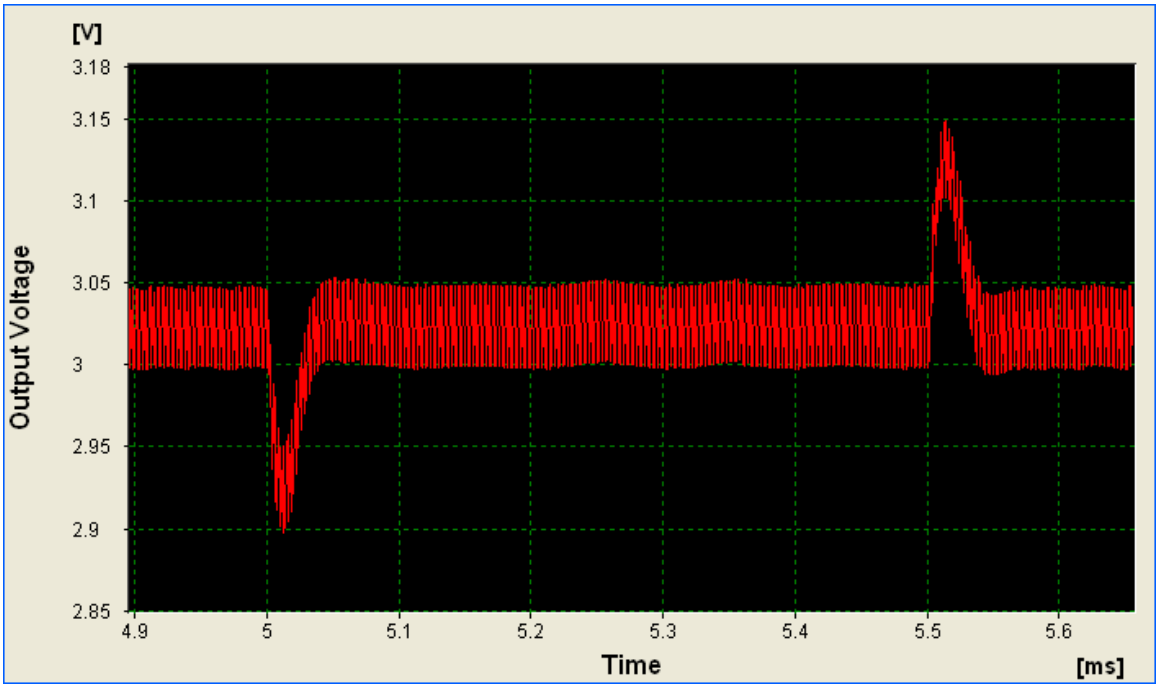


Figure 14. Simulation results for output filter example showing the ripple, undershoot, and overshoot due to the 7.5 Amp current step (loading and unloading).

4. Filter Design Tool

An Excel-based design tool is available to assist in designing the input and output filters. It is available on the Power-One website at:

http://www.power-one.com/resources/products/appnote/z_inoutfilters_designtool.exe

Download and run the executable file to install the design tool.

A screen shot of the design tool is shown in Figure 15.

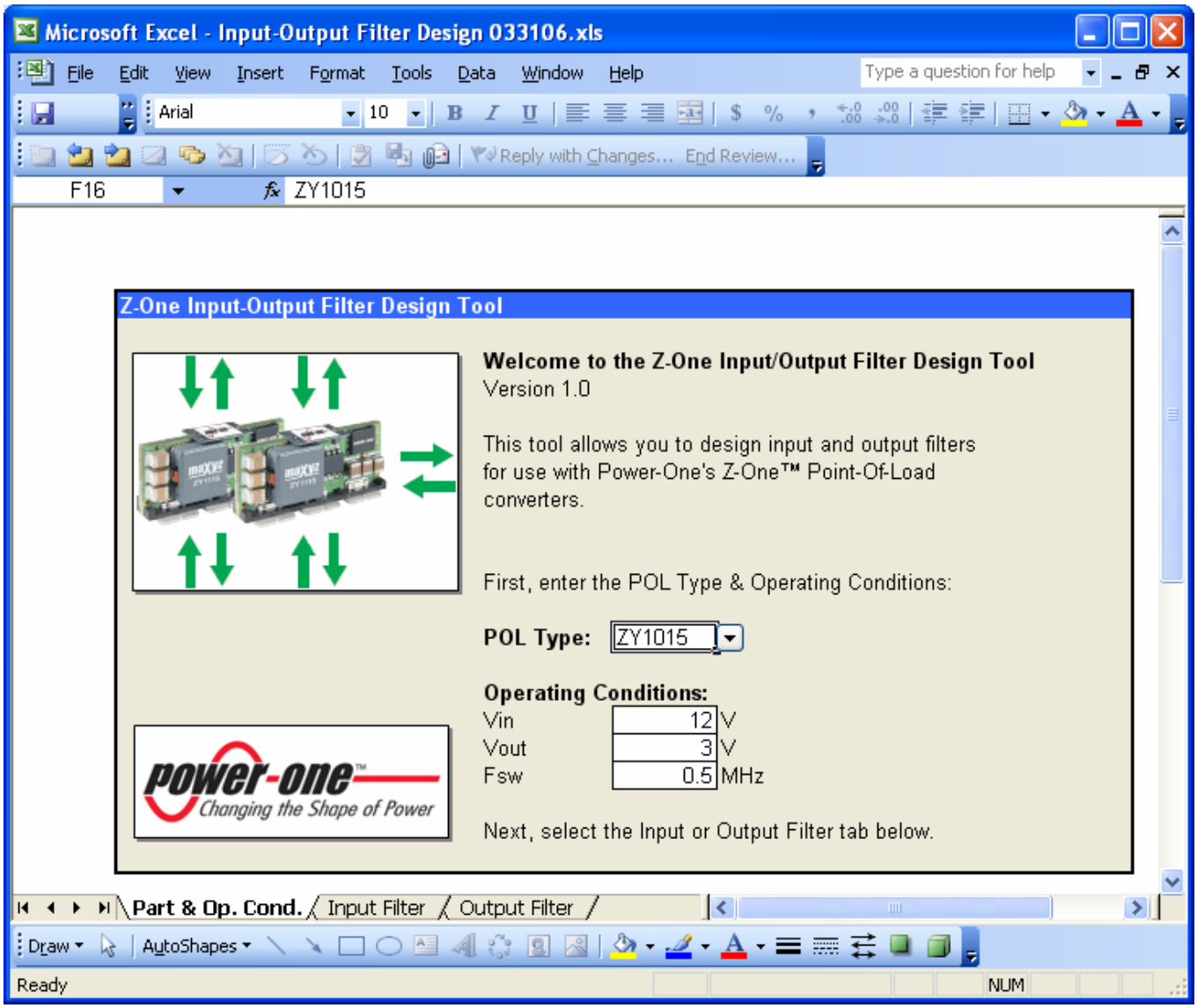
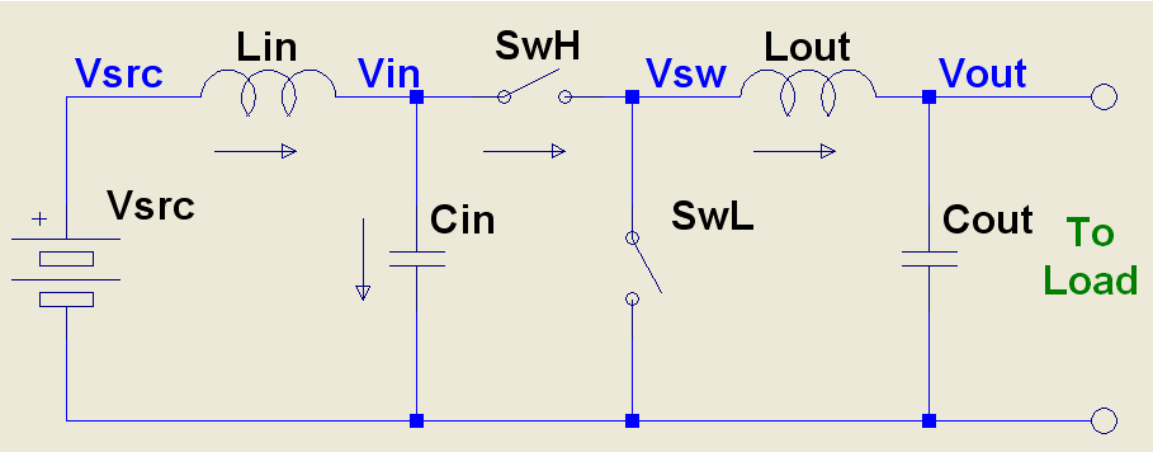
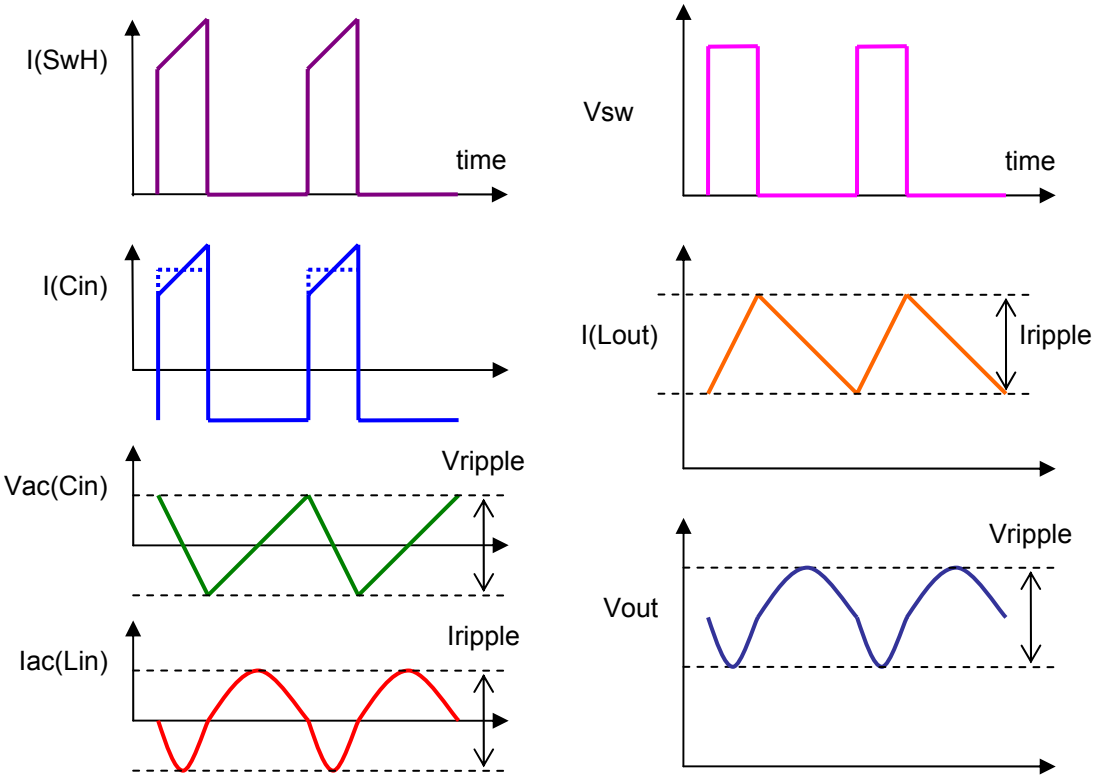


Figure 15. Input/Output filter design tool.

5. Appendices

5.1 Synchronous Buck Waveforms





(not to scale)

5.2 Onboard Capacitor and Inductor Table

POL	Cin [µF]	Lout [µH]	Cout [µF]	Vin [mV] pk_pk (1), (2)	Vout [mV] pk_pk (1), (2)
ZY1207	10	0.82	44	231	27
ZY1015	30	0.7	30	165	47
ZY1115	30	0.75	30	165	44
ZY1120	30	0.7	30	220	47
ZY7007	10	0.68	44	231	33
ZY7010	30	0.68	44	110	33
ZY7015	30	0.75	30	165	44
ZY7115	30	0.75	30	165	44
ZY7120	30	0.7	30	220	47

Notes:
(1) Calculated ripple with no added capacitors
(2) Conditions: Vin=12, Vout=2.5, Iout=Irated, Fsw=500 kHz

5.3 Key Formulas

Buck Converter Duty Cycle:

$$D = \frac{Vout\_DC}{Vin\_DC}$$

Input Filter:

Use the larger of the following two Cin values:

$$Cin = \frac{Iout\_DC \cdot D \cdot (1-D)}{Fsw \cdot Vin\_pk\_pk}$$

$$Cin = \frac{Lin\_total}{Zout\_\max^2}$$

$$Cin\_external = Cin - Cin\_internal$$

$$Lin = \frac{Vin\_pk\_pk}{8 \cdot Fsw \cdot Iin\_pk\_pk}$$

$$Lin\_total = Lin + Lsrc\_\max$$

$$Zin\_\min = \frac{Vin\_DC^2}{Vout\_DC \times Iout\_DC\_\max}$$

With damper, use 12dB separation:

$$Zout\_\max = \frac{Zin\_\min}{4}$$

Without damper, use 26 dB separation or more:

$$Zout\_\max = \frac{Zin\_\min}{20}$$

$$Cdamp \geq 4 \cdot Cin$$

$$Rdamp = \sqrt{\frac{Lin\_total}{Cin}}$$

Output Filter:

$$Cout\_ripple = \frac{Vin\_DC \cdot D \cdot (1-D)}{8 \cdot Lout \cdot Vout\_pk\_pk \cdot Fsw^2}$$

$$Cout\_external1 = Cout\_ripple - Cout\_internal$$

$$Zout\_\max = \frac{\Delta Vout\_allowed}{\Delta Iout\_\max\_step}$$

$$Cout\_\min = \frac{1}{Zout\_\max \cdot 2 \cdot \pi \cdot Fc}$$

$$ESR\_max = Zout\_max$$

$$Cout\_external2 = Cout\_min - Cout\_internal - Cout\_external1$$

5.4 Units

Unless otherwise stated, SI units are used in all calculations. (E.g., Volts, Amps, Hertz, Farads, Henries, Watts, Ohms, Seconds, etc.)

5.5 Variables Defined

|Zin_conv| = magnitude of converter's input impedance
|Zout_filter| = magnitude of filter's out impedance
Cdamp = input filter damping capacitance
Cin = input filter capacitance (not including Cdamp)
Cin_external = input filter capacitance external to POL module
Cin_internal = input filter capacitance internal to POL module
Cout_internal = internal output capacitance
Cout_min = minimum output capacitance to meet transient spec
Cout_external1 = external output capacitance 1 (near POL module)
Cout_external2 = external output capacitance 2
Cout_ripple = output capacitance required to meet ripple spec
D = duty cycle of buck converter
ESR_max = maximum ESR of output capacitance to meet transient spec
Fsw = switching frequency of buck converter
Iin_pk_pk = peak to peak input ripple current
Iout_DC = DC output current
Lin = input filter inductance
Lout = buck output inductor
Pout = output power
Rdamp = input filter damping resistance
Vin_DC = DC input voltage
Vin_pk_pk = peak to peak input ripple voltage
Vout_DC = DC output voltage
Vout_pk_pk = peak to peak output ripple voltage
Zout_max = maximum output impedance to meet transient spec
ΔIout_max_step = maximum transient step load change
ΔVout_allowed = allowed transient output voltage change

5.6 Glossary

GUI – Graphical User Interface
IBV – Intermediate Bus Voltage
MLCC capacitor – Multi Layer Ceramic Chip capacitor
POL – Point-Of-Load
SPICE – Simulation Program with Integrated Circuit Emphasis

5.7 References

[1] Erickson, Robert W. and Dragan Maksimovic, Fundamentals of Power Electronics, 2nd ed.; Norwell, Mass.: Kluwer Academic, 2001, 883 p. ISBN: 0792372700

[2] Jerrold Foutz, Input Filter Interaction With Switching-Mode Power Supplies: http://www.smpstech.com/filter00.htm

[3] Middlebrook, R. D., Input Filter Considerations in Design and Application of Switching Regulators, IEEE Industry Applications Society Annual Meeting, October 11-14, 1976, Chicago, IL. IAS Republished in Advances in Switch-Mode Power Conversion, Volumes I and II, 2nd edition, TESLAco, 1983, paper 7, pp. 91-107.