

# DATA SHEET

## **74LVC138A**

3-to-8 line decoder/demultiplexer;  
inverting

Product specification

1998 Apr 28

# 3-to-8 line decoder/demultiplexer; inverting

# 74LVC138A

## FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85°C

## DESCRIPTION

The 74LVC138A is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC138A accepts three binary weighted address inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and when enabled, provides 8 mutually exclusive active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_7$ ).

The 74LVC138A features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH ( $E_3$ ). Every output will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH.

This multiple enable function allows easy parallel expansion of the 74LV138A to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138A ICs and one inverter. The 74LV138A can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

| SYMBOL            | PARAMETER   | CONDITIONS                         | TYPICAL    | UNIT |
|-------------------|---|------------------------------------|------------|------|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>An to $\bar{Y}_n$ ,<br>$E_3$ to $\bar{Y}_n$ , $\bar{E}_n$ to $\bar{Y}_n$ | $C_L = 50$ pF;<br>$V_{CC} = 3.3$ V | 3.5<br>3.5 | ns   |
| $C_I$             | Input capacitance   |                                    | 5.0        | pF   |
| $C_{PD}$          | Power dissipation capacitance per package   | $V_{CC} = 3.3$ V<br>Notes 1 and 2  | 44         | pF   |

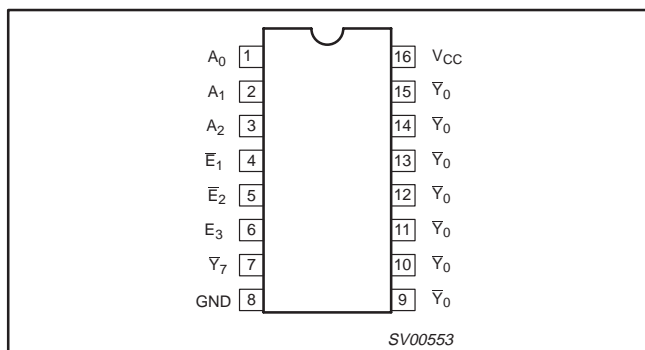
### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$

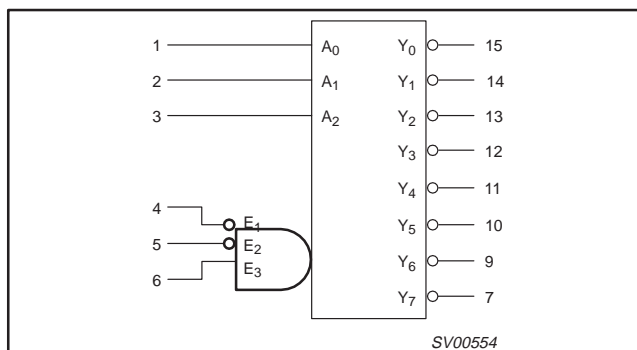
## ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA  | PKG. DWG. # |
|-----------------------------|-------------------|-----------------------|----------------|-------------|
| 16-Pin Plastic SO           | -40°C to +85°C    | 74LVC138A D           | 74LVC138A D    | SOT109-1    |
| 16-Pin Plastic SSOP Type II | -40°C to +85°C    | 74LVC138A DB          | 74LVC138A DB   | SOT338-1    |
| 16-Pin Plastic TSSOP Type I | -40°C to +85°C    | 74LVC138A PW          | 74LVC138APW DH | SOT403-1    |

## PIN CONFIGURATION



## LOGIC DIAGRAM



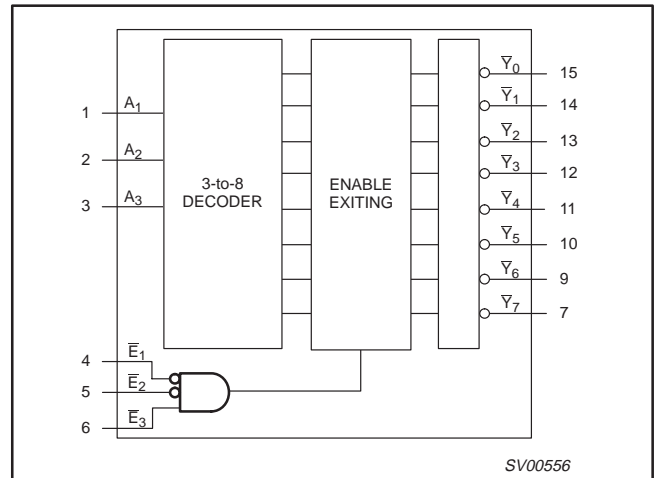
# 3-to-8 line decoder/demultiplexer; inverting

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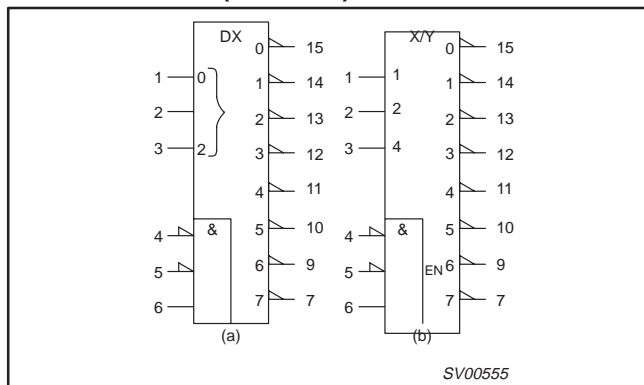
### PIN DESCRIPTION

| PIN NUMBER                   | SYMBOL                     | NAME AND FUNCTION           |
|------------------------------|----------------------------|-----------------------------|
| 1, 2, 3                      | $A_0$ to $A_2$             | Address inputs              |
| 4, 5                         | $\bar{E}_1, \bar{E}_2$     | Enable inputs (active LOW)  |
| 6                            | $E_3$                      | Enable inputs (active HIGH) |
| 15, 14, 13, 12, 11, 10, 9, 7 | $\bar{Y}_0$ to $\bar{Y}_7$ | Outputs                     |
| 8                            | GND                        | Ground (0 V)                |
| 16                           | $V_{CC}$                   | Positive supply voltage     |

### FUNCTIONAL DIAGRAM



### LOGIC SYMBOL (IEEE/IEC)



### FUNCTION TABLE

| INPUTS      |             |       |       |       |       | OUTPUTS     |             |             |             |             |             |             |             |
|-------------|-------------|-------|-------|-------|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| $\bar{E}_1$ | $\bar{E}_2$ | $E_3$ | $A_0$ | $A_1$ | $A_2$ | $\bar{Y}_0$ | $\bar{Y}_1$ | $\bar{Y}_2$ | $\bar{Y}_3$ | $\bar{Y}_4$ | $\bar{Y}_5$ | $\bar{Y}_6$ | $\bar{Y}_7$ |
| H           | X           | X     | X     | X     | X     | H           | H           | H           | H           | H           | H           | H           | H           |
| X           | H           | X     | X     | X     | X     | H           | H           | H           | H           | H           | H           | H           | H           |
| X           | X           | L     | X     | X     | X     | H           | H           | H           | H           | H           | H           | H           | H           |
| L           | L           | H     | L     | L     | L     | L           | H           | H           | H           | H           | H           | H           | H           |
| L           | L           | H     | H     | L     | L     | H           | L           | H           | H           | H           | H           | H           | H           |
| L           | L           | H     | L     | H     | L     | H           | H           | L           | H           | H           | H           | H           | H           |
| L           | L           | H     | H     | H     | L     | H           | H           | H           | L           | H           | H           | H           | H           |
| L           | L           | H     | H     | L     | H     | H           | H           | H           | H           | L           | H           | H           | H           |
| L           | L           | H     | L     | H     | H     | H           | H           | H           | H           | H           | L           | H           | H           |
| L           | L           | H     | H     | H     | H     | H           | H           | H           | H           | H           | H           | L           | H           |

#### NOTES:

H = HIGH voltage level

L = LOW voltage level

X = don't care

## 3-to-8 line decoder/demultiplexer; inverting

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER   | CONDITIONS   | LIMITS |          | UNIT |
|------------|---|--|--------|----------|------|
|            |   |  | MIN    | MAX      |      |
| $V_{CC}$   | DC supply voltage (for max. speed performance)    |  | 2.7    | 3.6      | V    |
|            | DC supply voltage (for low-voltage applications)  |  | 1.2    | 3.6      |      |
| $V_I$      | DC input voltage range                            |  | 0      | 5.5      | V    |
| $V_{I/O}$  | DC output voltage range; output HIGH or LOW state |  | 0      | $V_{CC}$ | V    |
|            | DC input voltage range; output 3-State            |  | 0      | 5.5      |      |
| $T_{amb}$  | Operating free-air temperature range              |  | -40    | +85      | °C   |
| $t_r, t_f$ | Input rise and fall times                         | $V_{CC} = 1.2$ to $2.7V$<br>$V_{CC} = 2.7$ to $3.6V$ | 0      | 20<br>10 | ns/V |

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).  
Voltages are referenced to GND (ground = 0V).

| SYMBOL            | PARAMETER   | CONDITIONS   | RATING                 | UNIT |
|-------------------|---|--|------------------------|------|
| $V_{CC}$          | DC supply voltage   |  | -0.5 to +6.5           | V    |
| $I_{IK}$          | DC input diode current  | $V_I < 0$  | -50                    | mA   |
| $V_I$             | DC input voltage  | Note 2   | -0.5 to +6.5           | V    |
| $I_{OK}$          | DC output diode current   | $V_O > V_{CC}$ or $V_O < 0$  | ± 50                   | mA   |
| $V_{I/O}$         | DC output voltage; output HIGH or LOW                                   | Note 2   | -0.5 to $V_{CC} + 0.5$ | V    |
|                   | DC input voltage; output 3-State  | Note 2   | -0.5 to 6.5            |      |
| $I_O$             | DC output source or sink current  | $V_O = 0$ to $V_{CC}$  | ± 50                   | mA   |
| $I_{GND}, I_{CC}$ | DC $V_{CC}$ or GND current  |  | ± 100                  | mA   |
| $T_{stg}$         | Storage temperature range   |  | -65 to +150            | °C   |
| $P_{TOT}$         | Power dissipation per package   |  |                        |      |
|                   | - plastic mini-pack (SO)<br>- plastic shrink mini-pack (SSOP and TSSOP) | above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | 500<br>500             | mW   |

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

| SYMBOL           | PARAMETER   | TEST CONDITIONS   | LIMITS                |                  |      | UNIT |
|------------------|---|---|-----------------------|------------------|------|------|
|                  |   |   | Temp = -40°C to +85°C |                  |      |      |
|                  |   |   | MIN                   | TYP <sup>1</sup> | MAX  |      |
| V <sub>IH</sub>  | HIGH level input voltage                          | V <sub>CC</sub> = 1.2V  | V <sub>CC</sub>       |                  |      | V    |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   | 2.0                   |                  |      |      |
| V <sub>IL</sub>  | LOW level input voltage                           | V <sub>CC</sub> = 1.2V  |                       |                  | GND  | V    |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   |                       |                  | 0.8  |      |
| V <sub>OH</sub>  | HIGH level output voltage                         | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA  | V <sub>CC</sub> - 0.5 |                  |      | V    |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA | V <sub>CC</sub> - 0.2 | V <sub>CC</sub>  |      |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA  | V <sub>CC</sub> - 0.6 |                  |      |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA  | V <sub>CC</sub> - 1.0 |                  |      |      |
| V <sub>OL</sub>  | LOW level output voltage                          | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA   |                       |                  | 0.40 | V    |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA  |                       | GND              | 0.20 |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA   |                       |                  | 0.55 |      |
| I <sub>I</sub>   | Input leakage current                             | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND  |                       | ±0.1             | ±5   | μA   |
| I <sub>CC</sub>  | Quiescent supply current                          | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                   |                       | 0.1              | 10   | μA   |
| ΔI <sub>CC</sub> | Additional quiescent supply current per input pin | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0           |                       | 5                | 500  | μA   |

**NOTE:**1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.**AC CHARACTERISTICS**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C

| SYMBOL                             | PARAMETER  | WAVEFORM    | LIMITS                       |                  |     |                        |     | UNIT |
|------------------------------------|--|-------------|------------------------------|------------------|-----|------------------------|-----|------|
|                                    |  |             | V <sub>CC</sub> = 3.3V ±0.3V |                  |     | V <sub>CC</sub> = 2.7V |     |      |
|                                    |  |             | MIN                          | TYP <sup>1</sup> | MAX | MIN                    | MAX |      |
| t <sub>PHL</sub> /t <sub>PLH</sub> | Propagation delay<br>A <sub>n</sub> to $\bar{Y}_n$ | Figure 1, 3 | 1.5                          | 3.5              | 5.8 | 1.5                    | 6.8 | ns   |
| t <sub>PHL</sub> /t <sub>PLH</sub> | Propagation delay<br>E <sub>3</sub> to $\bar{Y}_n$ | Figure 1, 3 | 1.5                          | 3.6              | 5.8 | 1.5                    | 6.8 | ns   |
| t <sub>PHL</sub> /t <sub>PLH</sub> | Propagation delay<br>E <sub>n</sub> to $\bar{Y}_n$ | Figure 2, 3 | 1.5                          | 3.5              | 5.8 | 1.5                    | 6.8 | ns   |

**NOTE:**1. These typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

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## AC WAVEFORMS

$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$

$V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7\text{ V}$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

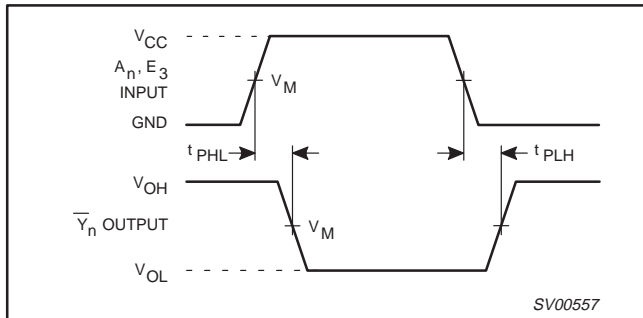


Figure 1. Input (nA) to output (nY) propagation delays.

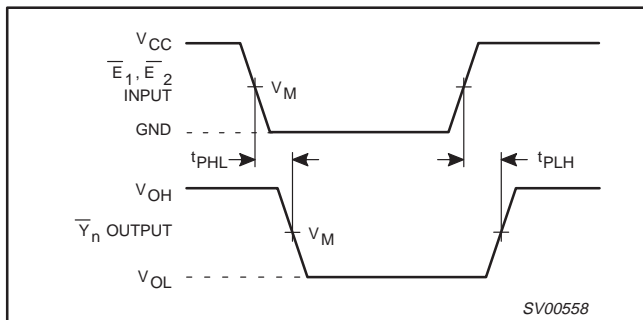


Figure 2. 3-State enable and disable times.

## TEST CIRCUIT

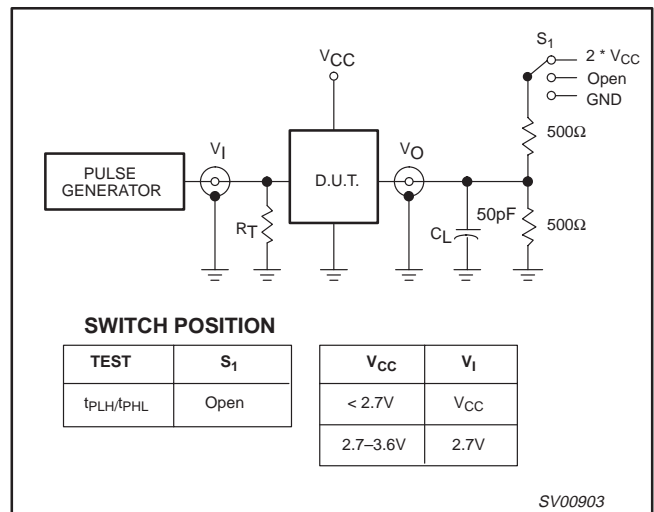


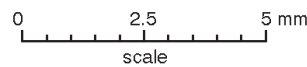
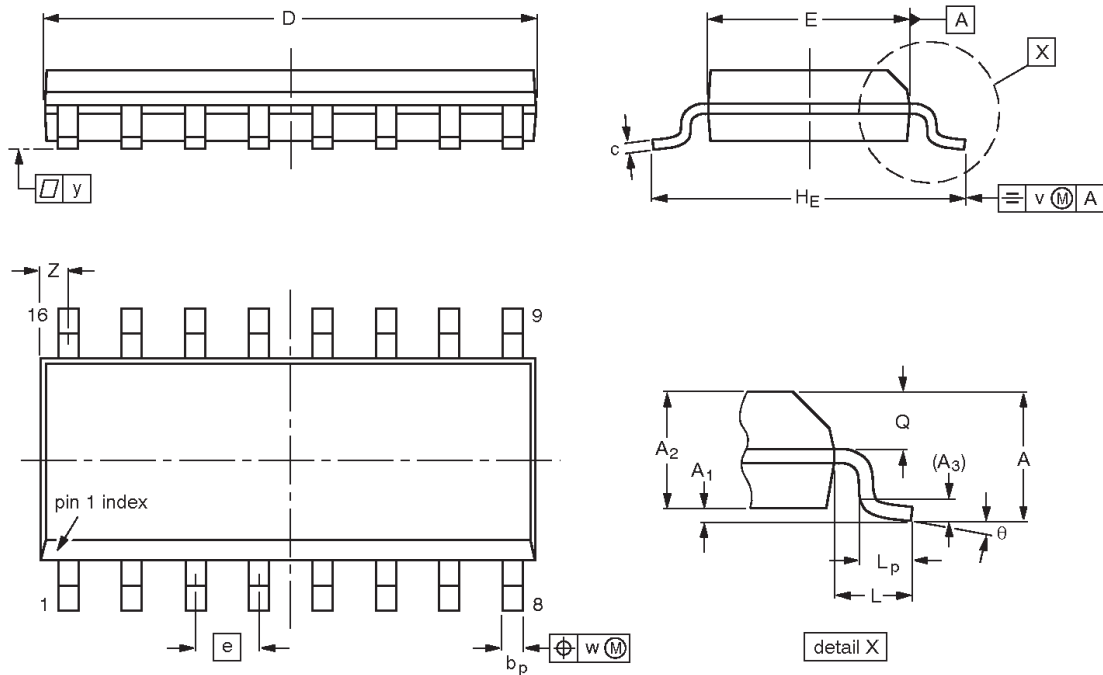
Figure 3. Load circuitry for switching times.

3-to-8 line decoder/demultiplexer; inverting

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max.         | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c                | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75<br>0.10   | 0.25<br>1.25   | 1.45<br>0.049  | 0.25           | 0.49<br>0.36   | 0.25<br>0.19     | 10.0<br>9.8      | 4.0<br>3.8       | 1.27  | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069<br>0.004 | 0.010<br>0.049 | 0.057<br>0.014 | 0.01           | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38     | 0.16<br>0.15     | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

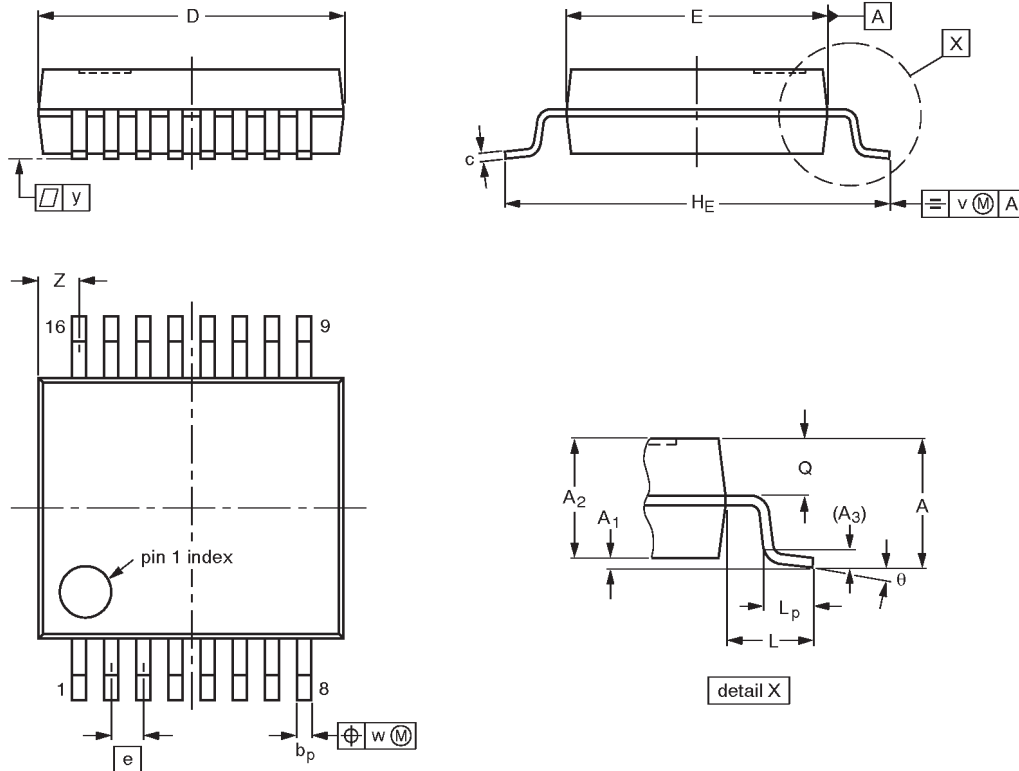
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT109-1        | 076E07S    | MS-012AC |      |  |                     | 95-01-23<br>97-05-22 |

3-to-8 line decoder/demultiplexer; inverting

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L    | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 2.0    | 0.21<br>0.05   | 1.80<br>1.65   | 0.25           | 0.38<br>0.25   | 0.20<br>0.09 | 6.4<br>6.0       | 5.4<br>5.2       | 0.65 | 7.9<br>7.6     | 1.25 | 1.03<br>0.63   | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55     | 8°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

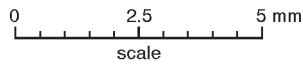
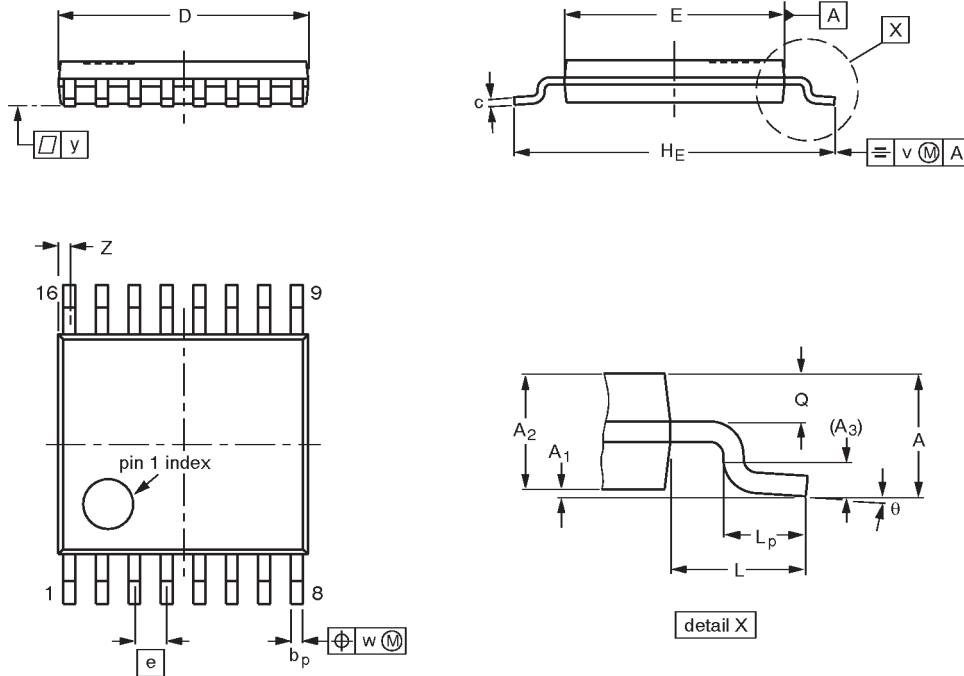
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|----------|------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                       |
| SOT338-1        |            | MO-150AC |      |  |                     | 94-01-14-<br>95-02-04 |

3-to-8 line decoder/demultiplexer; inverting

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.10   | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 5.1<br>4.9       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06     | 8°<br>0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                      |
| SOT403-1        |            | MO-153 |      |  |                     | 94-07-12<br>95-04-04 |